



NASA Electronic Parts and Packaging (NEPP) Program  
**Evaluation of Silicon on Insulator (SOI) Processes  
for Mixed Signal ASICs**



**Task Manager: Dr. Udo Lieneweg (JPL)**

## Objective

- Perform a comprehensive technology characterization of SOI Mixed Signal ASIC processes
- Partner with industry, academia, and government-sponsored laboratories to characterize SOI Mixed Signal ASIC technology for high reliability applications in an extended temperature range down to  $-150^{\circ}\text{C}$ .
- Provide critical design, functionality, and reliability information for analog device and mixed signal circuit designers relating to the characteristics and limitations of this technology.

## Deliverables

- Test report LL chip
- Test report Honeywell chip
- Device simulation (DESSIS) report
- SOI device design guidelines
- Process Qualification Reports [GSFC]
- Test report of simple SOI circuits [GRC]

## Participating Centers

- Ashok Shama (GSFC)
- GRC