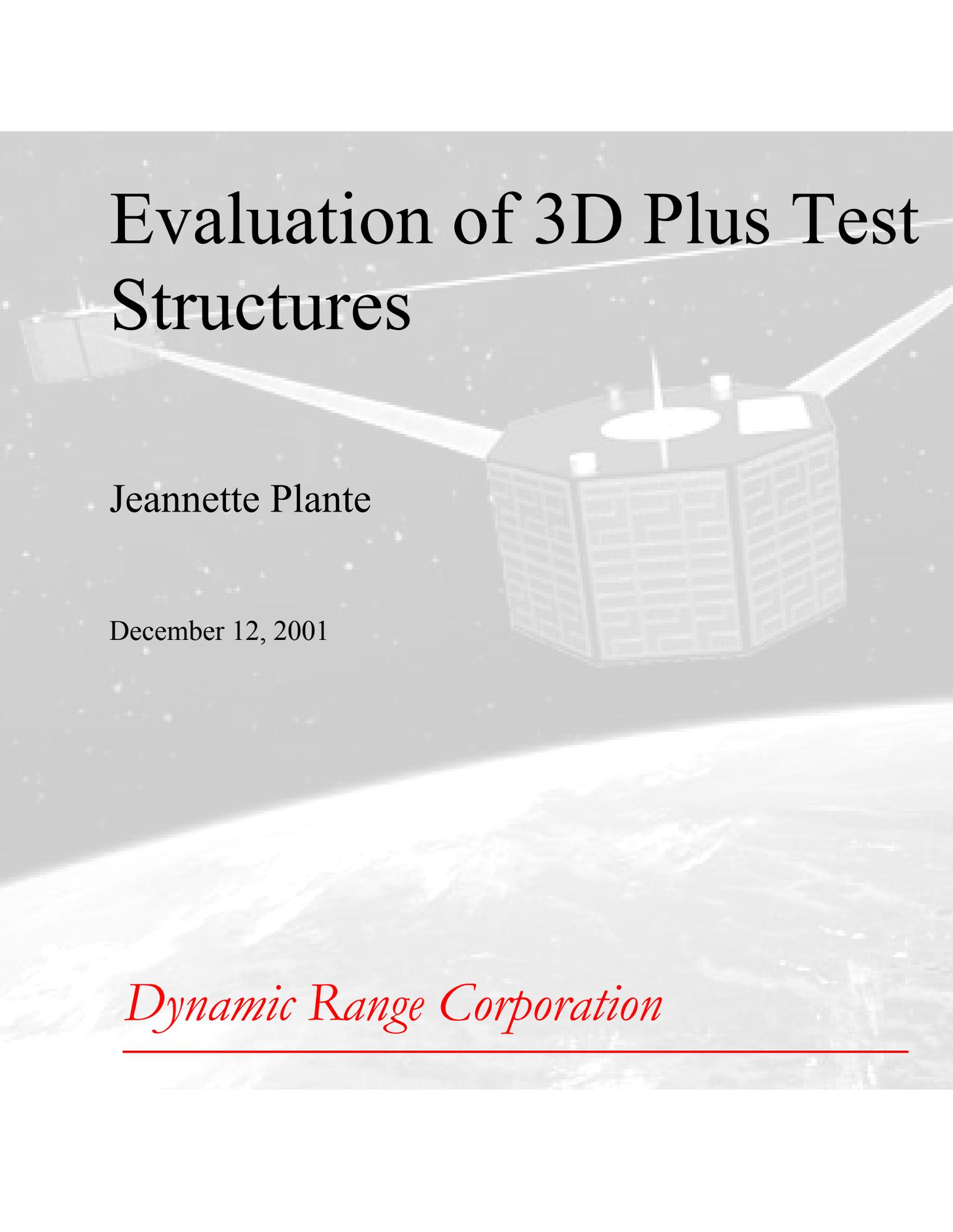


# Evaluation of 3D Plus Test Structures



Jeannette Plante

December 12, 2001

*Dynamic Range Corporation*

---

# Evaluation of 3D+ Test Structures

Jeannette Plante, Dynamic Range Corporation.  
Harry Shaw, Associate Branch Head, Code 562.

## 1. Background:

Electronics packaging in the commercial world has seen innovations that have revolutionized the industry. NASA GSFC is constantly exploring advanced electronic packaging techniques so that they too can achieve a higher degree of miniaturization, thereby contributing volume and weight reduction to advanced spacecraft systems. In this vein, test vehicles were chosen for evaluation of stacked Multi-Chip-Modules (MCMs) developed by the company 3D Plus Electronics.

3D Plus' primary products are memory modules. Custom modules have also been produced including test vehicles (daisy chain cubes for JPL, thermal cubes for JPL and the CESAR cube for ESA). Other custom cube designs have included a Temic microcontroller, an optical iris, an FPGA and a DC/DC converter. The electronic parts inside the cube can be bare electronic dice, packaged parts (plastic or ceramic) or chip passives (capacitors and resistors). They have several package designs, which enable the use of high-speed components, very small plastic encapsulated microcircuits (PEMs), and heavier and hotter ceramic packaged parts. 3D Plus' miniaturization technique typically provides an 80% reduction in footprint.

## 2. Design Concept:

3D Plus' product is a packaging technology based on plastic encapsulation of stacked up layers of electronic devices mounted to metallized polyimide film substrates. Various types of pin-outs are offered from Pin-Grid-Array (PGA) to Ball-Grid-Array (BGA). The test vehicles evaluated here were lead frame flat pack type (Fig1).

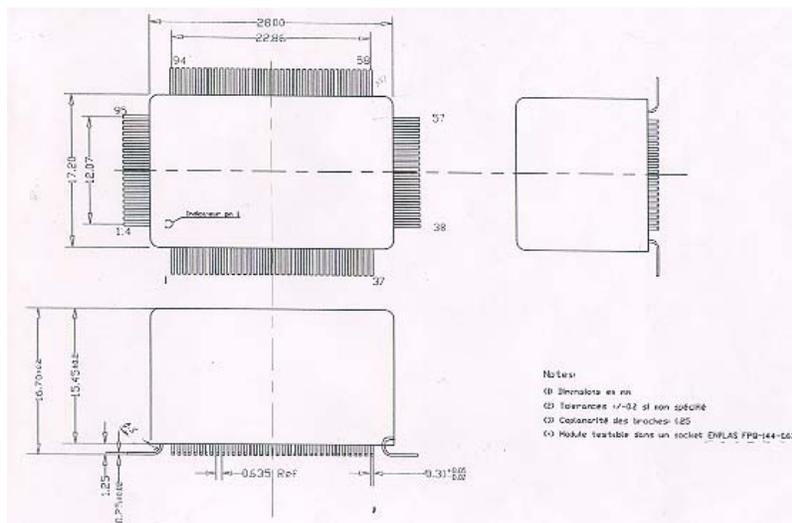


Fig.1 Lead Frame Configuration of 3D Plus Test Vehicles

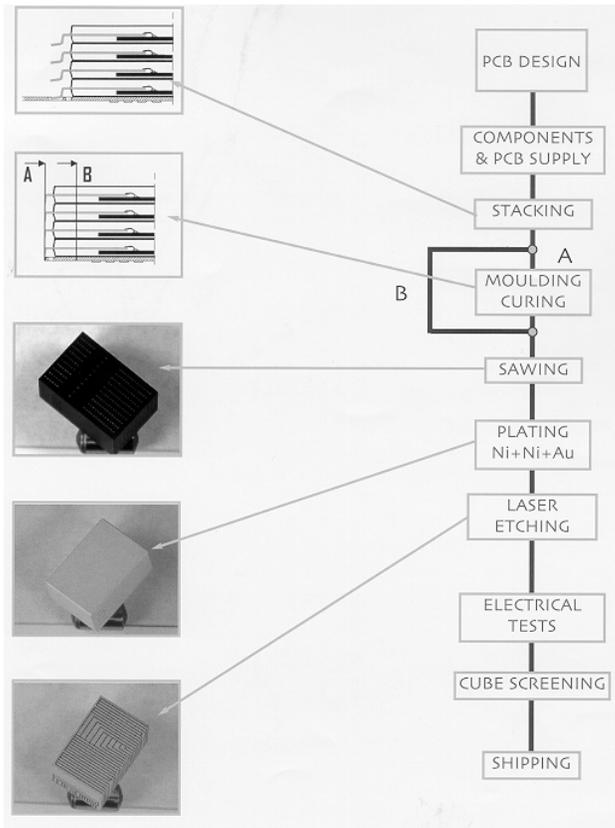
The key elements in the manufacturing process are: film design, population of the film, stack up and encapsulation, sawing, plating and scribing. This manufacturing flow is shown in Figure 2.

### 2.1 Film Design:

Metallized flexible films are used for layer substrates. They can be polyimide or FR4 BT material. The metallization is Cu+Ni+Au and is a minimum of 0.127 mm in trace width and pitch. 3D Plus subcontracts the production of the films. The metallization pattern allows interface between the internal part and the final, external surface of the cube. This is the tertiary interface counting from the board into the part. The film metallization must provide a multi-bond surface: wire bondable, epoxy bondable and solderable. This allows mixing of dice and packaged parts and passive chips. Mechanical

features in the film allow proper stack-up of the module and alignment of the secondary interface. Measurement of films which were delivered as part of the CESAR project found the resistance of the traces to be 0.8 mΩ/square.

Figure 2. 3D Plus Manufacturing Flow



## 2.2 Population of the Films:

The films are populated with packaged parts, dice and/or chip passives. 3D Plus has used glob top on their wire bonds on evaluation items though it is not known if this is a standard practice and what the material is. Population and glob topping is done at the 3D Plus facility. The populated films are then electrically tested and screened in accordance with customers' requirements.

## 2.3 Stack Up, Encapsulation and Sawing

Stack up and encapsulation is done at the 3D Plus facility. The standard products are 4 and 8 layers high, typically. The evaluation cube discussed here is 10 layers high. The lead frame is installed during this step and can be PGA or flat pack. BGA is also available. The encapsulation with Hysol FP4450 followed by sawing brings the layers together and exposes the secondary interconnects at the external faces of the module.

The sawing process cuts through the encapsulation and through the metallization tracks on the flex substrates making the secondary interconnects flush with the external layers of the cube.

## 2.4 Plating and Scribing

The final manufacturing step is plating and scribing. Plating is also a subcontracted process. Gold is plated over nickel. The plating process effectively connects all of the secondary interconnects which are exposed on each of the vertical external faces of the cube. Following plating, tracks are scribed down the side faces to arrange connection between the secondary interconnects and the pins on the lead frame or BGA and to isolate secondary interconnects from each other (some secondary interconnects are not separated from each other with a scribe line when bussing is desired). The scribing process is done at the 3D Plus facility using a computer-controlled laser. The scribe design makes use of available "no

connect” pins on the lead frame to provide individual control to each of the layers. Like-pins, such as address or data pins can be tied together. 3D Plus reports the limit to this process is a minimum width of 0.380 mm.

### 3. CESAR Test Vehicles

Specially designed test structures, manufactured using standard 3D+ processes, were evaluated cooperatively by ESA, CNES, 3D+ and NASA GSFC. The testing and the design of the evaluation structures was intended to explore the ability of the process to produce rugged, stacked, electronic devices which survive typical conditions of space flight use. The layers of the stack include special devices that are used to detect:

1. moisture ingress
2. torsion stress during temperature changes
3. the effect of the stacking on chip resistors and capacitors mounted on the same layer as silicon devices
4. the effect of the stack design on typical memory chips, both packaged and in die form
5. the ability of the cube to dissipate heat with and without an internal heat sink.

Table 1 describes the composition of the layers. Figure 3 provides the same information pictorially.

Table 1. Composition of the 10 Layer Test Structure

Layer	Devices
10	Corrosion chip and contact continuity pattern
9	Strain gauge and 5kΩ chip resistors
8	DRAM TSOP with all leads terminated inside of the cube
7	DRAM TSOP with half of the leads terminated inside of the cube and half terminated at the cube side face, 22nF ceramic chip capacitor and two 10 nF ceramic chip capacitors
6	Thermal chip with no heat sink
5	Strain gauge, 100 kΩ chip resistors, 200 daisy chained wire bonds
4	Thermal chip with heat sink
3	DRAM TSOP with half of the leads terminated inside of the cube and half terminated at the cube side face, two 100 nF ceramic chip capacitors and two 10 uF tantalum capacitors
2	DRAM TSOP with all leads terminated inside of the cube
1	Corrosion chip and contact resistance pattern

### 4. Test Units:

The test parts were contained ten layered circuits of those parts noted in Table 1. ESA and CNES used 22 units for their portion of the evaluation and NASA GSFC used 9. Two sets of unencapsulated, populated, layers were provided to facilitate testing and final analyses.

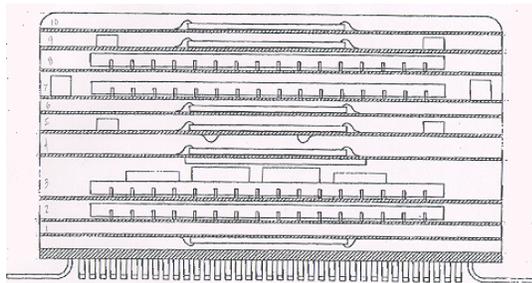
The DRAM devices in layers 2, 3, 7 and 8 were Samsung 16M x 4 bit KM44V16104A (4k refresh). The tantalum capacitors are 10 uF/10V and 2.2 uF/10V. The ceramic capacitors are 100 nF/50V, 22nF/50V and 10 nF/50V. The resistors are 5kΩ/125mW, 100 kΩ/125mW, 5kΩ/250mW and 100kΩ/250mW. The corrosion chip and the thermal chip were custom made for this evaluation. The strain gauge was identified by 3D+ as made by ACM. Detailed pin assignments and internal connections were provided to NASA GSFC by 3D+.

### 5. Testing:

#### 5.1 Test Plans

ESA and CNES managed the portion of the test plan that includes the following tests:

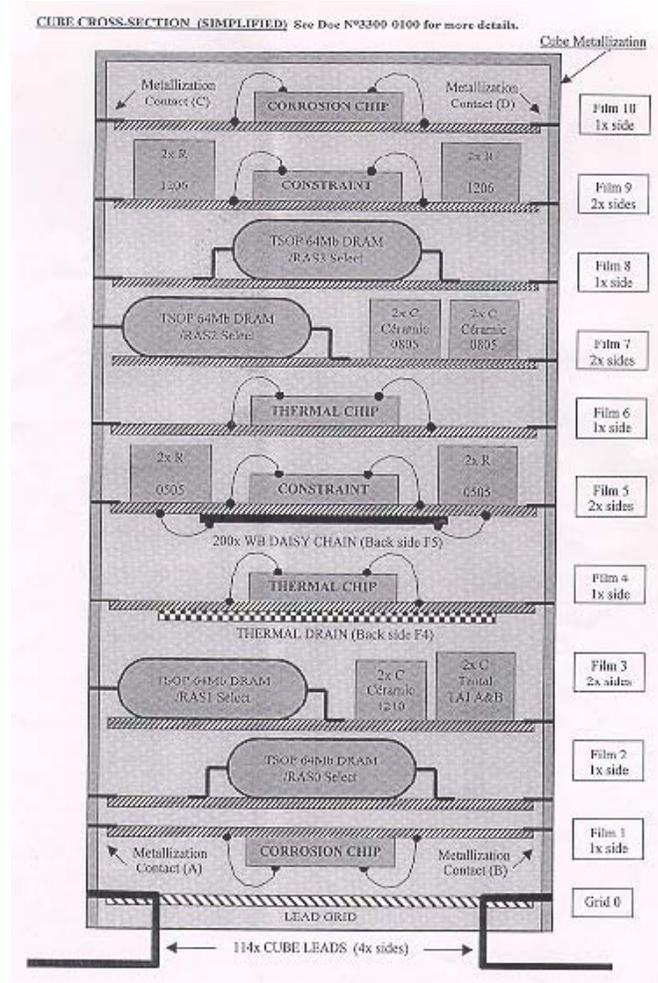
- preconditioning thermal (cycling) vacuum
- 500x thermal cycling (-55°C to +125°C)
- temperature humidity bias (+85°C/85%RH/1000 hrs)
- high temperature bake (+125°C, 2000 hrs)
- power cycling (30k x on/off, 120 sec on +110°C, 60 sec off +40°C)



(a.)

Figure 3. CESAR Test Vehicle:

- Scaled
- Element Positions



(b.)

The test flow is shown in Figure 4. NASA/GSFC provided the testing that is detailed in Figure 5 consisting of:

- CSAM,  $\mu$ focus X-ray
- thermal conditioning (+125°C, 48 hrs)
- voltage conditioning (+125°C, 320 hrs)
- thermal characterization
- vibration (sine & random)
- mechanical shock
- 85% humidity / 85°C
- finite element modeling

The NASA GSFC test flow conditions are shown in Table 2. Electrical tests were performed after each environmental test.

## 5.2 Test Unit Serialization and Sample Preparation

Each test unit was serialized as follows: FM13 (control), FM3, FM5, FM9, FM10, FM12, FM14, FM16, and FM17. FM13 occupied a board by itself and it was not conformally coated (Assembly 1). FM 14 and 15 were mounted to a test board and then conformally coated with Parylene C (Assembly 2). FM12 and FM16 were mounted to a test board and also

conformally coated with Parylene C (Assembly 3). FM3 and FM17 were mounted to a test board and then conformally coated with Uralane (Assembly 4). FM9 and FM10 were mounted to a test board and also conformally coated with Uralane (Assembly 5).

Figure 4. CNES Test Flow

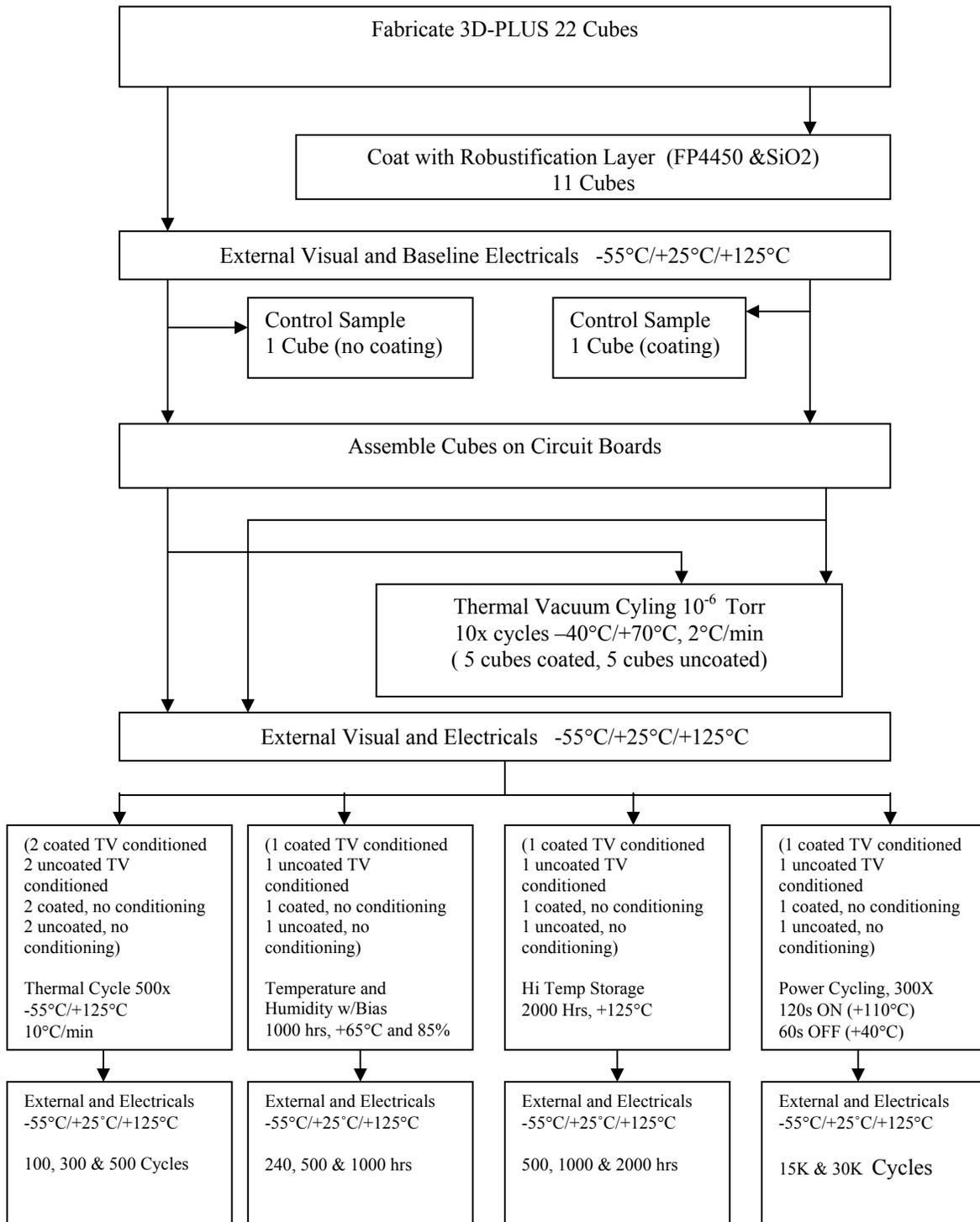
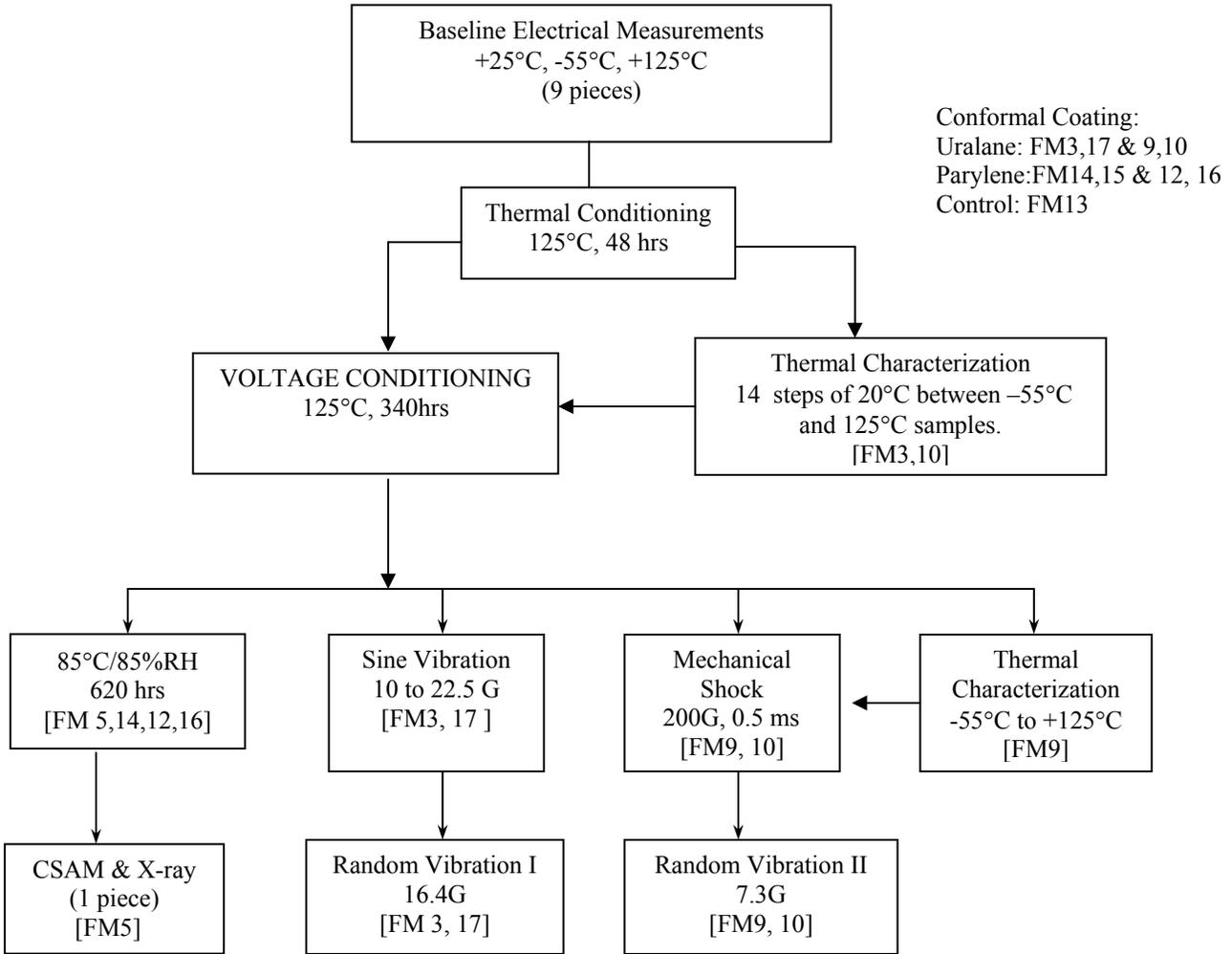


Figure 5. NASA GSFC Test Flow



### 5.3 Electrical and Environmental Test Conditions.

#### 5.3.1 Baseline electrical:

Electrical tests were done to establish a baseline of performance after every evaluation step, using the approach described in detail in Appendix I. Three temperature electricals were only taken at the beginning of the evaluation (this does not include the thermal characterization test). All other electrical data were taken at 25°C. The results of the electrical measurements are shown in Appendix II.

#### 5.3.2 Thermal Characterization:

Electrical characterization of the cubes was done to perform real time monitoring of the various test layers during increasing and decreasing thermal stress. The parts were exposed to the temperatures shown in Table 3. The time for transition rate between each temperature was 5°C/minute. The dwell at each temperature was 20 minutes. Electrical monitoring was done for the devices on each layer following a 10-minute dwell period.

5.3.3 Voltage Conditioning: A circuit was set up to bias as many of the internal components as possible. The biased parts were baked at 125°C for 340 hours.

5.3.4 85°C/85% RH. Samples was exposed to the heat and humidity test specified in MIL-STD-202, Method 103 to quantify the ability of Parylene C to protect the parts from moisture damage. The duration was 640 hours.

Table 3. Conditions for Temperature Characterization

Step	Temperature
1	25°C
2	45°C
3	65°C
4	85°C
5	105°C
6	125°C
7	85°C
8	55°C
9	25°C
10	10°C
11	-10°C
12	-30°C
13	-55°C
14	25°C

### 5.3.5 Sine Vibration.

Sine vibration was done in accordance with MIL-STD-202, Method 201, Condition A. Figure 6 shows the sine vibration profile used.

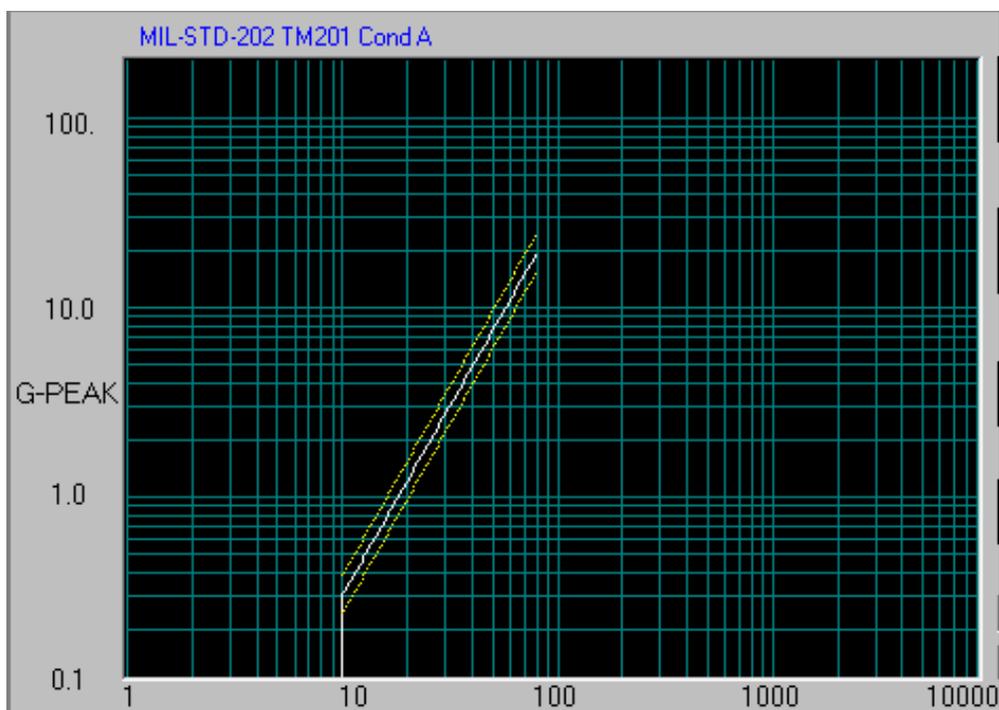


Figure 6.1 Spectrum

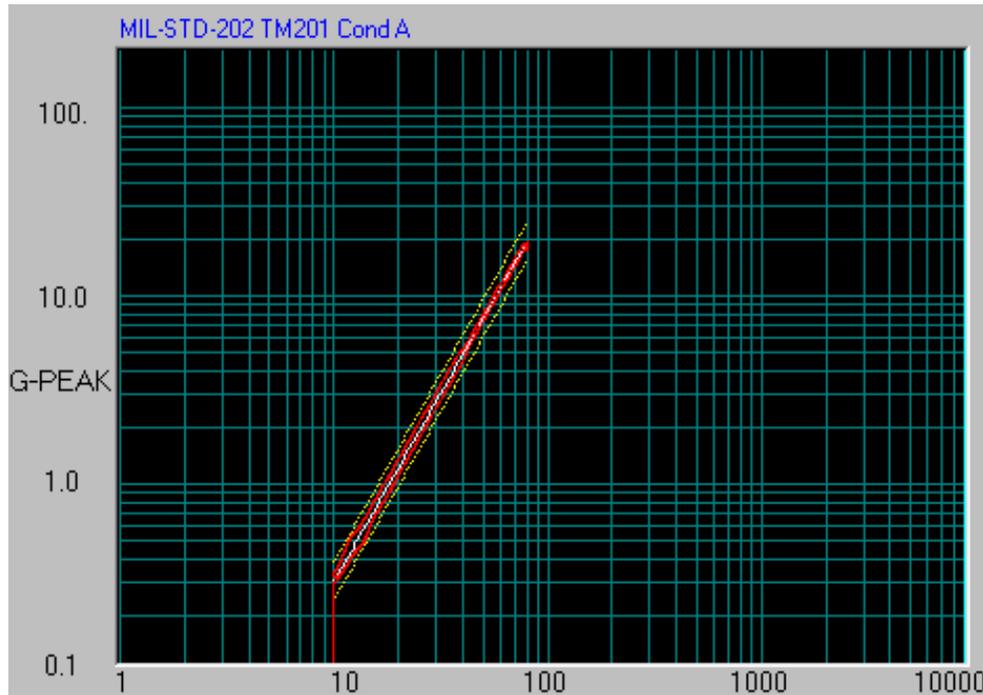


Figure 6.2 Resulting Profile

### 5.3.6. Mechanical Shock

Mechanical shock was performed in accordance with MIL-STD-883, Method 2002, with a peak level of 200g and a pulse duration of 0.5 ms. Figure 7 shows that shock was applied in the X,Y and Z axis in an upward and downward direction. All layers were electrically tested after the test.

Table 2. Test Methods and Conditions

Step	Test	Serial Number	Test Method	Conditions
1	Electrical Test & Visual Examination	All samples	Ref (1), Para. 10 and 11	-55°C, 25°C and 125°C
2	Thermal Conditioning	All Samples	Ref (2), Method 1008	Condition A, 125°C, 48 hours, unbiased
3	Voltage Conditioning	All Samples except FM13	Ref (2), Method 1015	+125°C, 368 hours, follow by electrical measurements at +25° (See step 2)
4	Temperature Characterization	FM 3, 9, 10	Para. 5.3.2 herein	+25°C to +125°C to -55°C to +25°C, taking electrical measurements at 20°C increments.
4	85°C/85%RH	FM 15, 14, 12, 16	Ref (3), Method 103	Bias will be applied in accordance with Table 3, Para. 5.6 below.
5	Sine Vibration	FM3, 17	Ref.(3), Method 202	10 to 22.5 Hz, 1 minute per sine sweep, 2 hours per axis, x, y & z axis
6	Mechanical Shock	FM 9, 10	Ref (2), Method 2002	Condition A, 200g, 0.5 ms pulse, no electrical load

Table 2. Continued

Step	Test	Serial Number	Test Method	Conditions
7	Random Vibration I	FM 3, 17	Ref (2) Method 2026	Condition E, 15 minutes in the x, y and z directions, 0.2 g <sup>2</sup> /Hz, electrical monitoring shall be done during the test, Para. 5.10.
8	Random Vibration II	FM 9, 10	Ref(2), Method 2026	Condition B, 15 minutes in the x, y and z directions, 0.04 g <sup>2</sup> /Hz, electrical monitoring shall be done during the test, Para. 5.10.
9	CSAM	FM5	MIL-STD-883C, TM 2030	
10	DPA	As Needed		

Ref(1): Specification De Tests, D'Essais De Selection & D'Evaluation, Structures D'Evaluation Technologie 3D, JFG Consultant, 3/99

Ref(2): MIL-STD-883

Ref(3): MIL-STD-202

Ref(4): Test method specified herein.



Figure 7a. Pictures of Test Set-Up in each directions

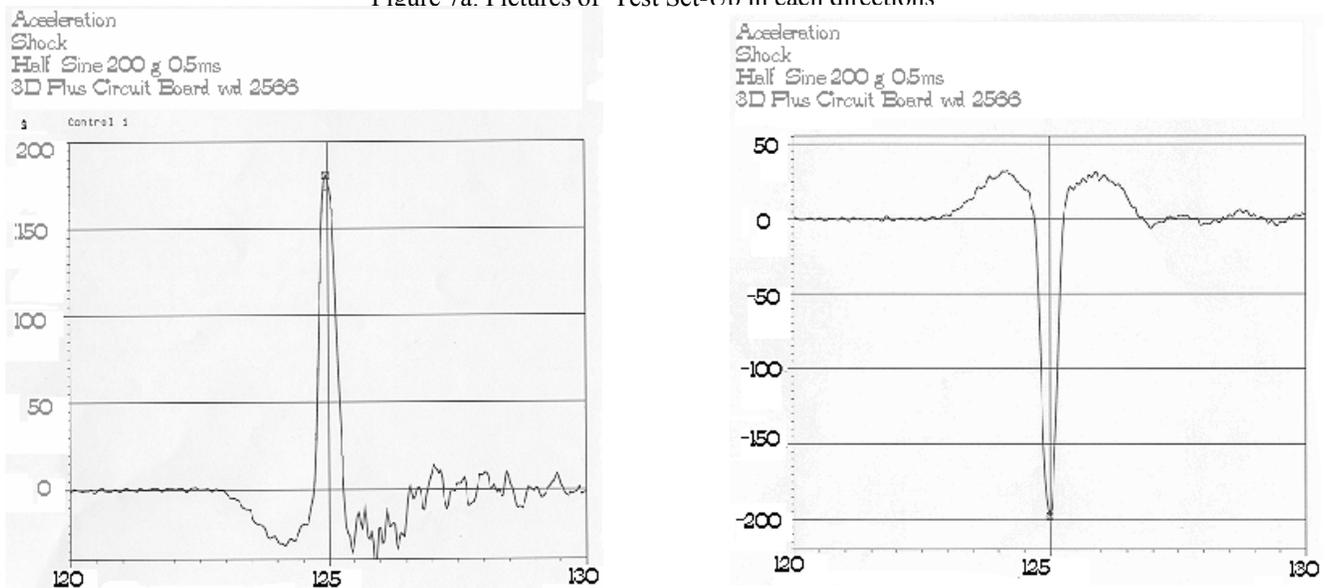


Figure 7b. Shock Profile

### 5.3.7 Random Vibration

Random vibration testing was performed in accordance with MIL-STD-883, Method 2026 in the X,Y and Z-axes. The 4.5" x 4.5" test board was rigidly mounted at the corners and at the center to limit board effects. Random Vibration I uses Condition E and Random Vibration II used Condition B. Figure 8 shows the applicable profile.

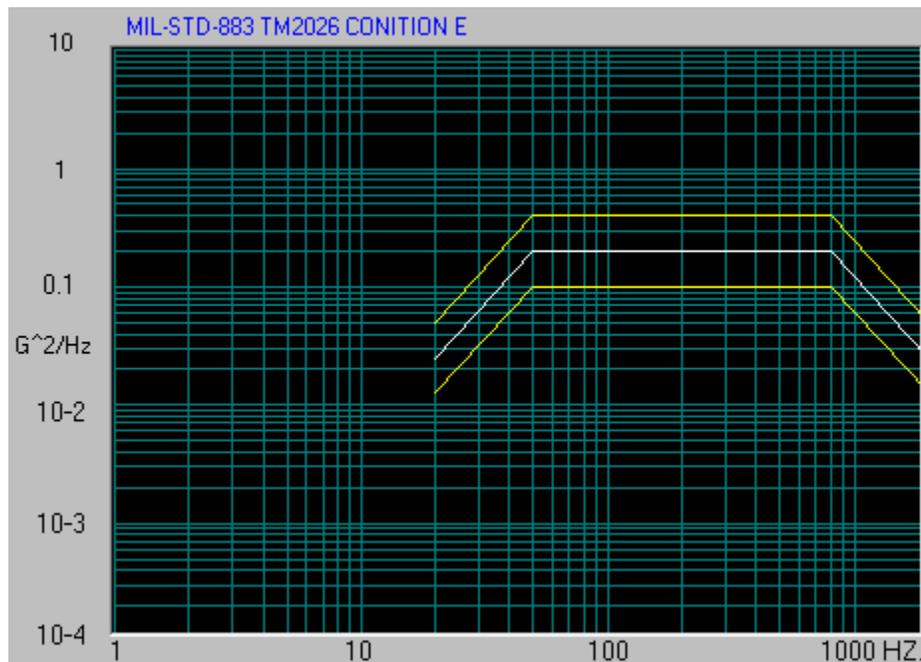


Figure 8a Spectrum – Vibration I

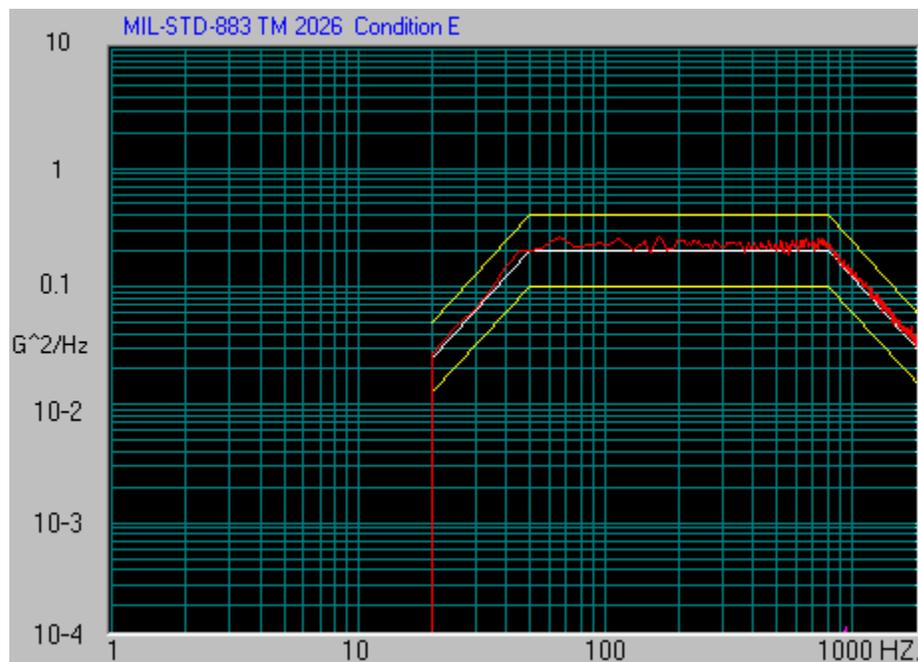


Figure 8b Resulting Spectrum – Vibration I

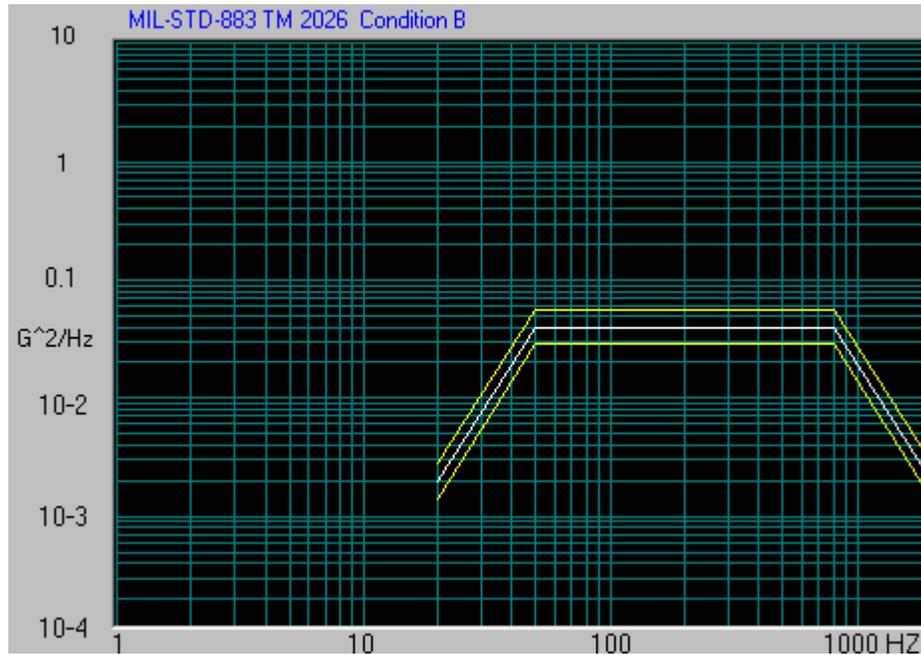


Figure 8c. Spectrum – Vibration II

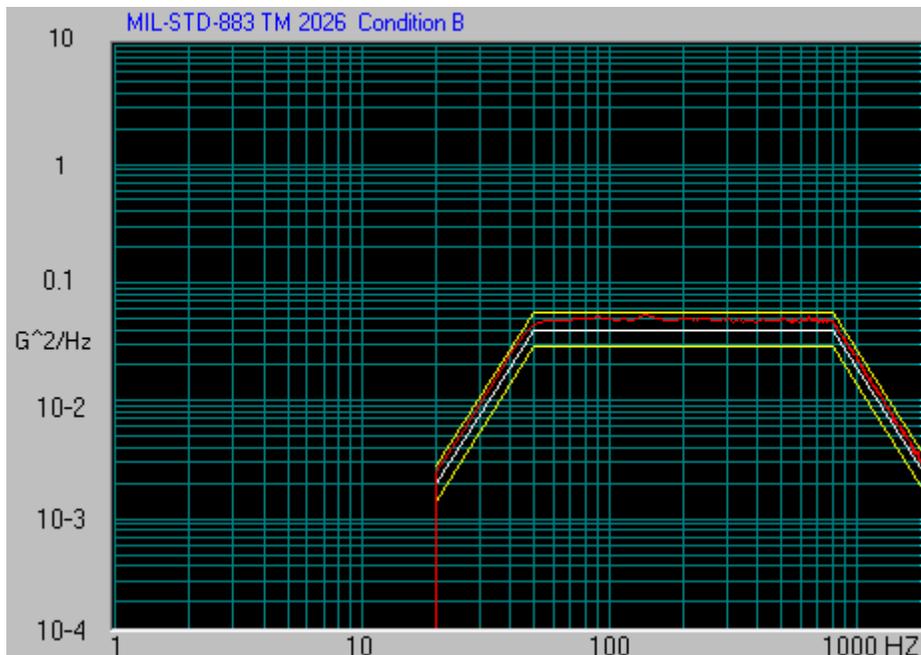


Figure 8d. Resulting Profile – Vibration II

### 5.3.8 CSAM and DPA

Scanning acoustic microscopy was employed to understand if the tool was at all useful with this type of layered, PEMs-like device. A DPA is in process to understand three data points that fail the electrical limits.

### 6.0 Finite Element Analysis:

Finite element modeling was used to show theoretical stress caused to the part due to static and dynamic vibration and thermal stress and thermal cycling. This analysis was performed for the evaluation stack design prior to testing. The results of this analysis gave cause for changing some of the conditions of the tests described above. Heavy conformal

coating was used to give the parts a better chance of passing the Vibration II test. Appendix III contains the results of the FEA.

## 7.0 Results

### 7.1 The Data Graphed

The data was collected by test unit (FM#), by device (layer) and by test. Appendix II contains graphs by device over the tests performed. All of the data, except three points, was within family and agreed with that collected by ESA. The three out of family data points were as follows:

1. Reverse current on diode 3, layer 6 of device FM17, measured to be shorted. This was an “as received failure”. ESA will pursue pre-ship records to determine if it was a result of handling during shipping or board assembly.
2. DRAM Iddq, in device FM3. This measurement combined Iddq for all four devices in the cube so it is unclear which or more failed. This part is being DPA'd by CNES. The failure occurred during thermal characterization while ramping to cold (between -30°C and -55°C).
3. Strain Gauge element 1 and 2 on layer 9, device FM5. This same device failed in some of the ESA samples. A DPA was performed which found metallization defects on the die, not believed to be related to the packaging.

The following was observed in the data:

1. Corrosion monitor resistance: The data was consistent over the testing, though some of the tracks on layer 10 baselined higher than those on layer 1. Layer 10 was also slightly more sensitive to moisture.
2. Corrosion monitor isolation: The data was all within specification though layer 10 seemed to be more sensitive to moisture (85/85 test). The sensitivity to the vibration tests may have also been moisture related as those tests were conducted during the most humid time of the year.
3. Contact Continuity: All measurements showed continuous circuits with no significant sensitivity to moisture.
4. Daisy Chain Wire Bonds: All measurements showed continuous circuits with no permanent sensitivity to moisture or other environment changes.
5. Strain Gauge: The dice in FM3 showed a sensitivity to temperature while the dice in FM9 and FM10 did not. No failure trends were encountered over the mechanical and moisture testing. FM5 had a failure during baseline electricals and voltage conditioning (see above).
6. a. Thermal Monitor, Vf, 0V and 12V on Heaters: No out of family data was encountered. No difference could be detected between the layer with and without a heat sink.  
b. Thermal Monitor, IR, 0V and 12V on Heaters: One device was received in a failed condition (see above). For the remaining data, no out of family data was encountered. No difference could be detected between the layer with and without a heat sink.
7. Capacitors: No significant change occurred over all tests.
8. Resistors: All measurements were within specification.
9. DRAM: A failure was apparent following Thermal Characterization and Sine vibration which continued through the subsequent Random Vibration I test (noted above). All other measurements were within specification.

### 7.2 CSAM

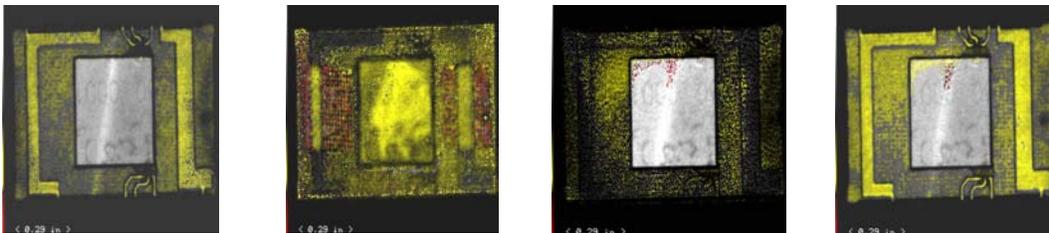


Figure 9a. Overall 1

9b. Below Die

9c. Die Surface

9d. Overall 2

It was fairly difficult to apply CSAM because the part was very thick with so much area of interest through the z-axis. Once a proper location could be identified, good images of the polyimide film, the metallization, glob top and the die could be discerned. We were not able to interpret the presence or not of voids under the die. CSAM may be useful prior to a planned FA or DPA but was not conclusive for a non-destructive evaluation tool in this case.

## 8.0 Conclusions

The 3D Plus packaging technology provides very high density and stable performance in rugged environments. The parts are suitably rugged with respect to high and low temperature, humidity, shock and vibration. Care must be given to properly stake the parts when they are as high as these evaluation cubes. The data did not indicate that there was a need for special moisture protection though these being non-hermetic, care should still be given to keep the parts as dry as possible to ensure long life. No significant performance difference was noted between the layer with the heat sink and the one without the heat sink. The results for the temperature cycling and long term temperature tests, performed by CNES and not presented here, were similarly stable for all of the layers (to be published in 2002).

Until the DPA has been completed it is inappropriate to give this technology an unconditional recommendation. However, it was exposed to severe environmental stress and thousands of passing data points were collected indicating that it is highly suited for use in extreme environments where normal derating and protection practices, for temperature and moisture, are used.

### Recognition:

Special thanks are extended to the many people who made this evaluation possible including: Harry Shaw of NASA GSFC, Dr. Dave Gerke of JPL, Mr. Alberto Boetti of ESA, Mr. Marc Billot of CNES, Dr. Christian Val and Mssr. Remy Frank, Pierre Maurice and Philippe Prieur of 3D Plus, Mssr. Michael Leibforth, Brandon G. Lee, Chris Kiely and Brendan Spear and Ms. Roberta Neyer of Dynamic Range Corporation.

## APPENDIX I: TEST SET-UP

### TEST 1: CORROSION MONITOR TRACE RESISTANCE

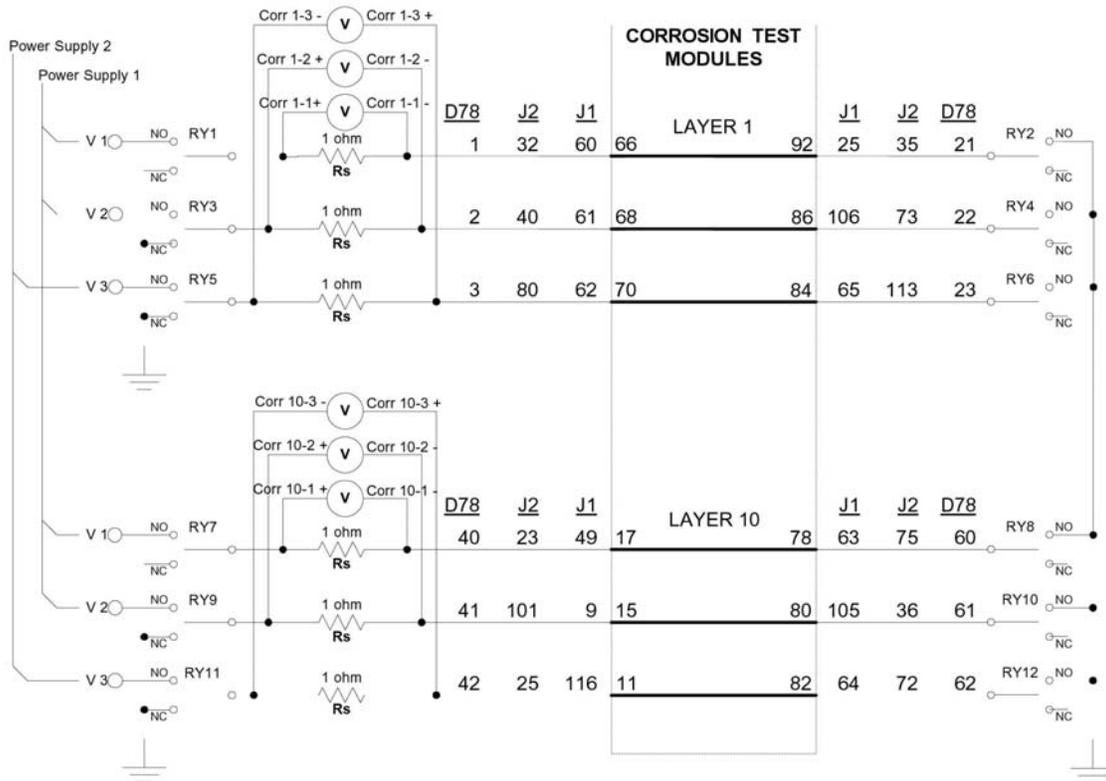
The corrosion test chip contains three aluminum traces with a 10µm line width, 10µm pitch, and 1µm thickness. Each trace is in series with a 1 ohm resistor. Each trace is tested separately. Voltage is measured across the 1 ohm resistor.

Resistance in the corrosion module is determined by  $R = R_S * V_i - V / V$ , where  $V$  = value of the voltage measured across the 1 ohm resistor,  $R_S = 1$  ohm, and  $V_i = V1, V2, \text{ or } V3$ .

$R_{\text{typical}}$  for each Resistance element is 763.5 ohms.

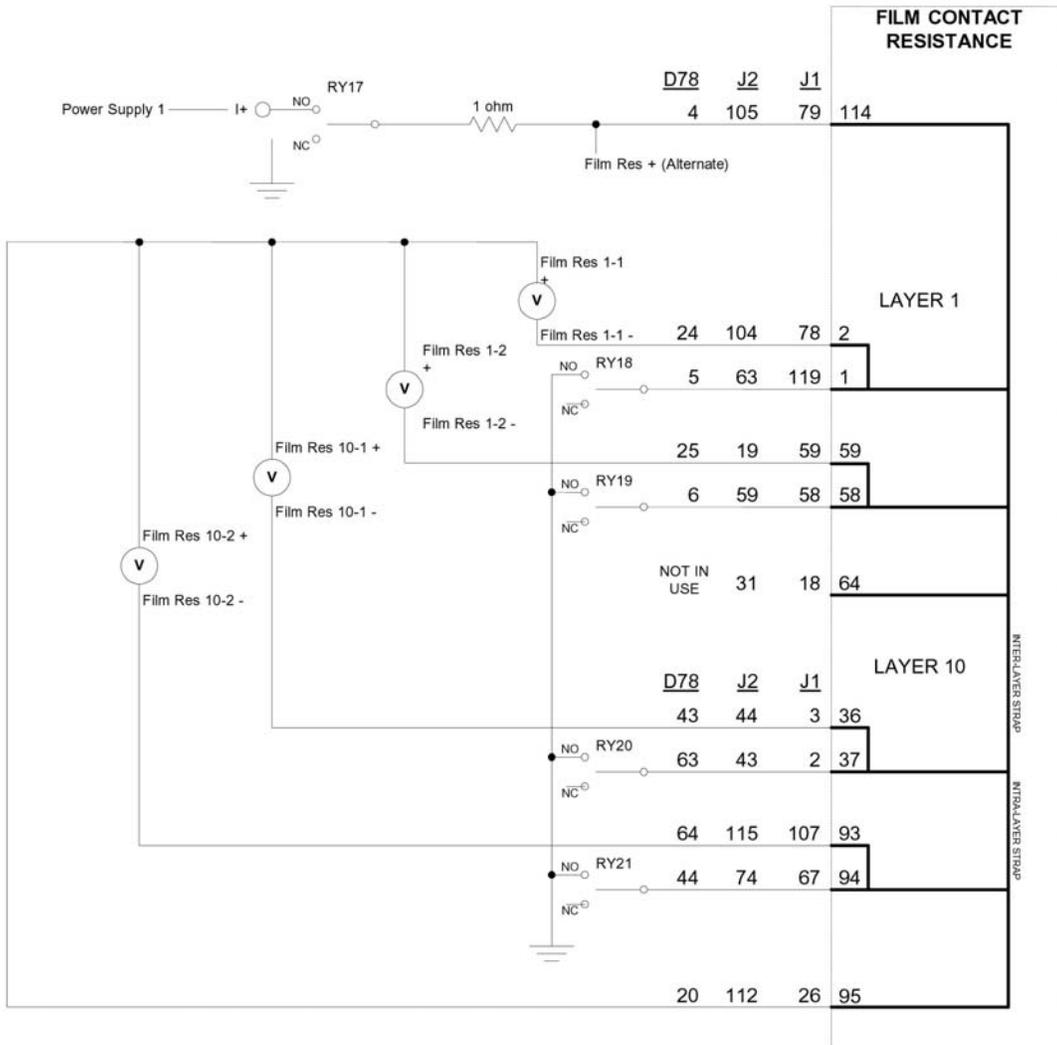
### TEST 2: CORROSION MONITOR TRACE ISOLATION

All three traces in a layer are tested simultaneously for leakage caused by corrosion. Ground relays are opened, then voltage is measured across the resistors. Current in each trace is determined by  $I = V / R_S$ , where  $V$  = value of the voltage measured across the 1 ohm resistor, and  $R_S = 1$  ohm.



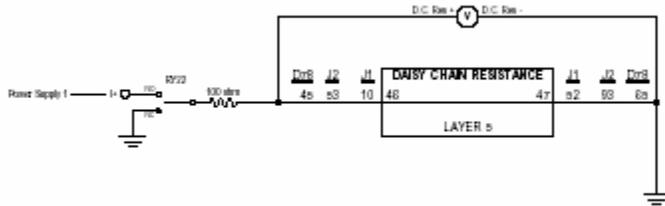
### TEST 3: FILM CONTACT CONTINUITY

The film is constructed of tracks conductive pastes, daisy chained together by wirebond connections. Each contact is four point probe tested; no more than one relay is closed at a time. Resistance is determined by  $R = V/I$ , where  $V$  = value of the measured voltage and  $I = 300$  mA. Pass is Resistance < 1 Ohm



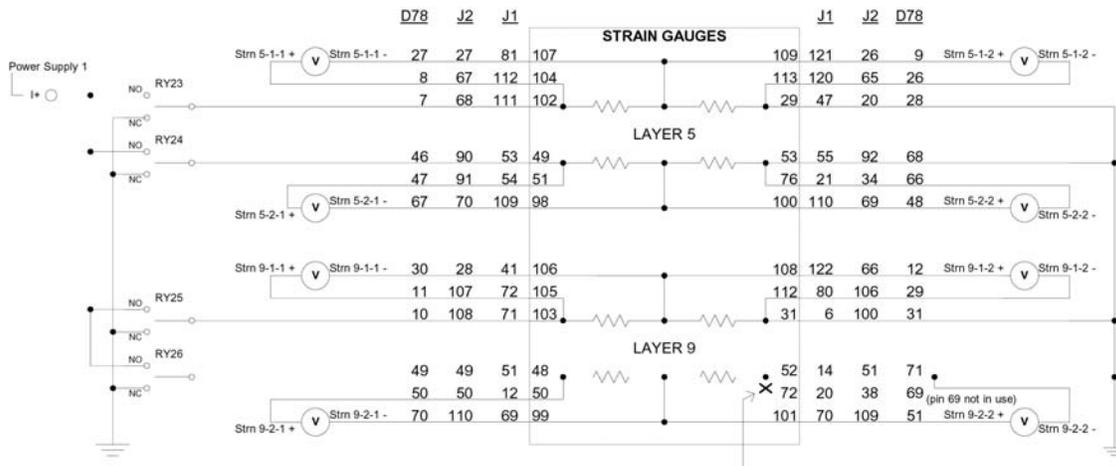
### TEST 4: DAISY CHAIN CONTINUITY

The film is constructed of tracks conductive pastes, daisy chained together by wirebond connections. Voltage is measured across the Daisy Chain Resistance. Daisy Chain Resistance is determined by  $R = V/I$ , where  $V$  = value of the measured voltage and  $I = 10 \text{ mA}$ .  
 Pass is Resistance < 1 Ohm



### TEST 5: STRAIN GAUGES

Voltage is measured across each of the series resistors in each loop. Only one relay is closed at a time. Resistance is determined by  $R = V/I$ , where  $V$  = value of the voltage measured across the unknown resistance and  $I = 1 \text{ mA}$ .  
 Pass is Resistance = 3.5 KOhms  $\pm$  5%



## TESTS 6 AND 7: THERMAL MONITOR

(Heaters used only in Test 6.)

Heaters: V1 = +5V, +12V, +15V, +18V (Power 1)

Voltage is measured across the series resistors in each loop. During testing, only one relay should be closed at a time. When using the heaters, both relays may be closed. Resistance in the heater is determined by  $R_H = R_S \cdot V_i - V / V$ , where  $V =$  value of the voltage measured across the 10 ohm resistor,  $R_S = 10$  ohm, and  $V_i = V_1$ , ie, +5, +12, +15, or +18V.

Typical heater resistance is 300 Ohms.

Pass is Resistance = 300 Ohms  $\pm$  5%

Diodes: (Diode tests performed in both Test 6 and Test 7.)

Forward Test:

$I = -1$  mA (Power 2)

Current Relay is set to Current input, Voltage

Relay is set to

Ground.

Voltage drop across

Diode is measured.

Pass is  $0.5V < V_f < 1V$

Reverse Test:

V2 = -12 V (Power 2)

Current Relay is set to

10Kohm sense

resistor.

Voltage Relay is set

to Voltage input.

Voltage across the

sense resistor  $R_d$  is

measured.

Current is calculated

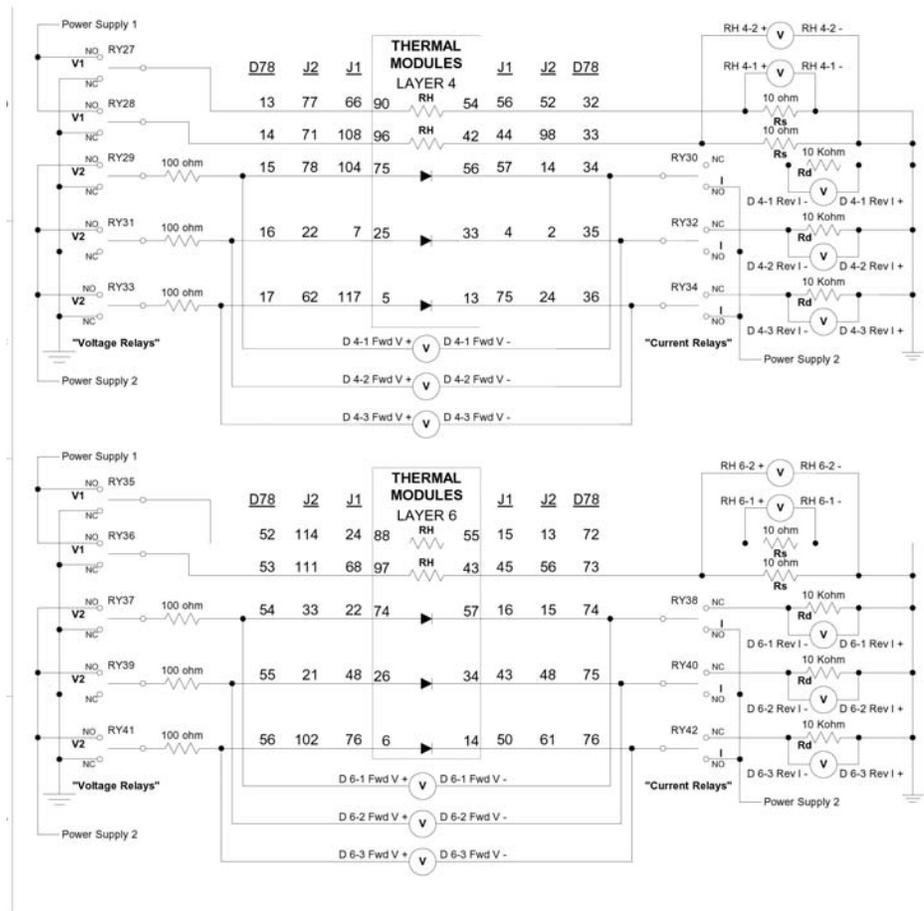
by  $I = V / R_d$ , where  $V =$

value of the voltage

measured across the

10Kohm resistor, and

$R_d = 10$  Kohm.



### TEST 8: CAPACITOR BLOCKS

Vi is from the Signal Generator

Vi = 9Vpeak-to-peak @ 100kHz, Vmin = 0V and Vmax = +9V

The AC voltage must be superimposed on a DC offset (+4.5 VDC) so that Vmin => 0V and Vmax =< +10V. (Vmax nominally +9V).

(The signal generator that is available to generate Vi is not amplitude-stable at 100kHz; thus this voltage will have to be monitored as part of the test setup.)

Only one relay is closed at a time.

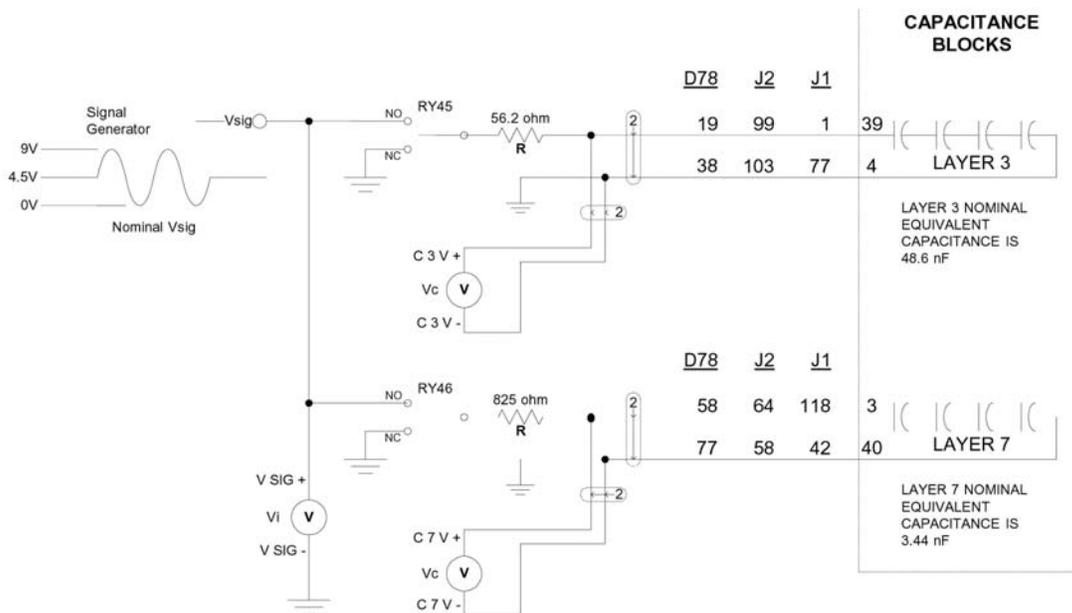
AC voltage is measured by sampling across the capacitor block.

Capacitance is determined by  $C = ((Vi^2 - Vc^2)^{1/2}) / (2 * \pi * f * R * Vc) - Co$ , where Vc = peak-to-peak value of the voltage measured across the capacitor block, Vi = measured peak-to-peak value of the input voltage, R = 56.2 ohm or 825 ohm (depending on the test in progress), f = 100kHz, Pi = 3.14159..., and Co is a constant resulting from the twisted pair wiring and test setup.

(Co is measured at test by determining "C" with the Module Unit that contain the Capacitor Blocks under test not connected.)

Layer 3 Pass is Capacitance = 48.6 nF ± 15%

Layer 7 Pass is Capacitance = 3.44 nF ± 15%



**TEST 9: RESISTANCE BLOCKS**

+I is from Power 1

+I = 1.0 mA, nominal as commanded, for all tests.

The actual value must be determined and used as part of the calculations.

Only one relay is closed at a time.

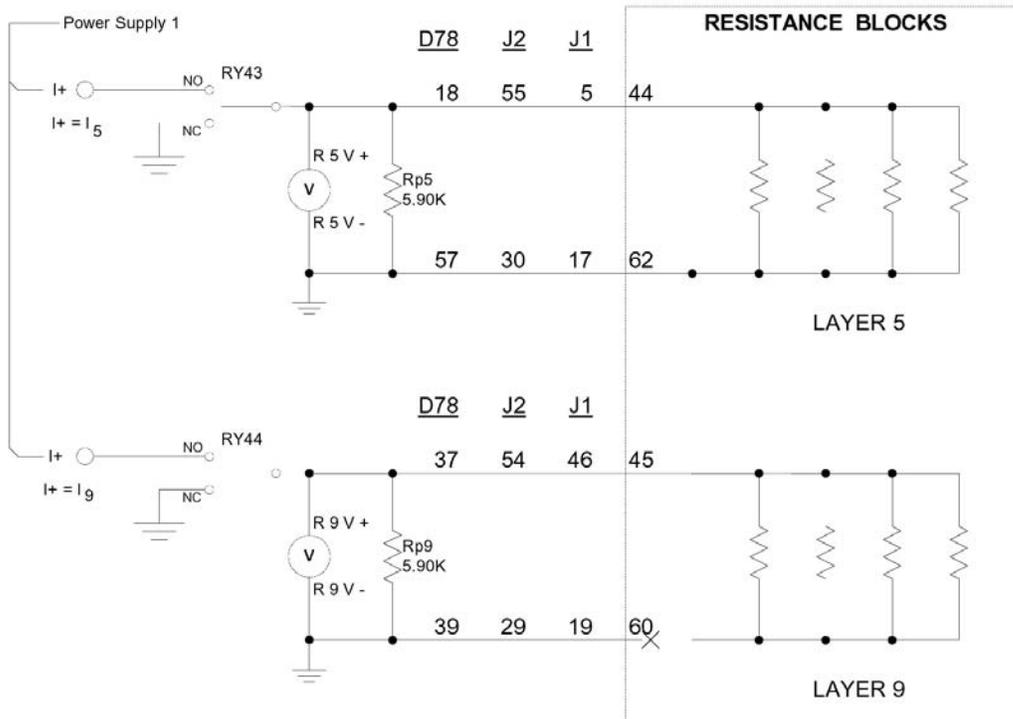
Voltage is measured across the Parallel Resistor Block.

The Resistance is determined by  $R = VR_p / (IR_p - V)$ , where V = value of the measured voltage, Rp5 and Rp9 have measured values as follows:

Rp5 = 5.90 Kohms and Rp9 = 5.88 Kohms, and Constant Current I has measured values as follows:

For  $V < 3.5V$ , then  $I = 1.06 \text{ ma}$ , else  $I = 1.13 \text{ ma}$ .

Pass = Nominal Resistance (1.25K or 25.0K)  $\pm 10\%$



## TEST 10: DRAM TEST

VCC = +3.3VDC

The quiescent current (Iccq) is measured for the DRAMs in each cube. Separate measurements are made for each DRAM in its enabled and disabled state.

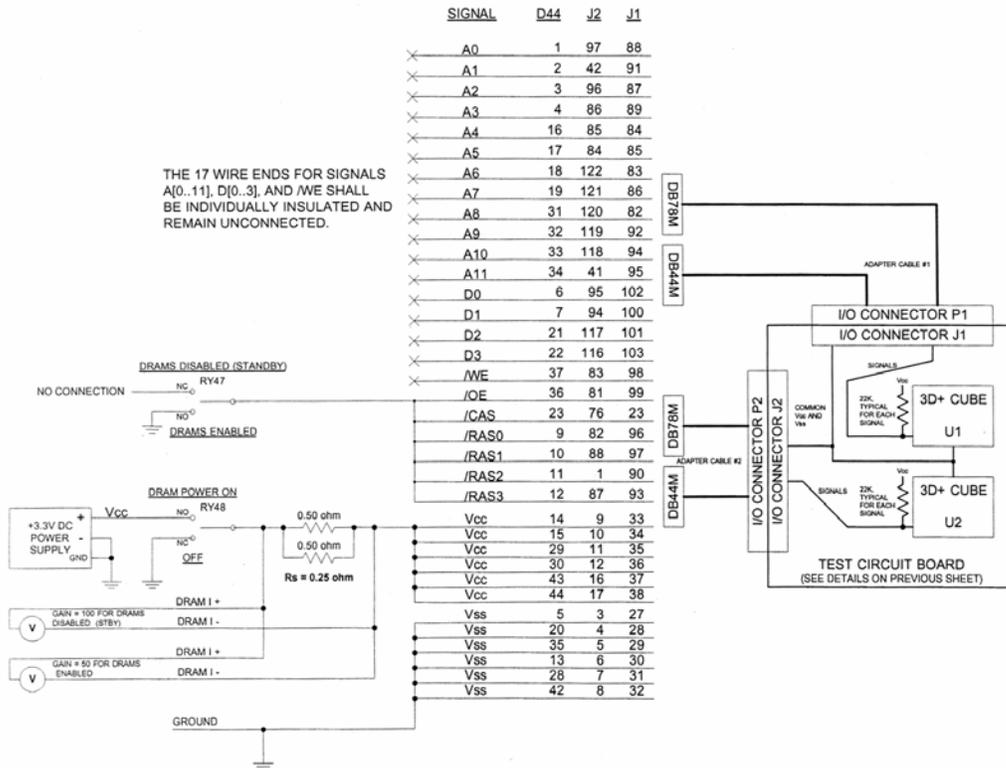
Two Separate A/D channels with different gains are provided by the Labview software. Gains of 100 and 50 were used in both the disabled (standby) and enabled condition.

Iccq is calculated as follows:

$I_{ccq} = V/R_s$ , where  $V$  = value of the voltage measured across  $R_s$  (2x .50 ohm resistors in parallel = .25 ohms).

Iccq standby per cube = 2.0mA max.

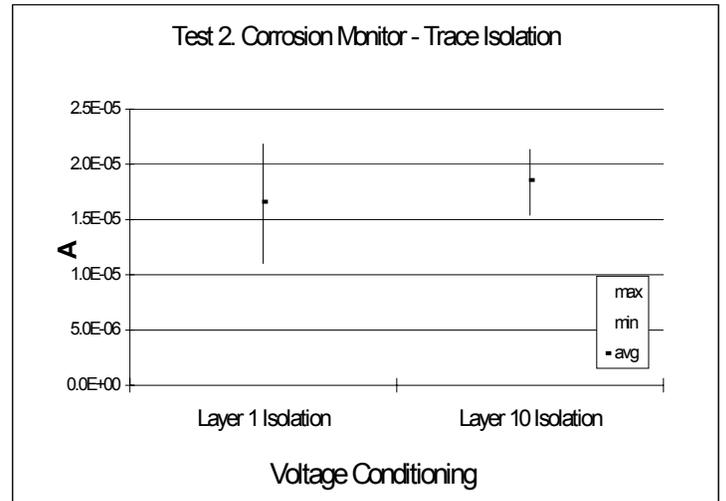
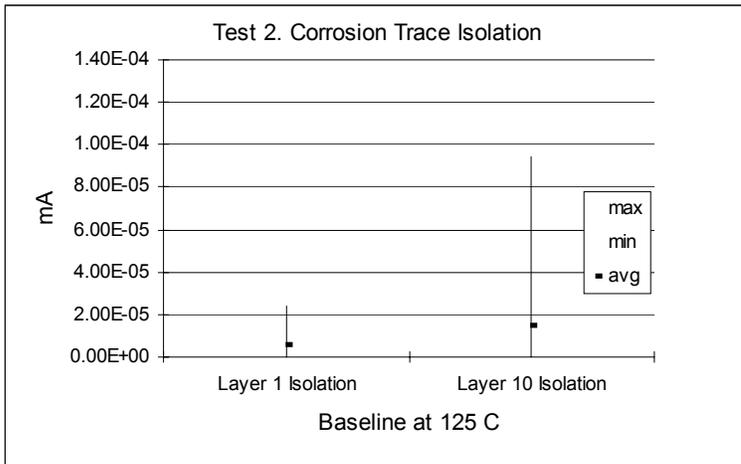
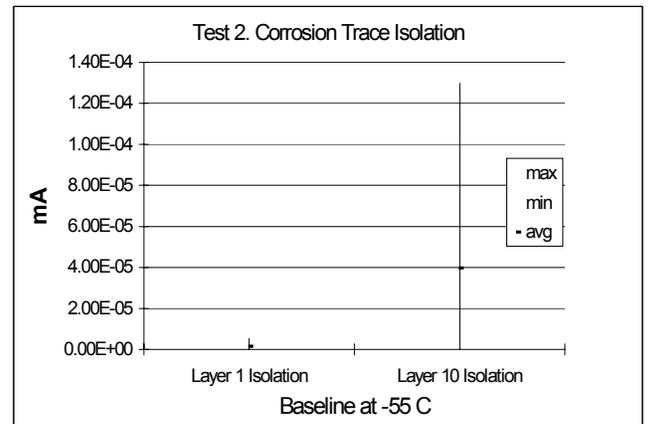
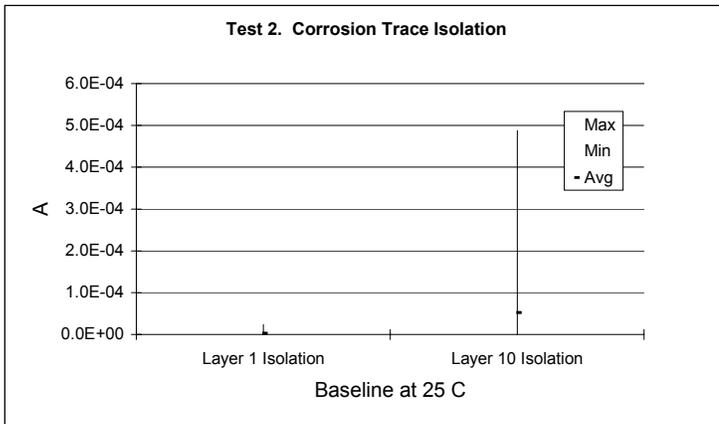
Iccq enabled per cube = 480mA max.

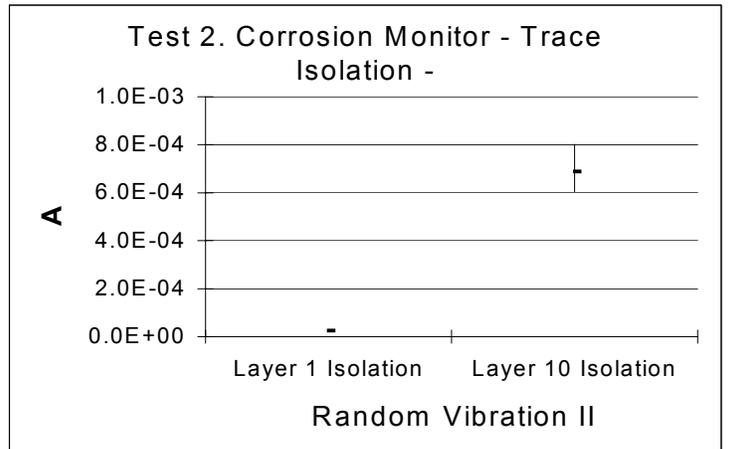
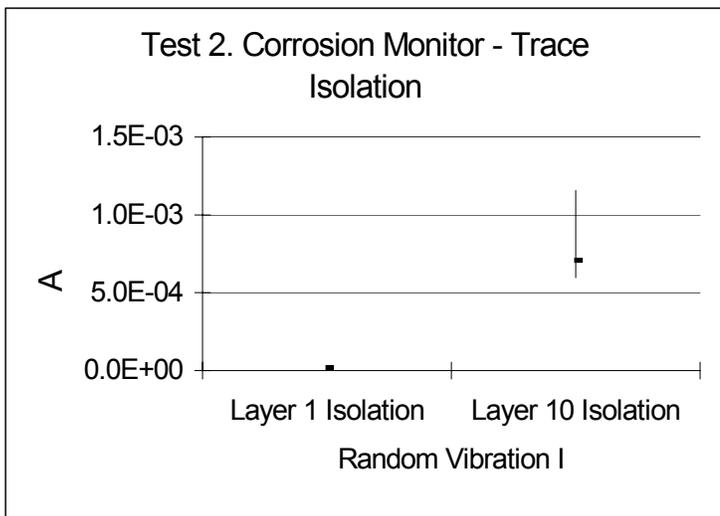
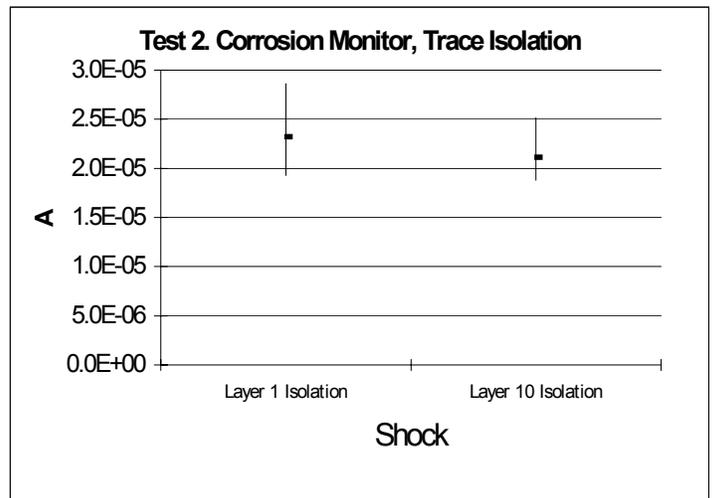
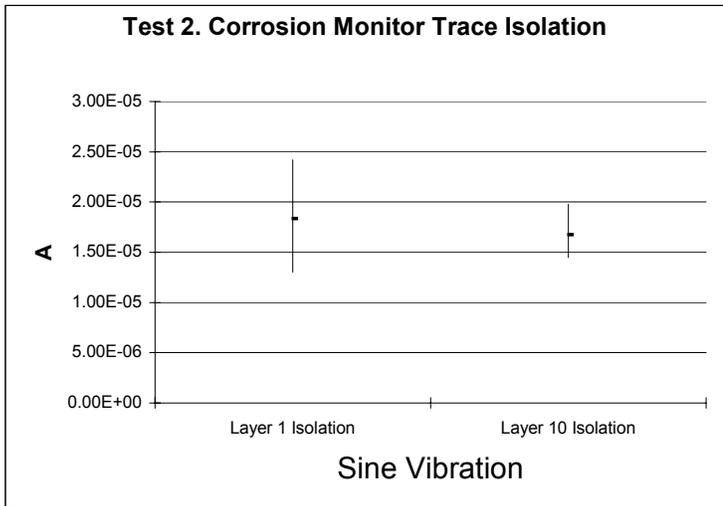
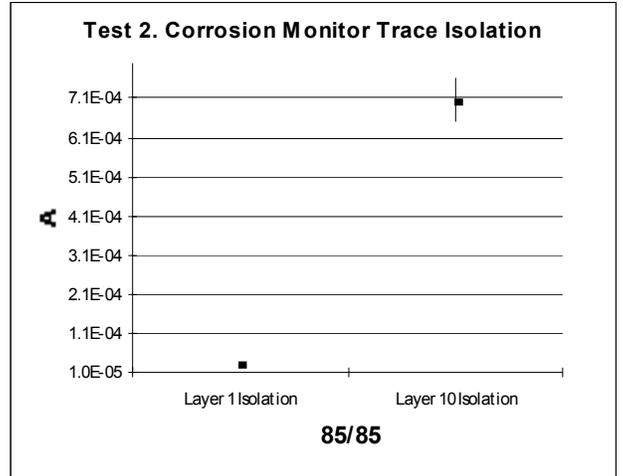
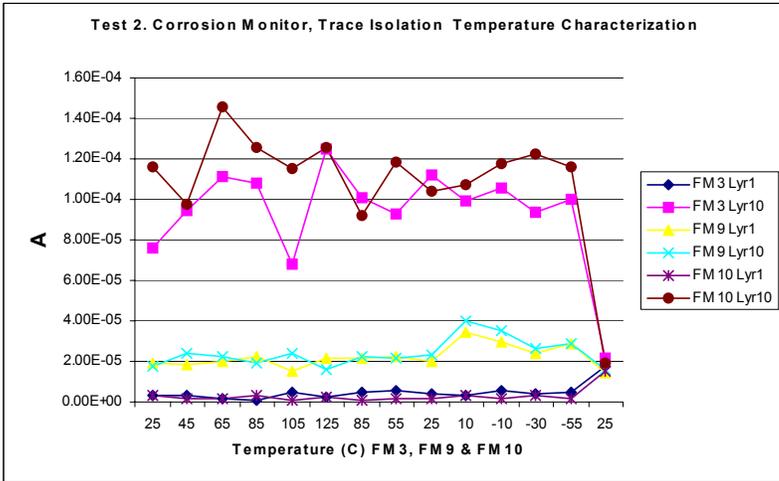


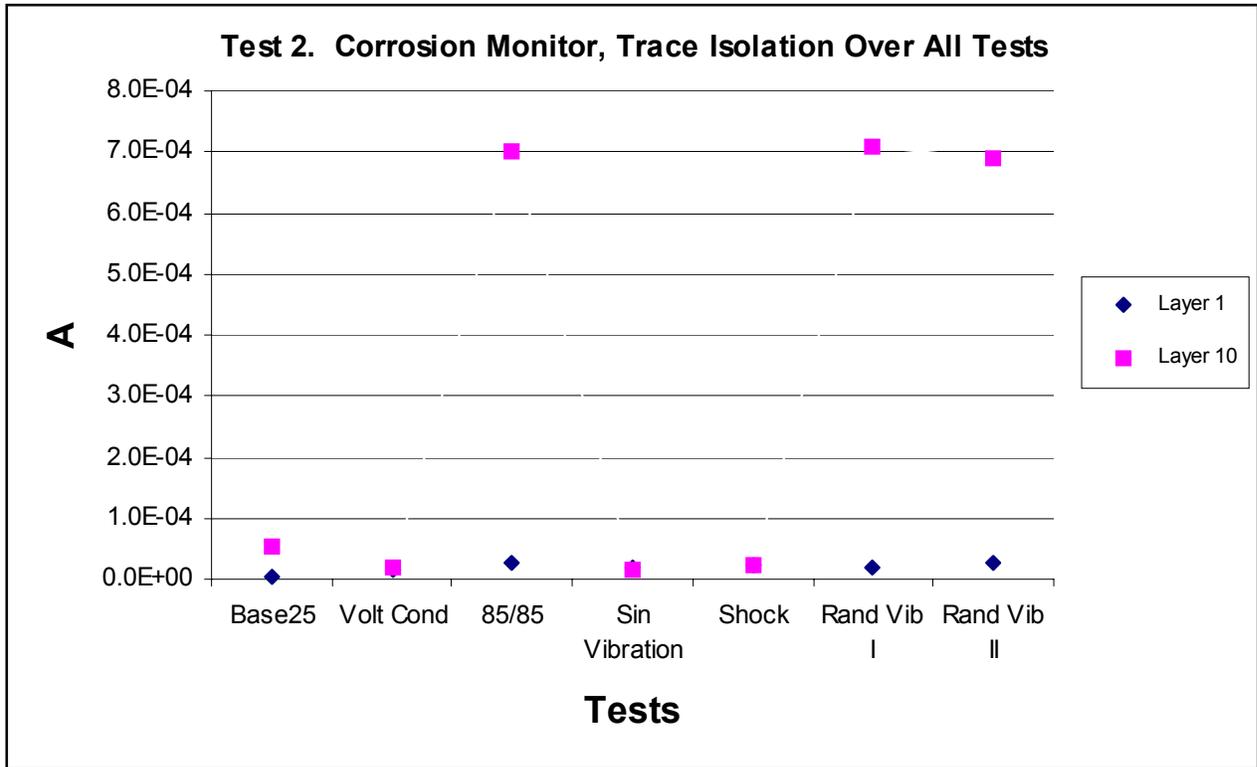
## 2.0 Corrosion Module Trace Isolation

The leakage current between the conductors of the corrosion module was expected to be < 1 mA. The values measured for the control sample (FM13) are shown in Table 2. All data shown in Table 2 is in Ohms.

Test	Layer 1	Layer 10
Baseline 25°C	2.4e-6	86.8e-6
Baseline 125°C	1.44e-6	114.8e-6
Baseline -55°C	0.96e-6	94.2e-6
Volt Cond.	11.0e-6	16.4e-6
Final 25°C	17.4e-6	374e-6



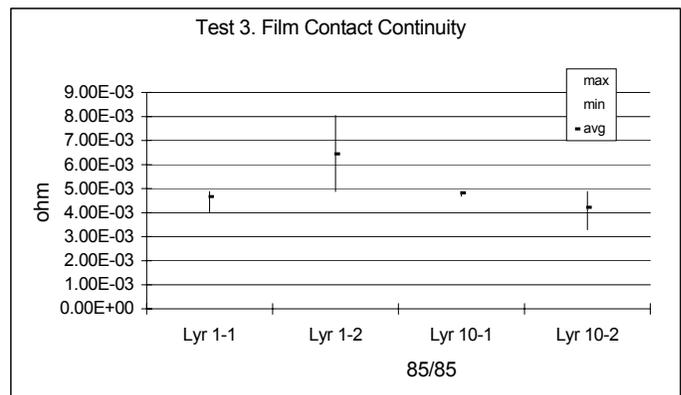
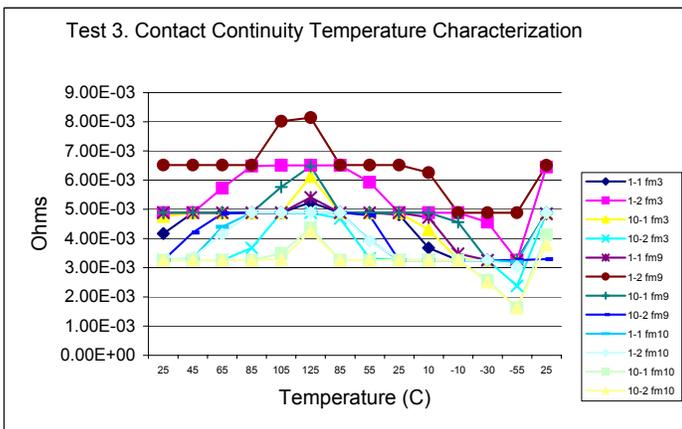
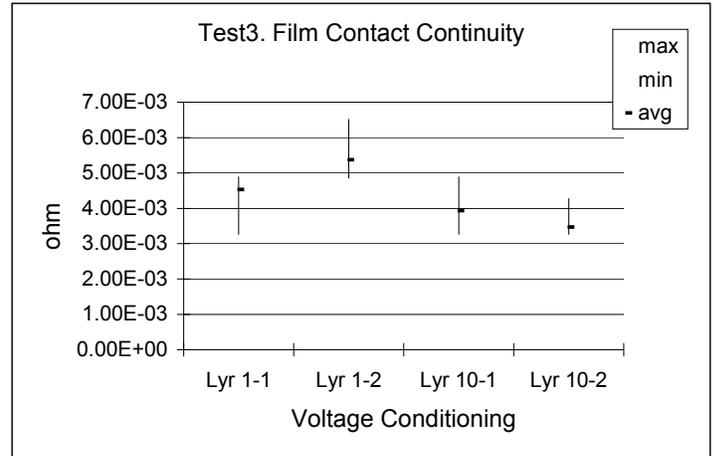
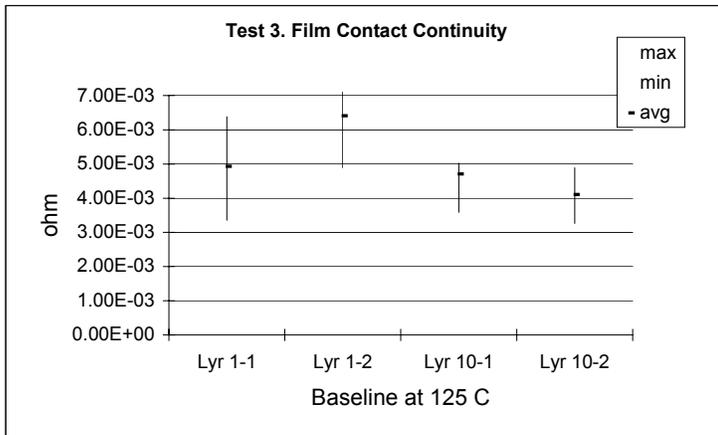
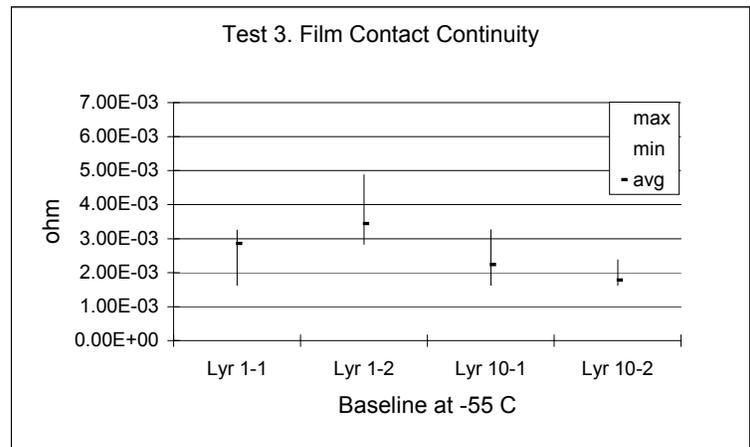
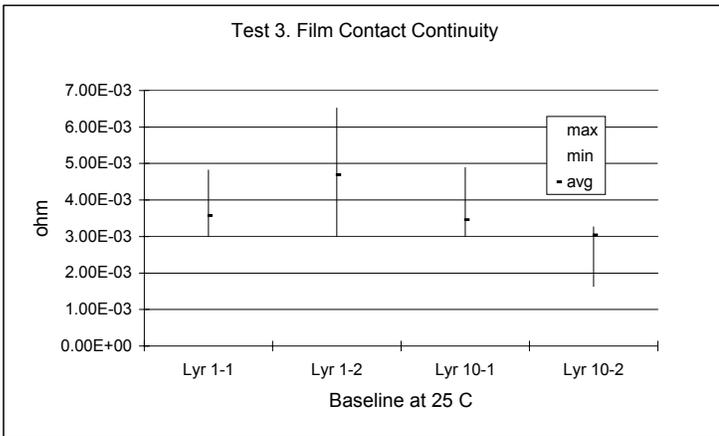


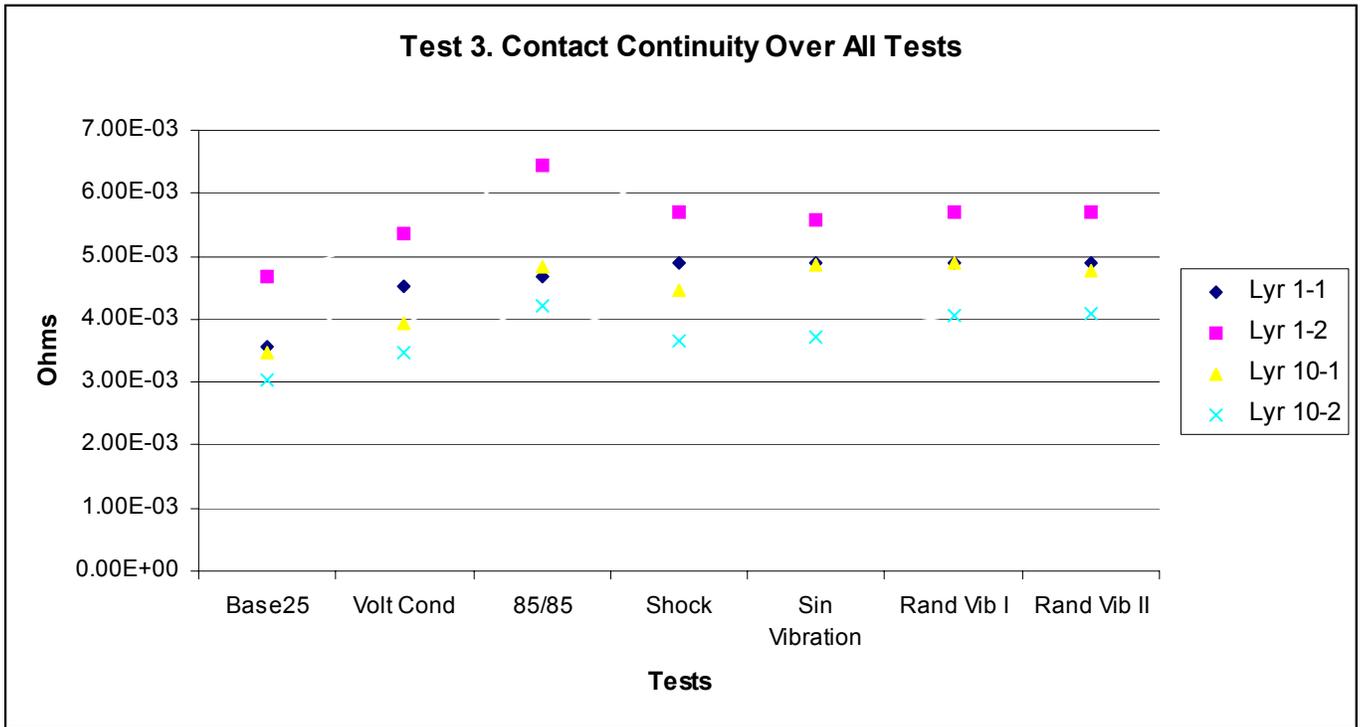
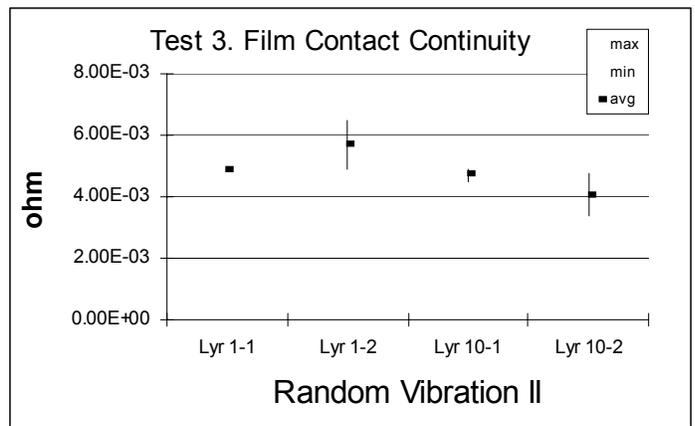
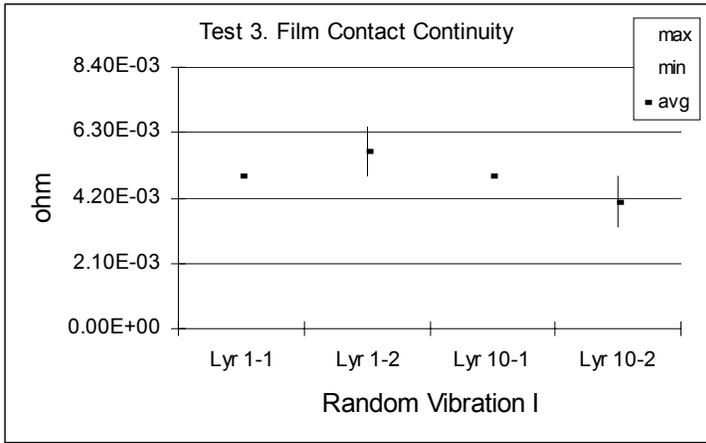
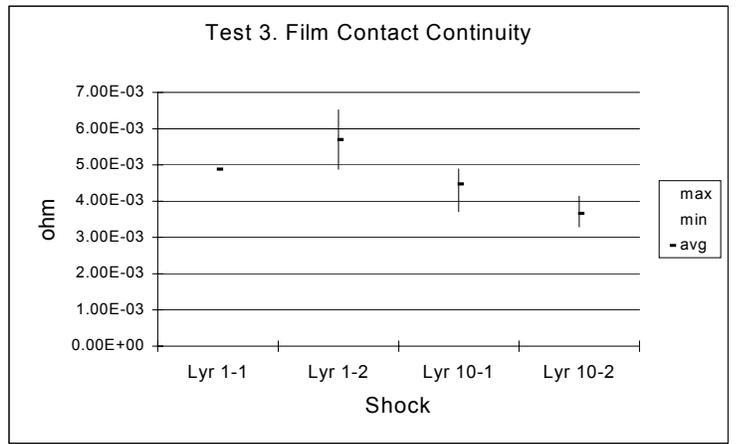
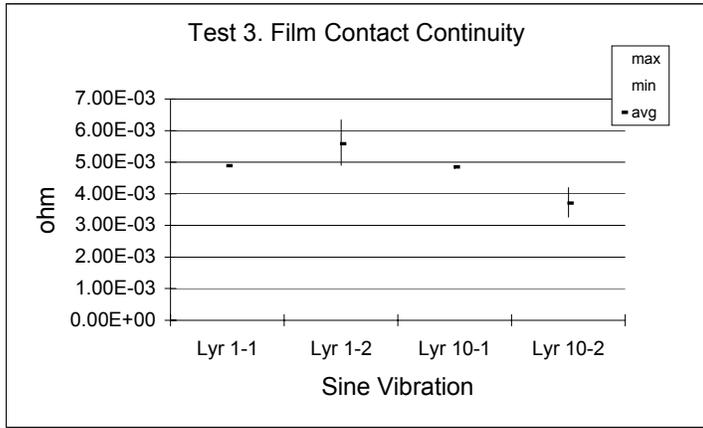


### 3.0 Contact Continuity

The resistance of tracks into the cube and along its outside are measured in Ohms. The expected value is less than 1 ohm, however the test is go/no go for continuity.

Test	Layer 1-1	Layer 1-2	Layer 10-1	Layer 10-2
Baseline 25°C	3.26E-03	4.89E-03	3.26E-03	3.26E-03
Baseline 125°C	4.88E-03	6.94E-03	4.89E-03	4.82E-03
Baseline -55°C	3.00E-03	3.29E-03	2.51E-03	1.76E-03
Volt Cond.	4.54E-03	5.37E-03	3.93E-03	3.47E-03
Final 25°C	4.88E-03	6.51E-03	4.88E-03	4.62E-03



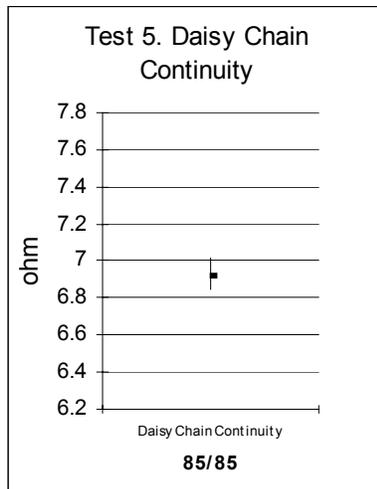
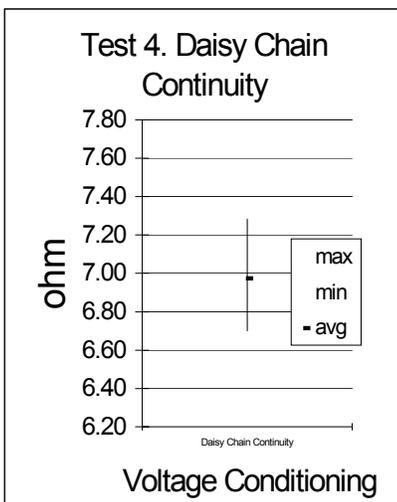
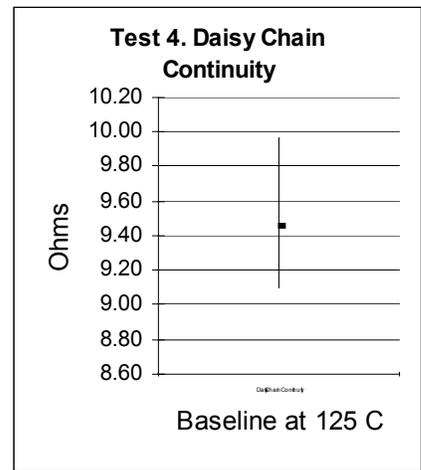
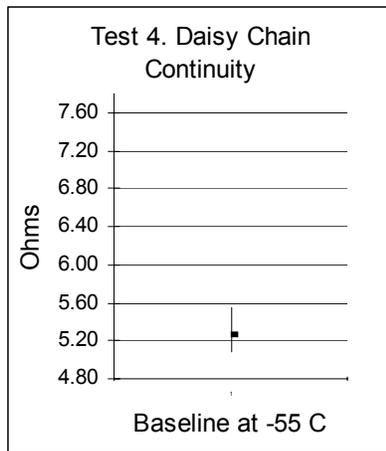
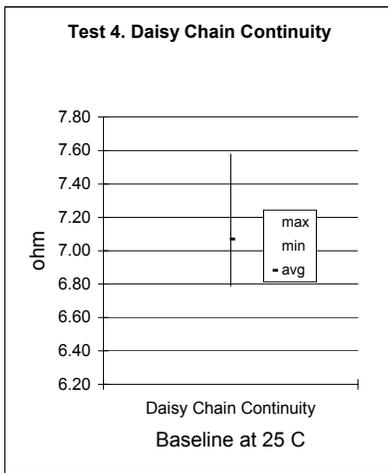


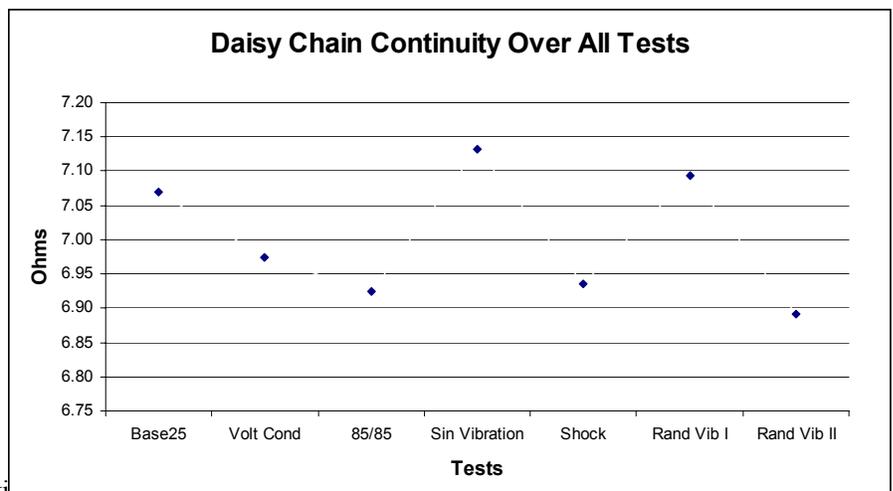
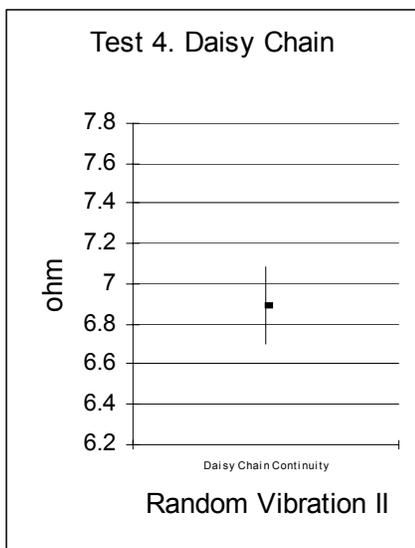
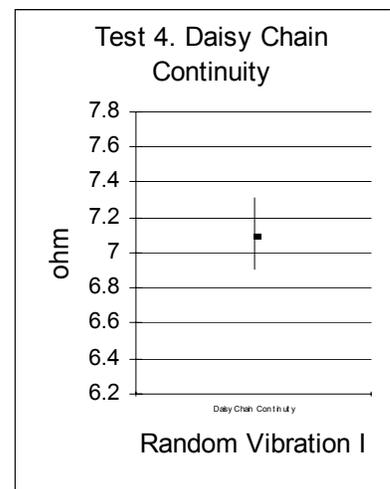
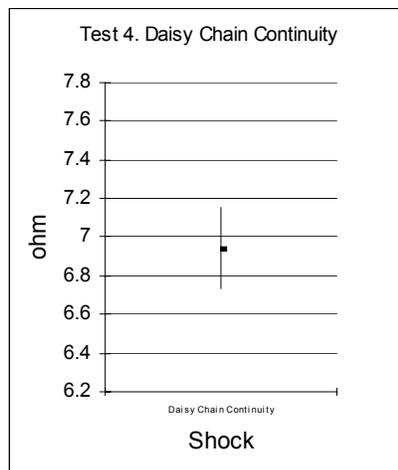
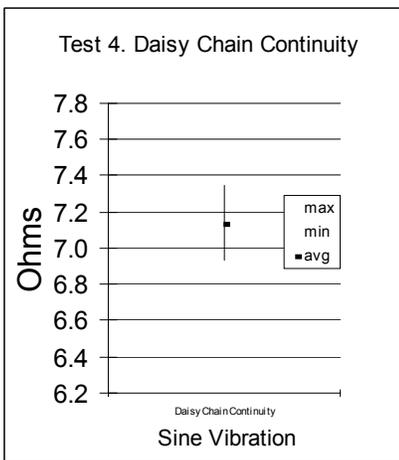
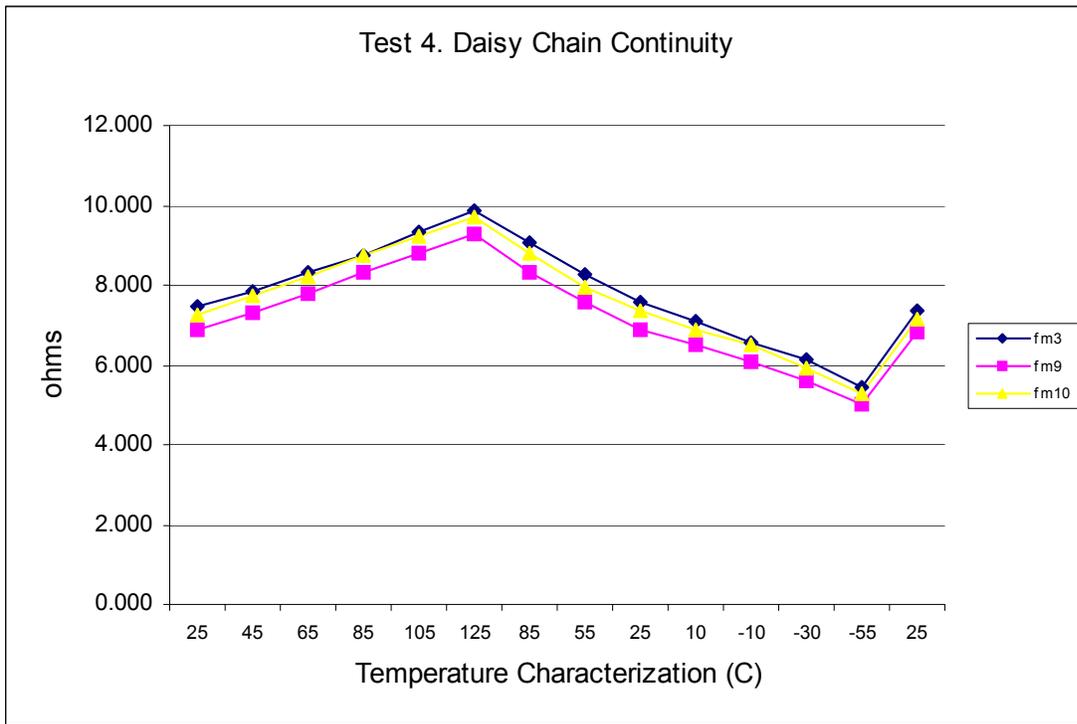
#### 4.0 Daisy Chain Continuity

A Daisy Chain of 200 wire bonds was measured for continuity. The baseline measurements indicate the resistance level associated with continuity.

Table 1. Control Sample Values

Test	Continuity Resistance ( $\Omega$ )
Baseline 25°C	7.2
Baseline 125°C	9.6
Baseline -55°C	5.3
Volt Cond. 25°C	7.2
Final 25°C	7.1



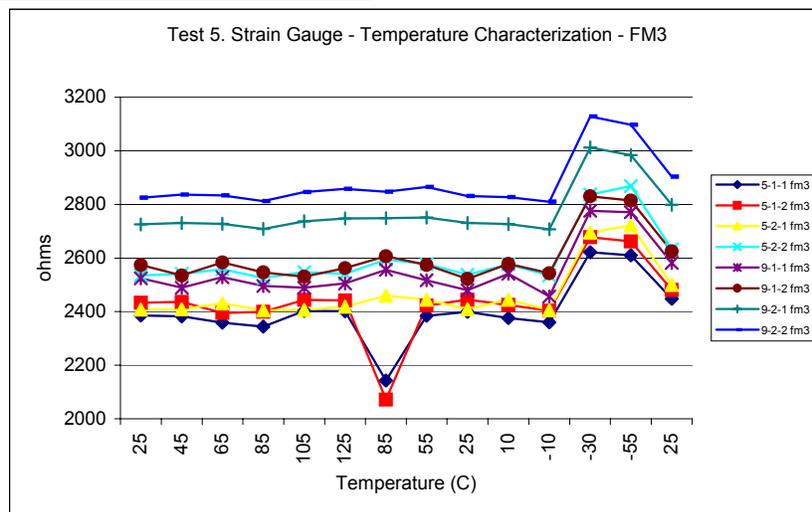
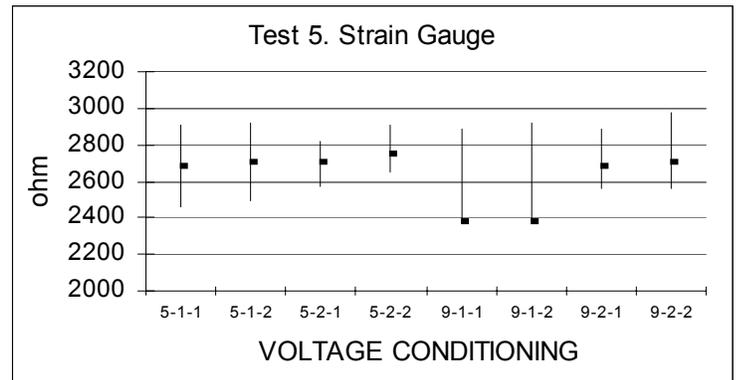
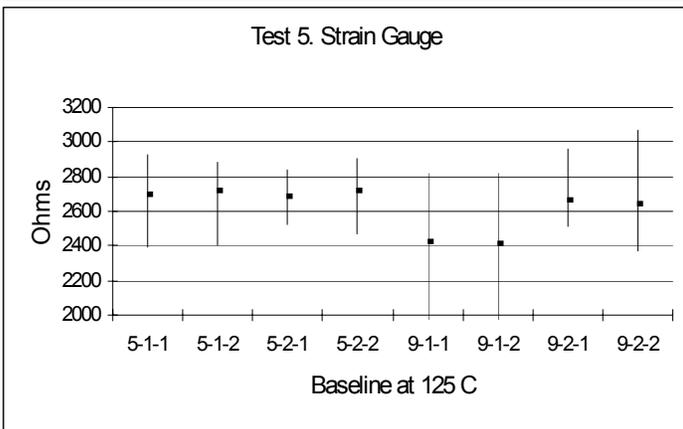
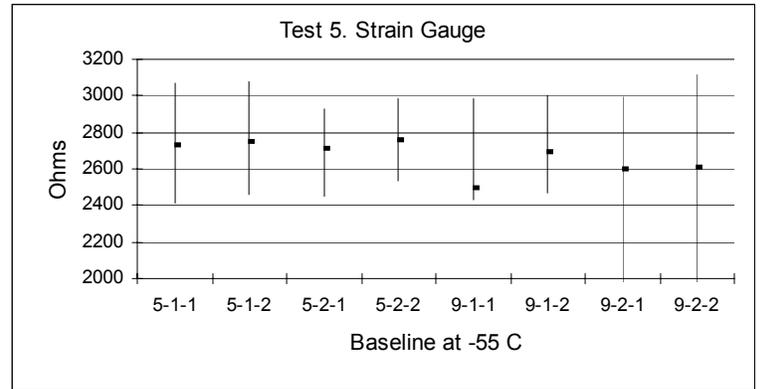
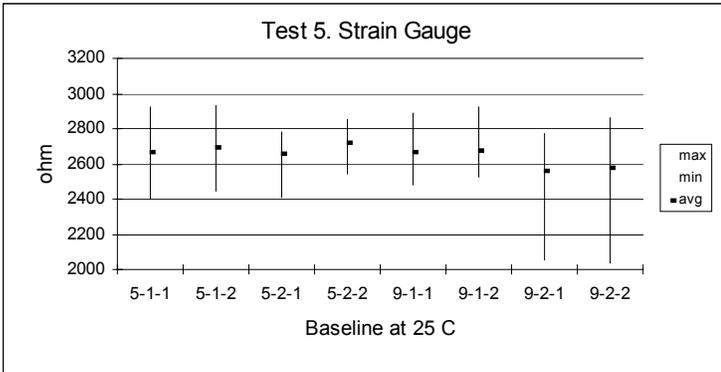


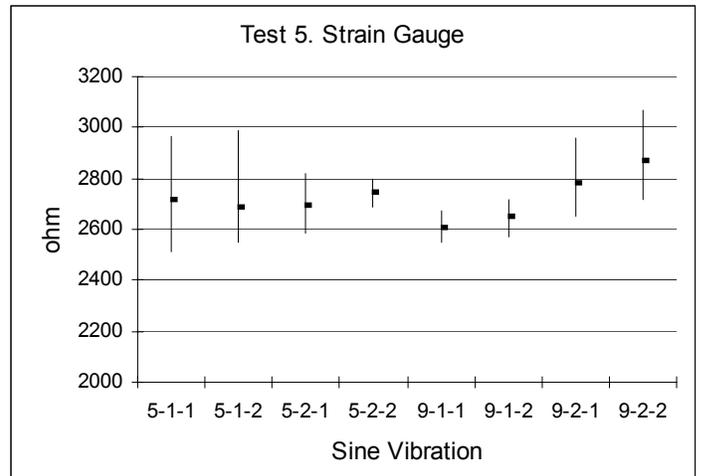
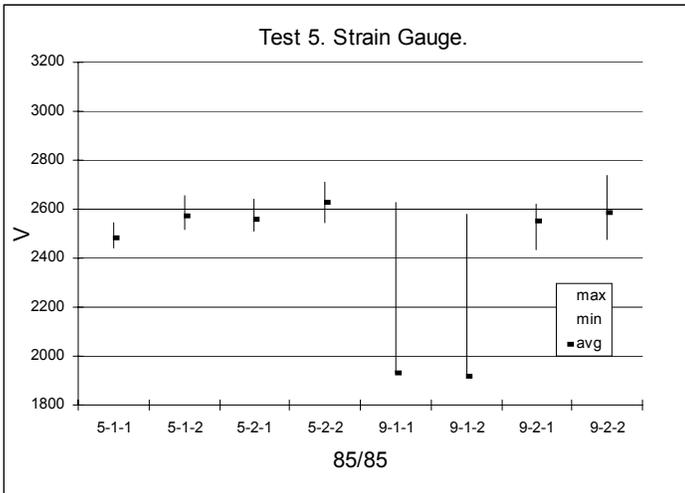
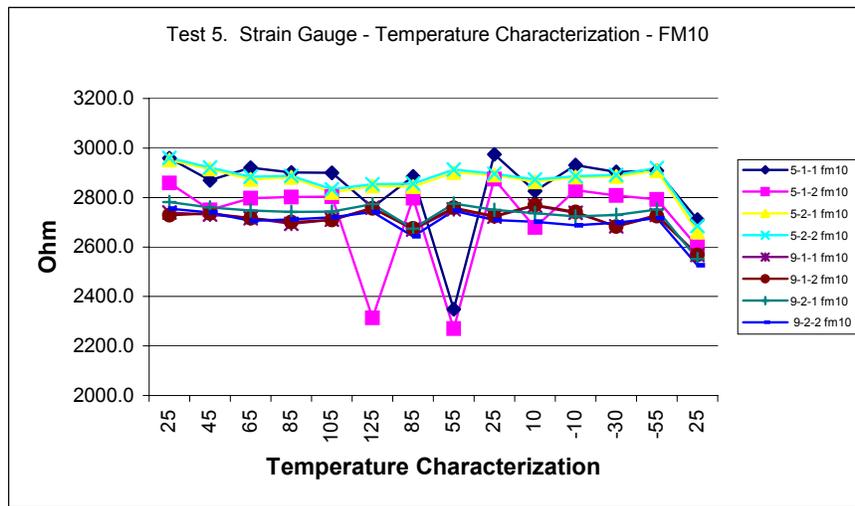
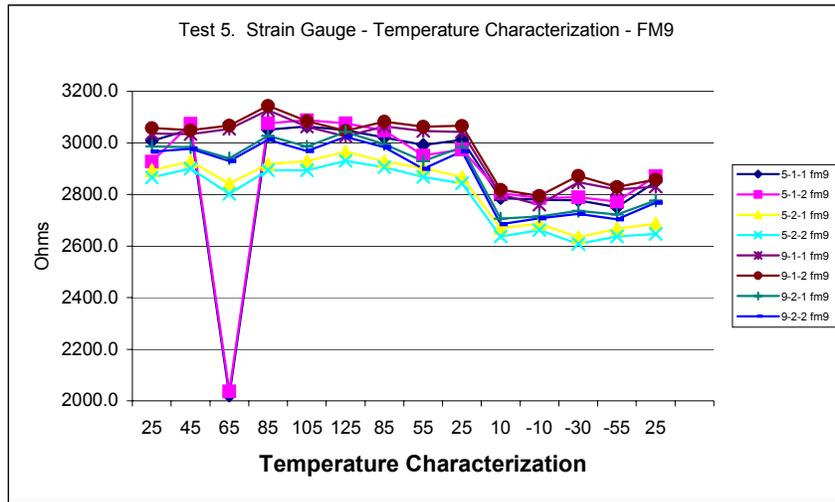
## 5.0 Strain Gauge

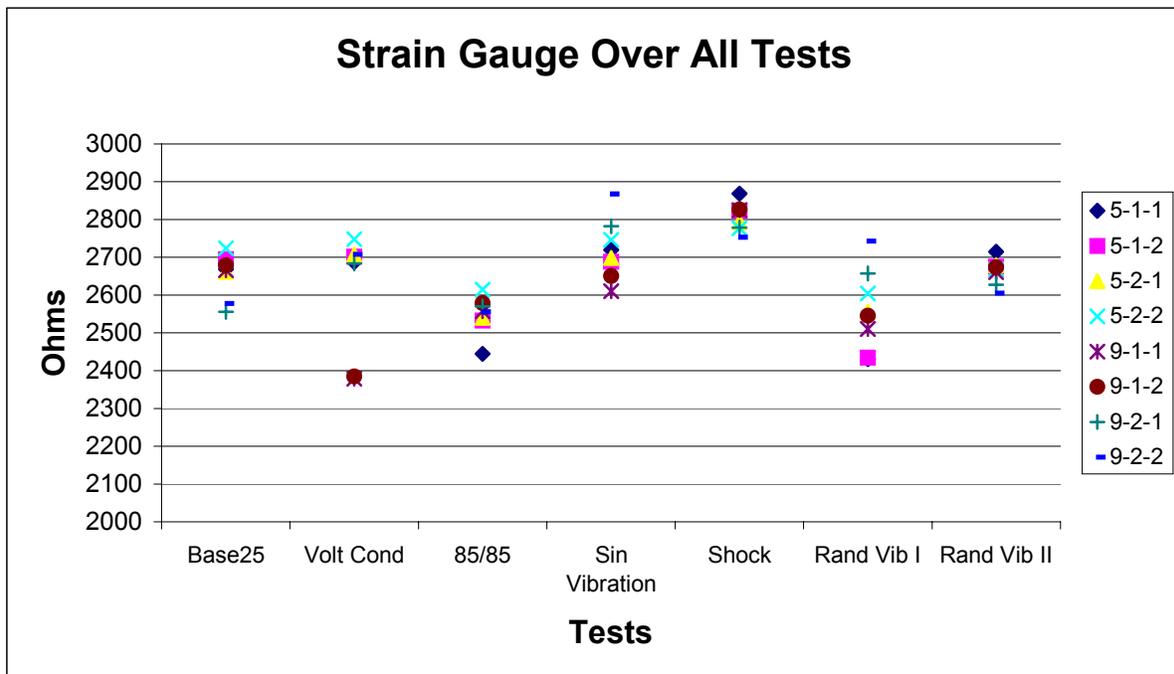
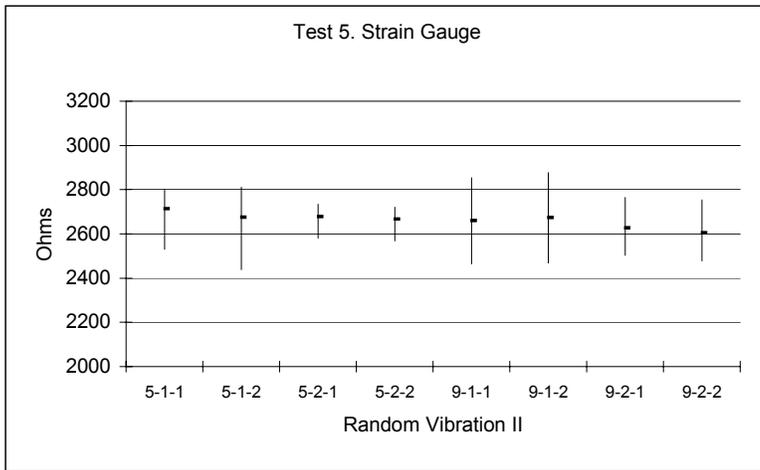
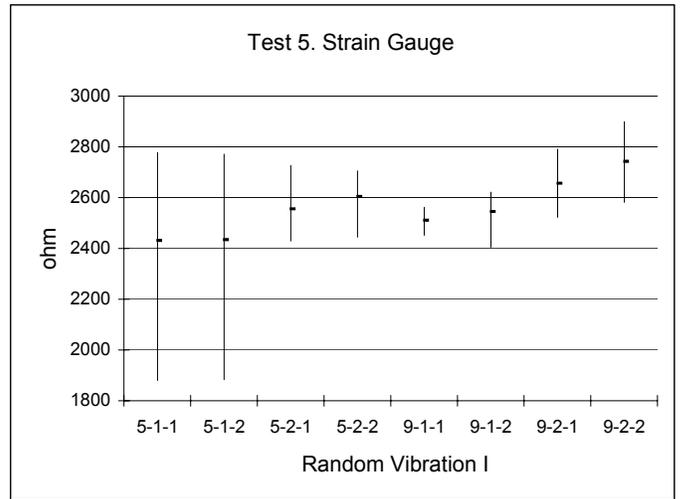
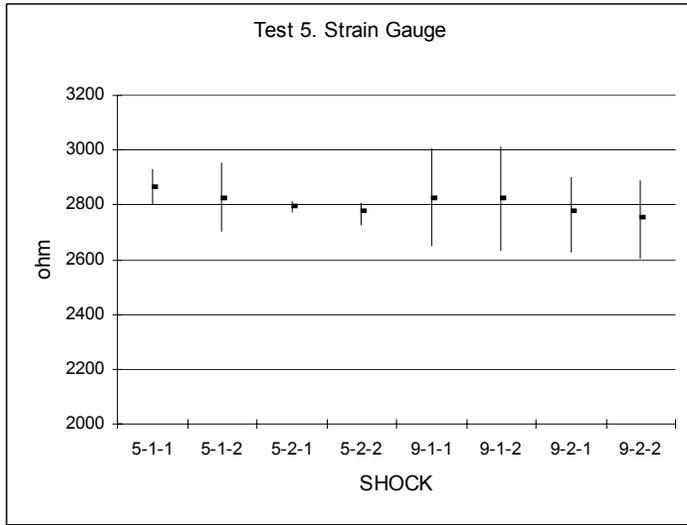
DC Resistance was measured for two strain gauge devices on each die (die on two layers, 5 and 9). The expected values were between 2565 and 2835 Ohms.

Table 1. Control Sample Values (Ohms)

Test	5-1-1	5-1-2	5-2-1	5-2-2	9-1-1	9-1-2	9-2-1	9-2-2
Baseline 25°C	2768	2797	2764	2858	2846	2833	2677	2635
Baseline 125°C	2783	2810	2805	2904	2763	2756	2619	2577
Baseline -55°C	2767	2785	2751	2843	2763	2761	2641	2597
Volt Cond. 25°C	2830	2849	2816	2906	2812	2802	2655	2629
Final 25°C	2661	2568	2650	2664	2727	2660	2309	2268





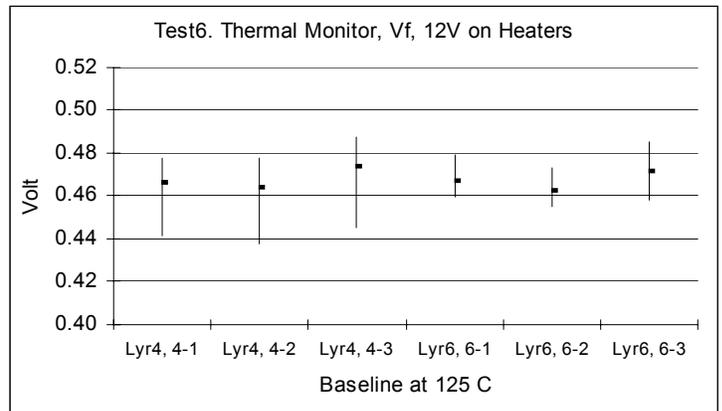
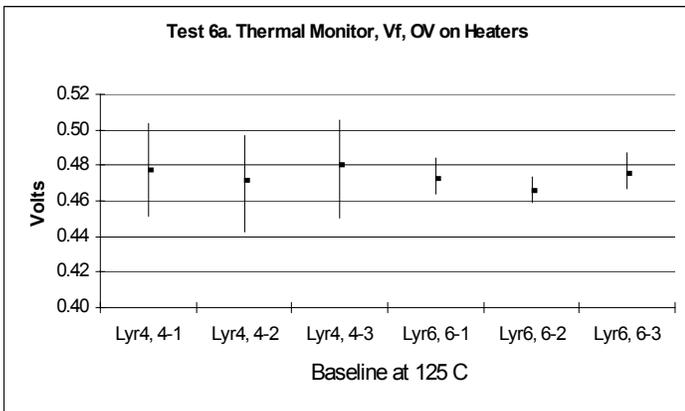
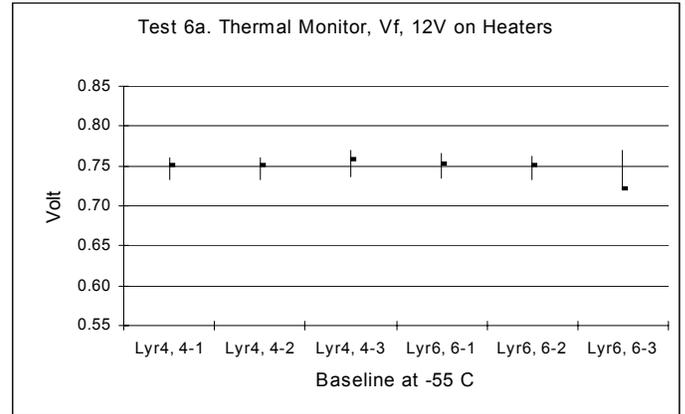
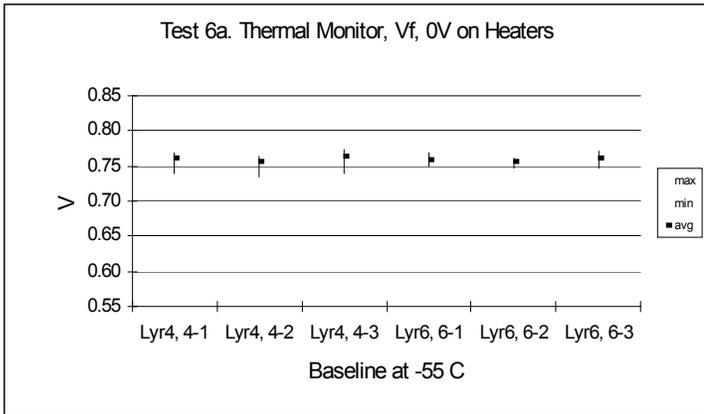
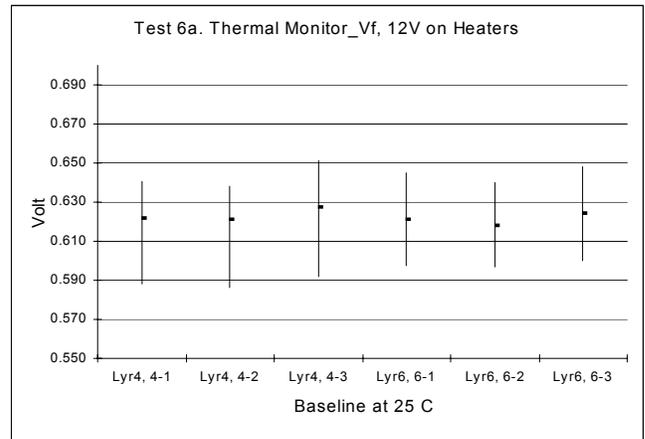
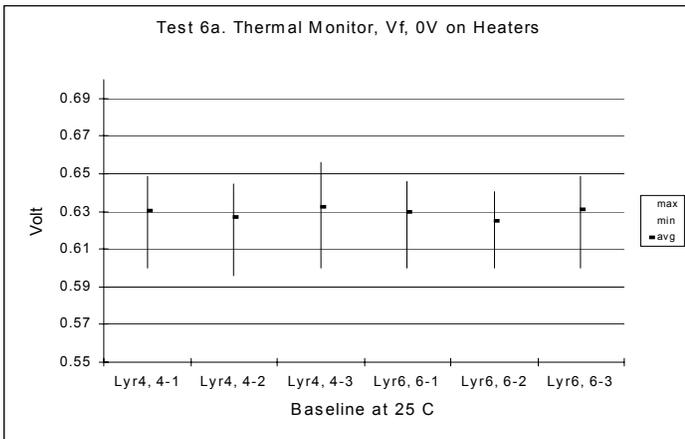


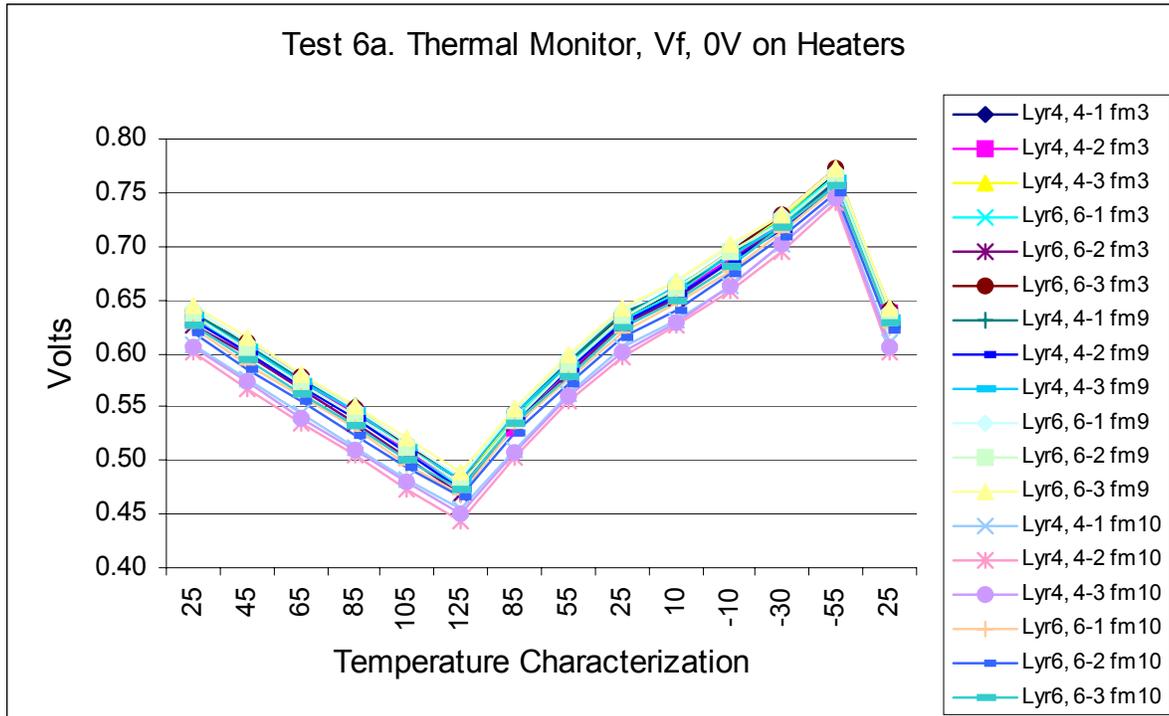
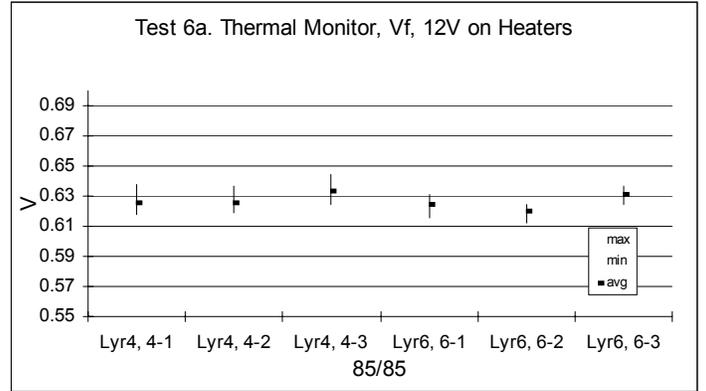
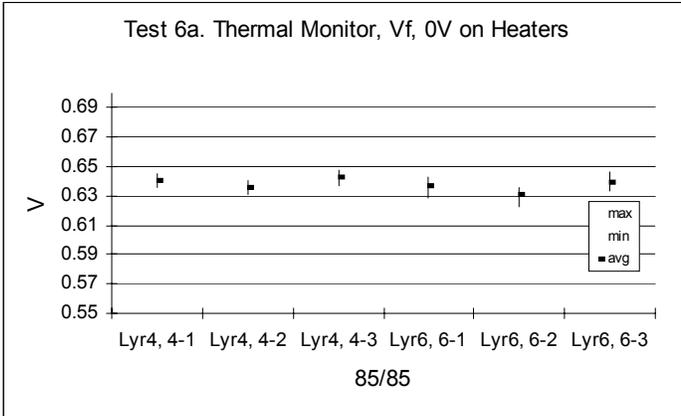
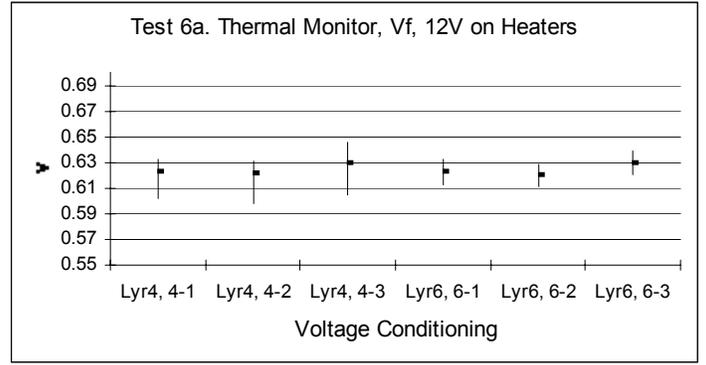
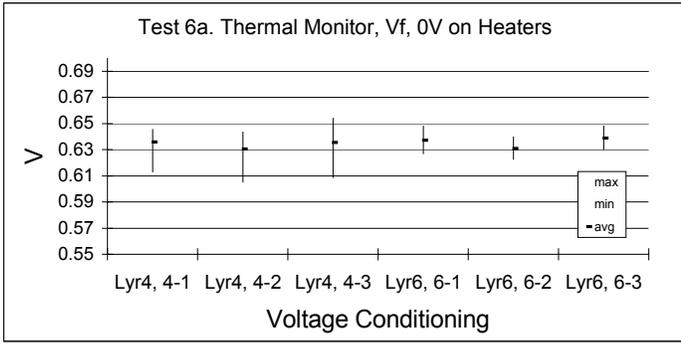
### 6.a. Thermal Monitor – Forward Voltage Drop

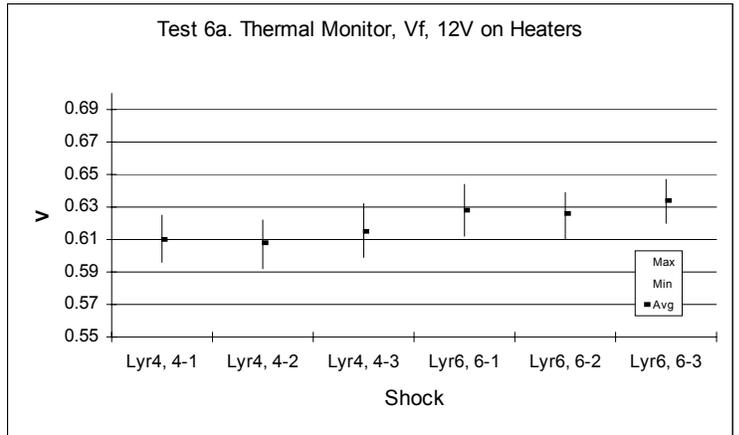
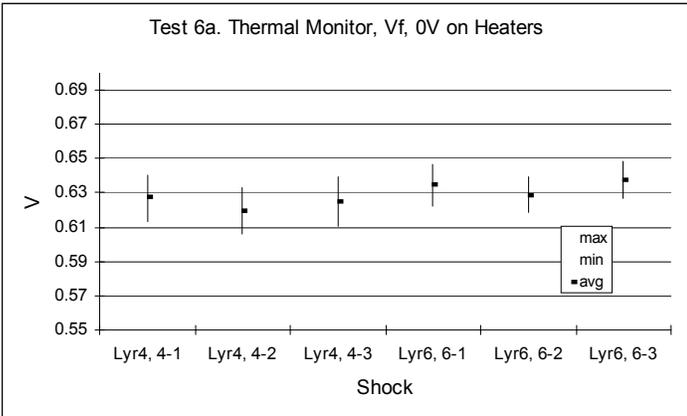
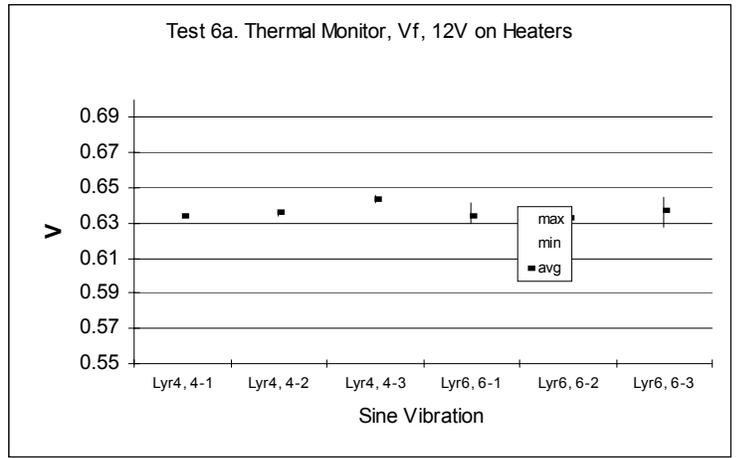
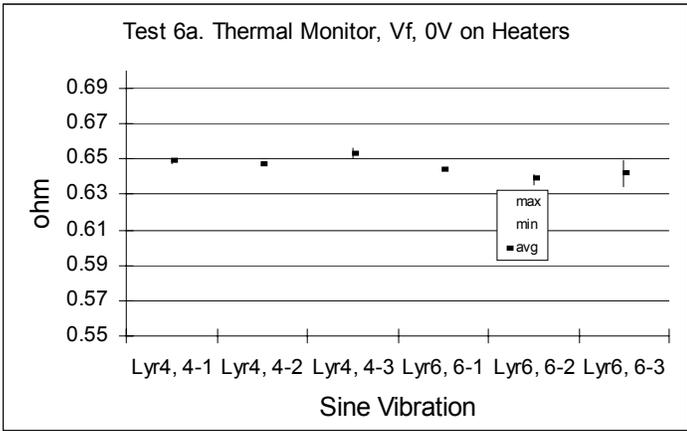
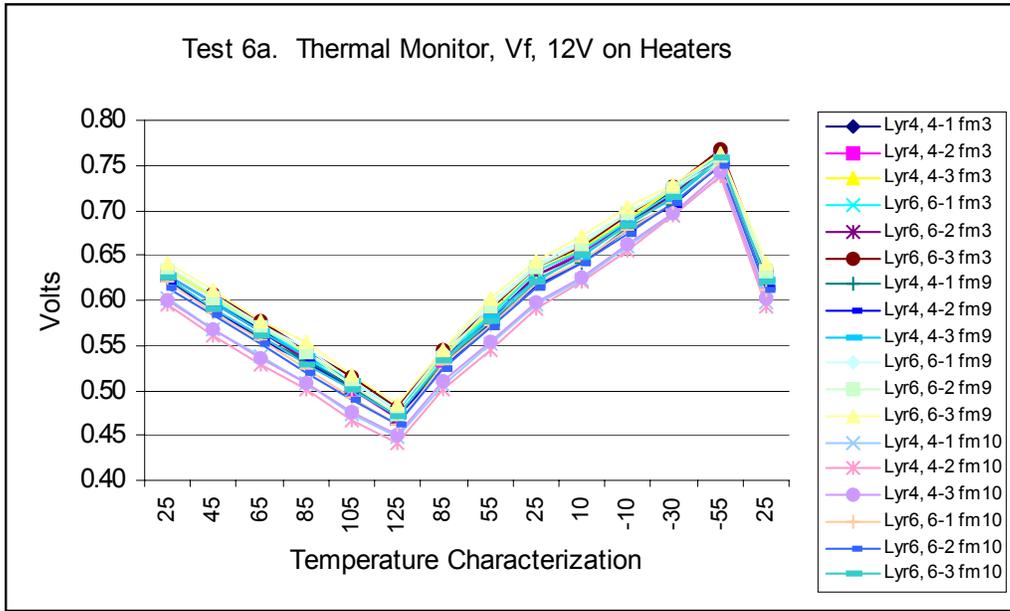
Forward voltage drop was measured for three diodes on the test chip while four heater resistors were both biased (12V) and unbiased (0V). Layer 4 contained a heat sink under it. The expected values were between 0.5V and 1V.

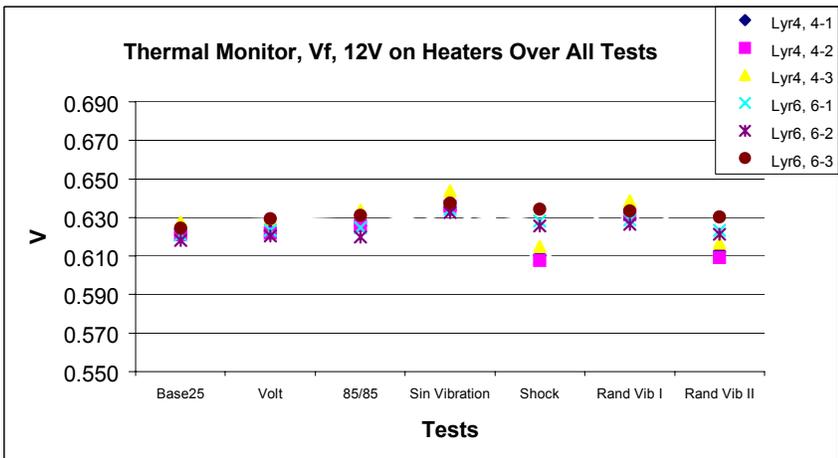
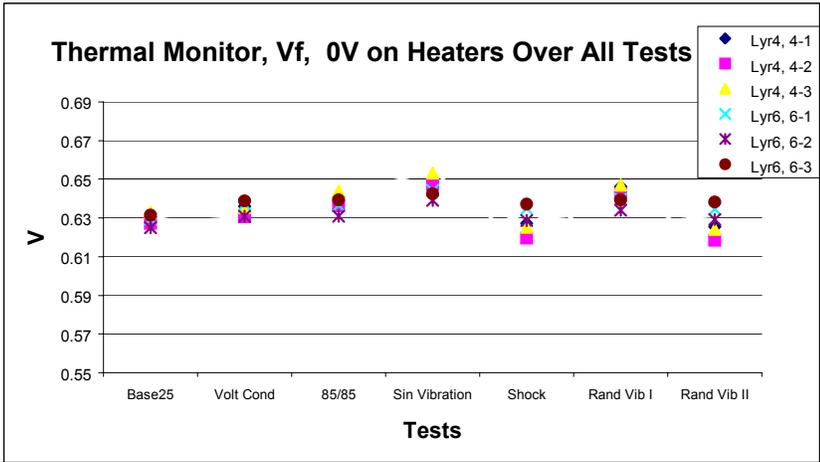
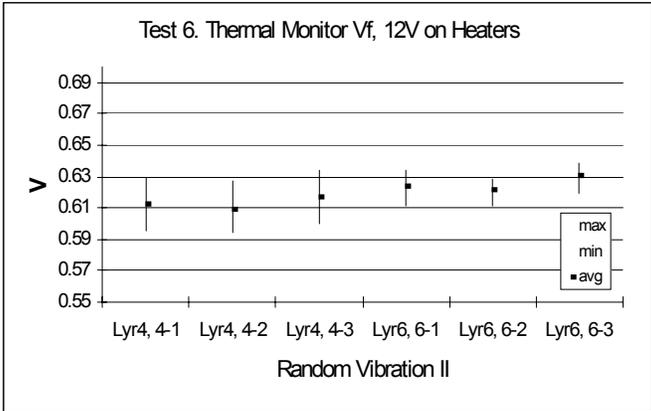
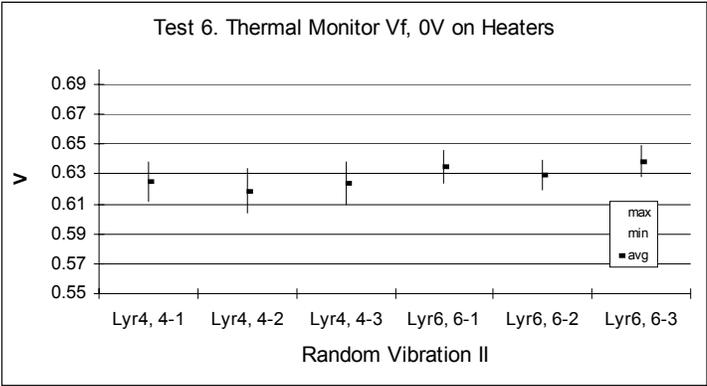
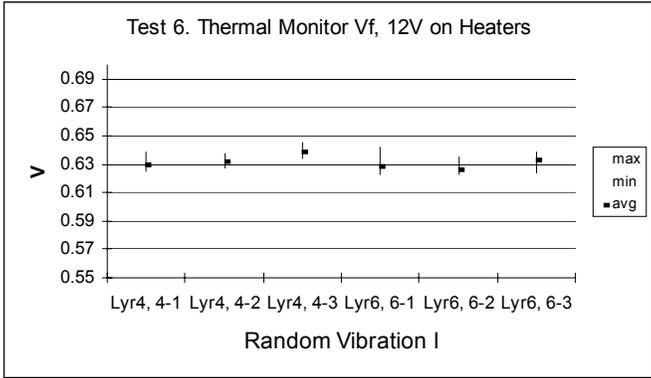
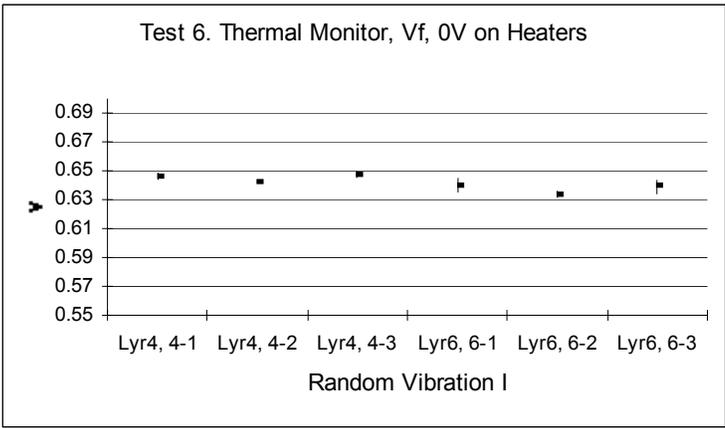
Table 1. Control Sample Values (V)

Test	4-1	4-2	4-3	6-1	6-2	6-3	4-1	4-2	4-3	6-1	6-2	6-3
	0 V on Heaters						12V on Heaters					
Baseline 25°C	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6
Baseline 125°C	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5
Baseline -55°C	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8
Volt Cond. 25°C	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6
Final 25°C	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6







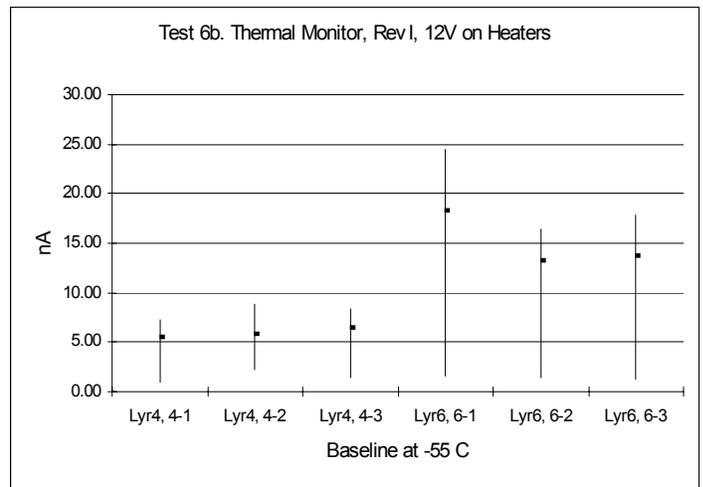
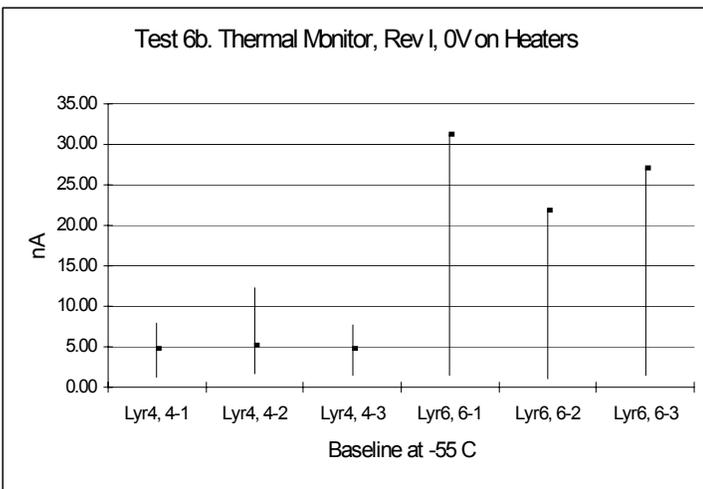
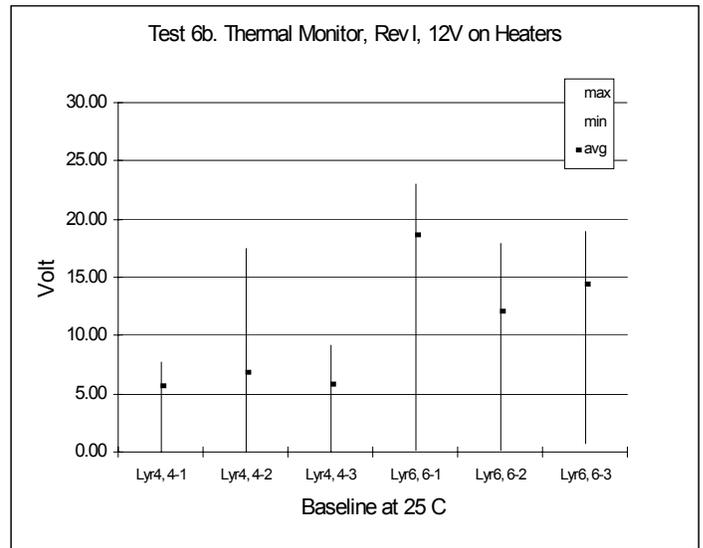
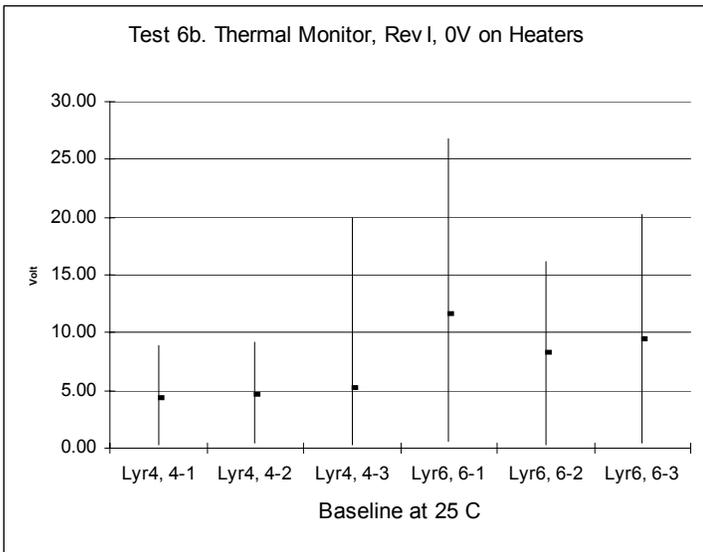


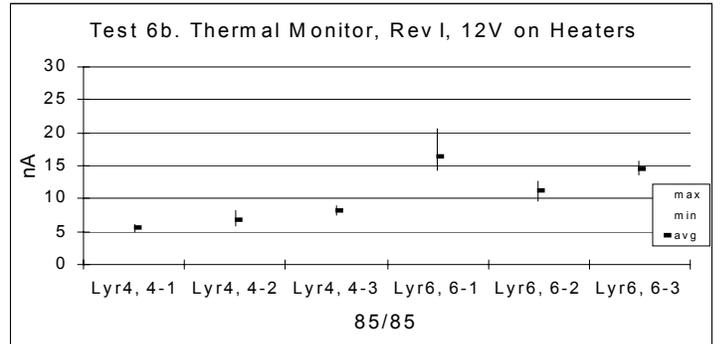
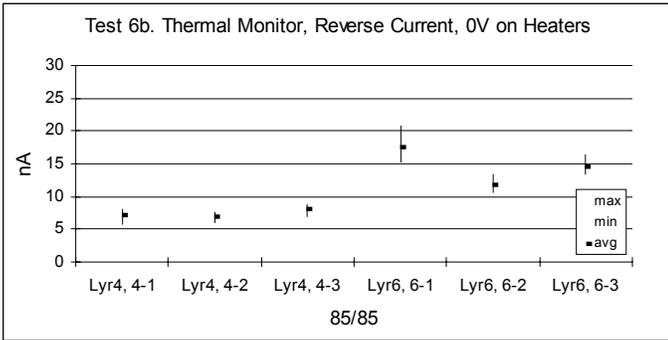
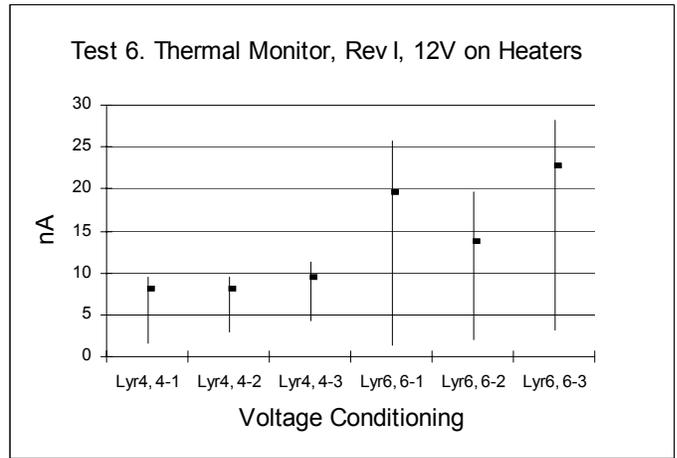
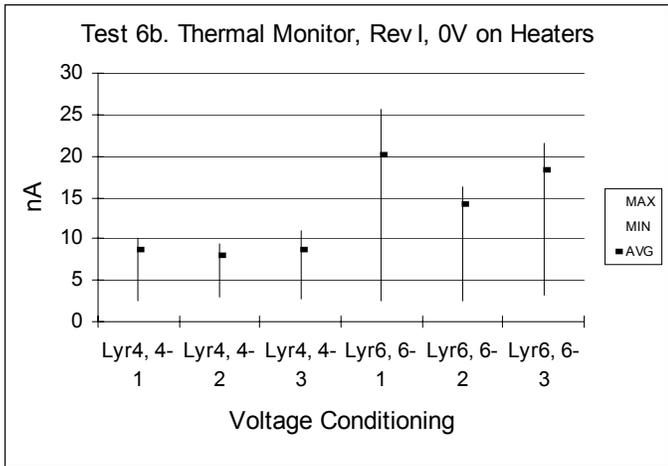
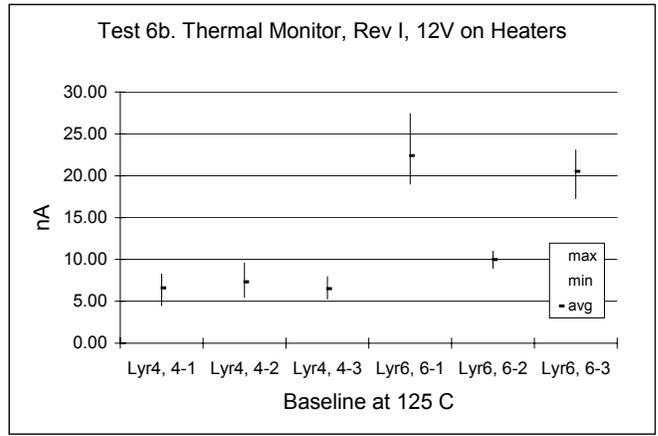
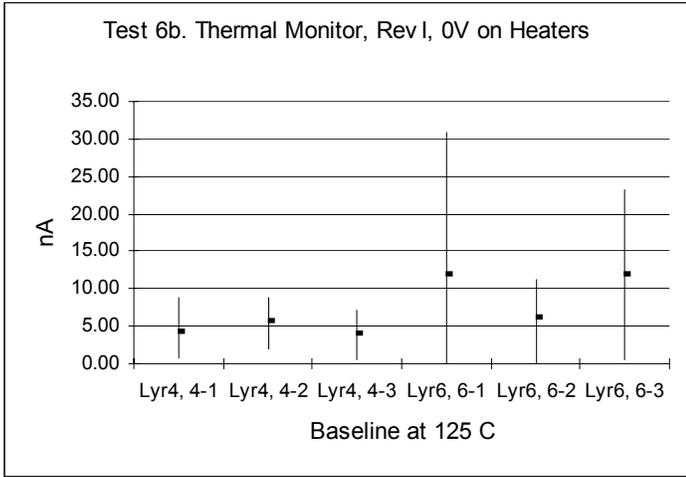
6.b. Thermal Monitor – Reverse Leakage Current

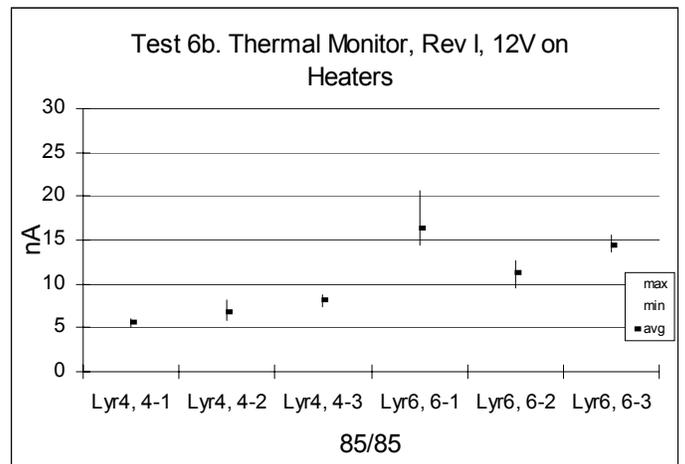
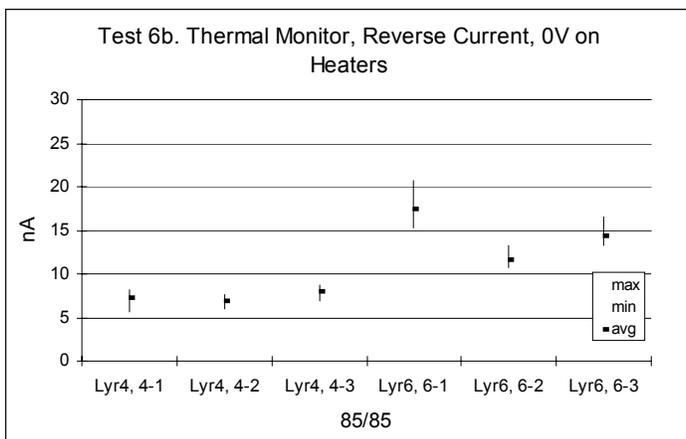
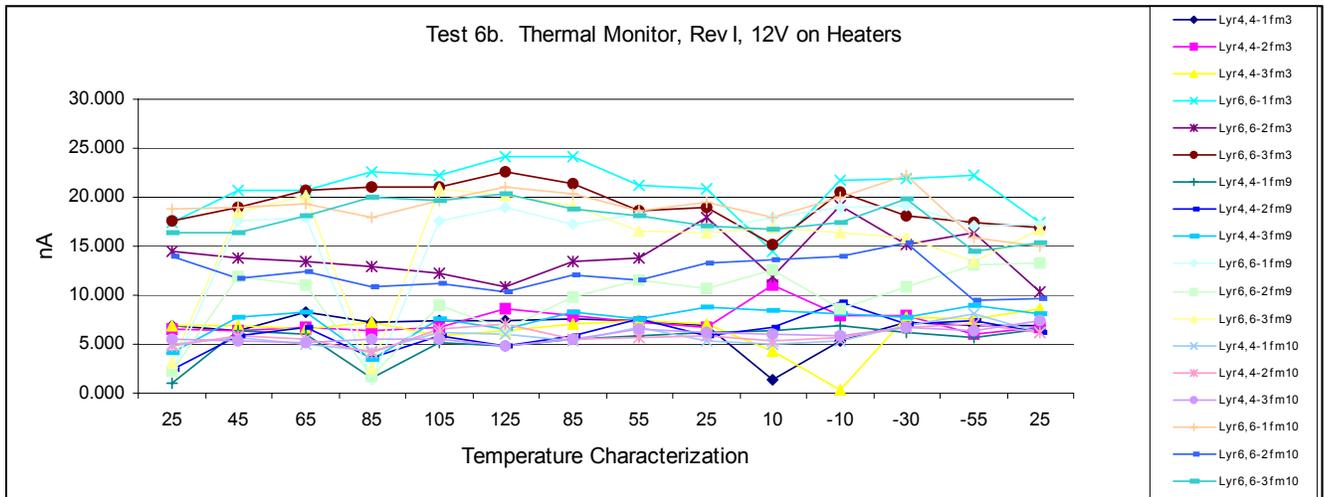
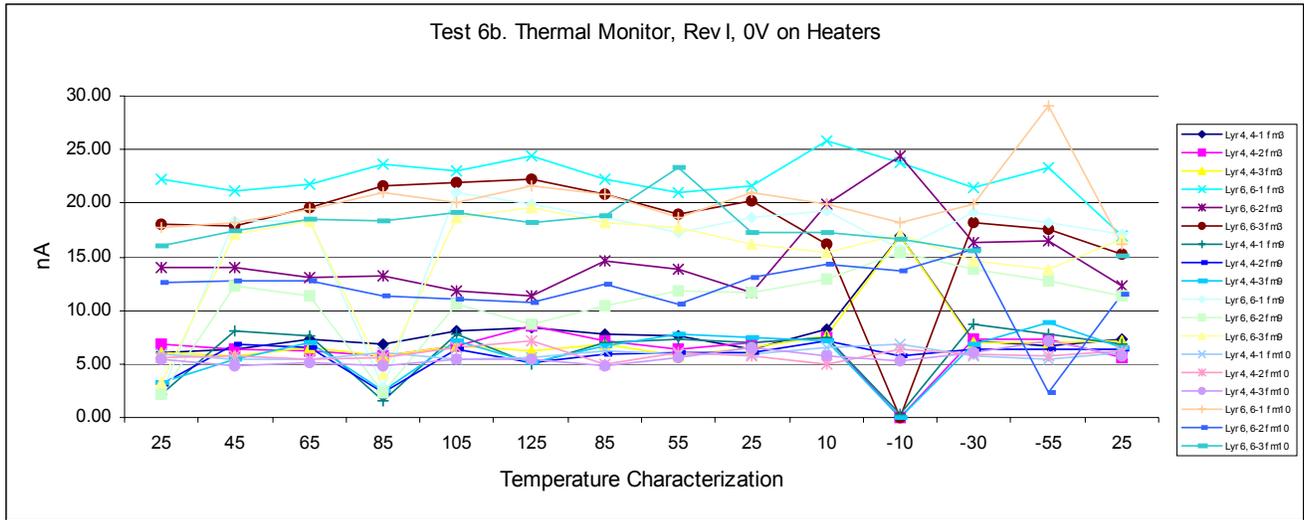
Reverse leakage current was measured for three diodes on the test chip while four heater resistors were both biased (12V) and unbiased (0V). Layer 4 contained a heat sink under it. The expected values were less than 100 nA.

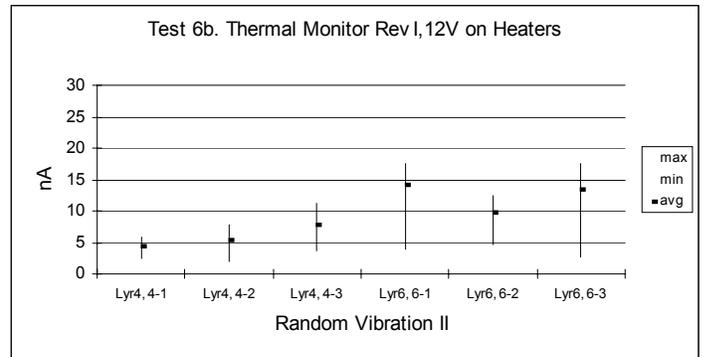
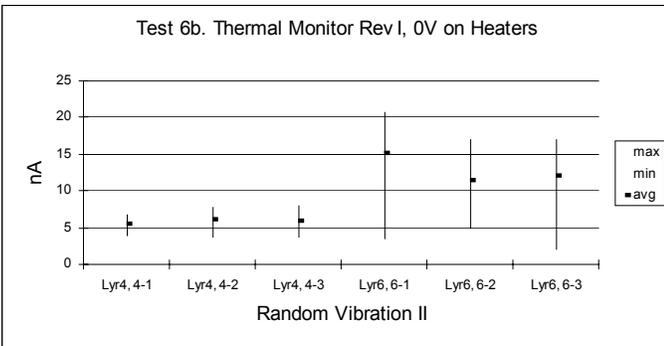
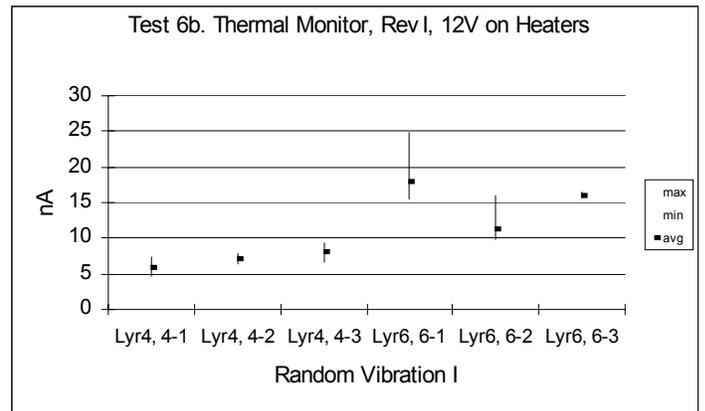
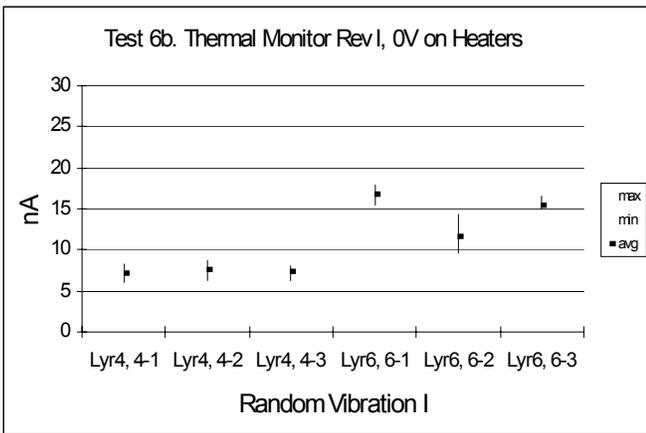
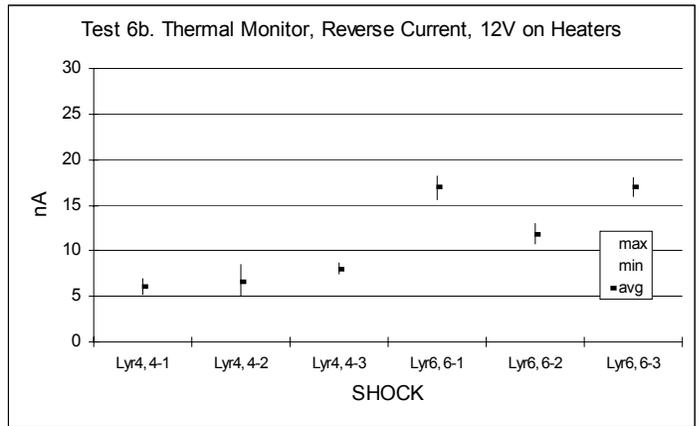
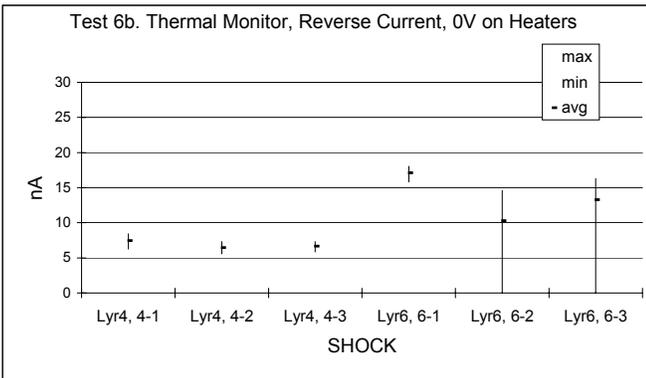
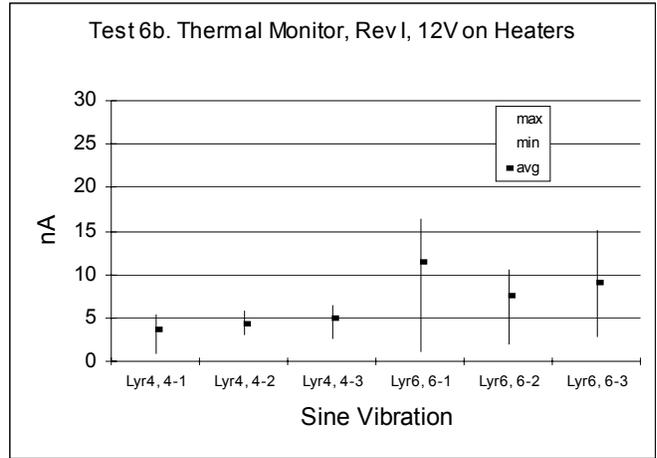
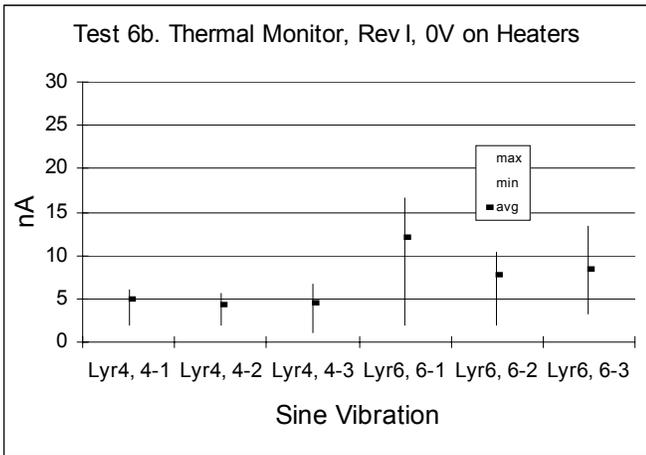
Table 1. Control Sample Values (nA)

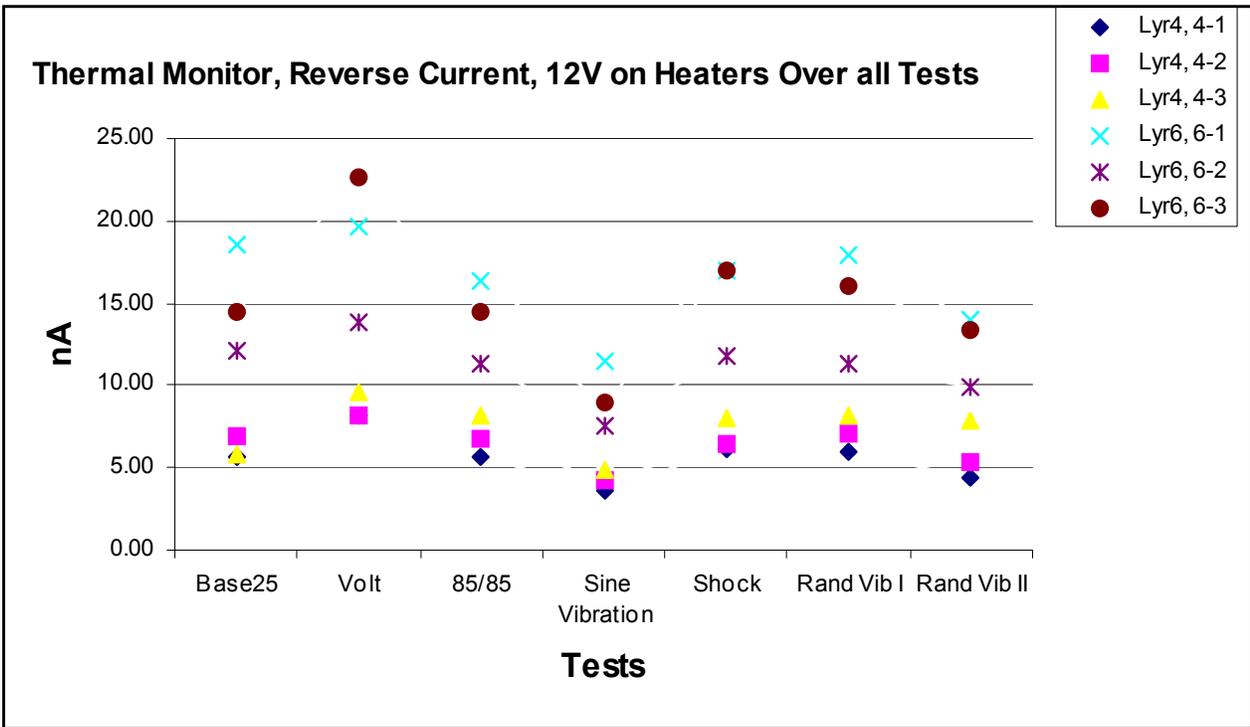
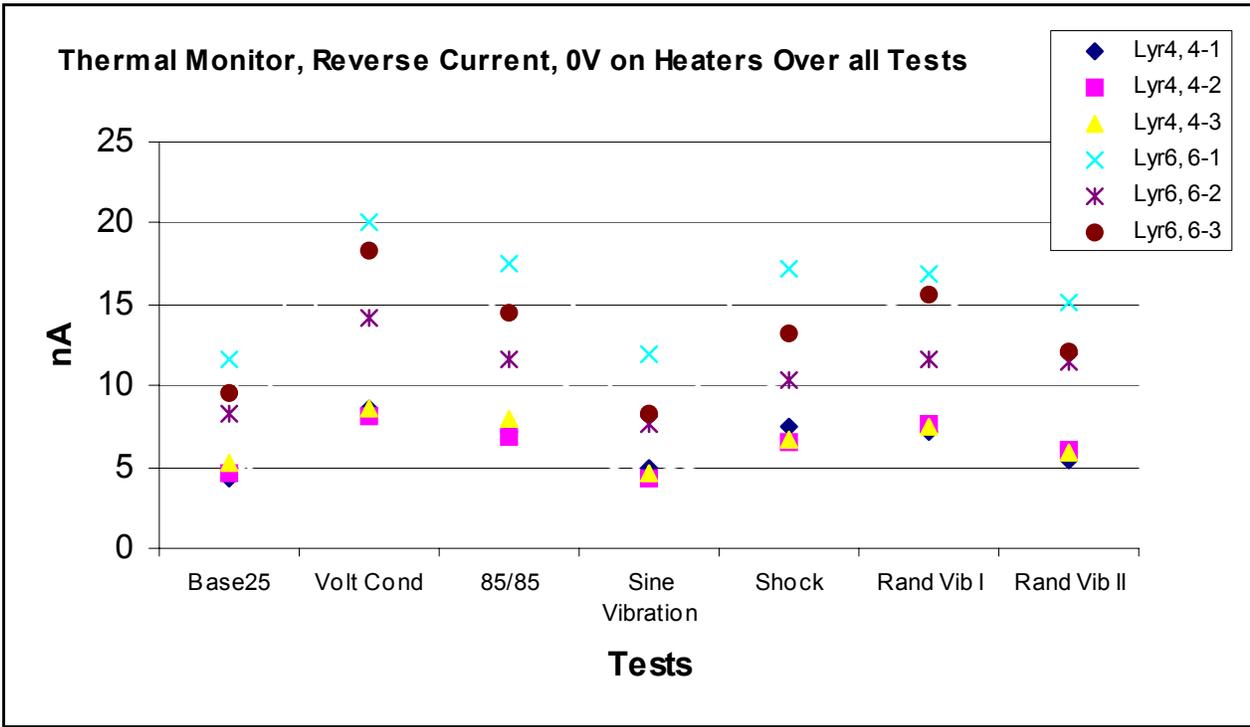
Test	4-1	4-2	4-3	6-1	6-2	6-3	4-1	4-2	4-3	6-1	6-2	6-3
	0 V on Heaters						12V on Heaters					
Baseline 25°C	6.3	6.7	6.1	17.7	13.5	13.8	6.3	7.5	7.4	18.3	12.2	16.0
Baseline 125°C	8.6	8.7	6.7	20.3	11.3	19.2	8.3	9.6	8.0	19.5	11.0	20.4
Baseline -55°C	6.4	6.0	6.1	19.7	12.7	15.0	6.5	6.6	6.4	19.7	13.6	13.9
Volt Cond. 25°C	2.43	2.92	2.68	2.48	2.53	3.31	1.66	2.93	4.39	1.27	3.26	4.39
Final 25°C	6.06	6.00	204.	13.48	11.48	13.43	2.24	5.81	14.64	15.62	10.69	14.31











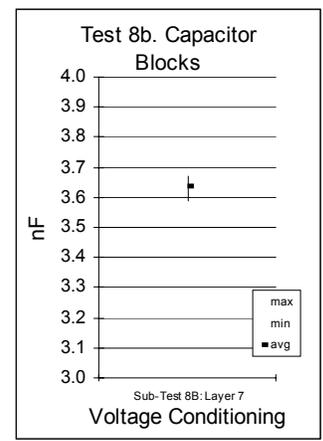
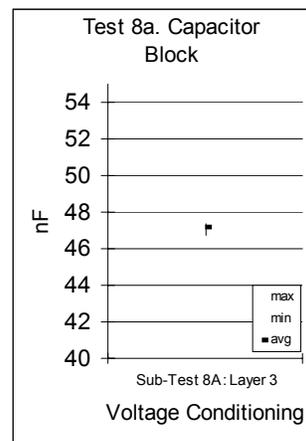
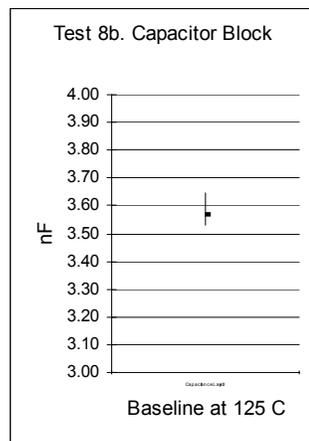
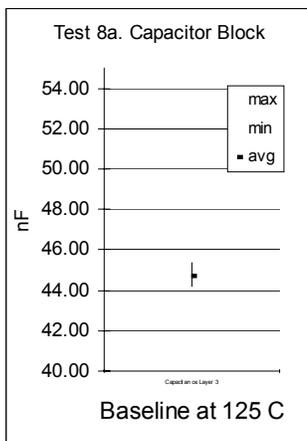
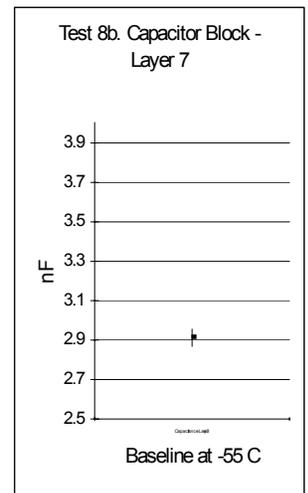
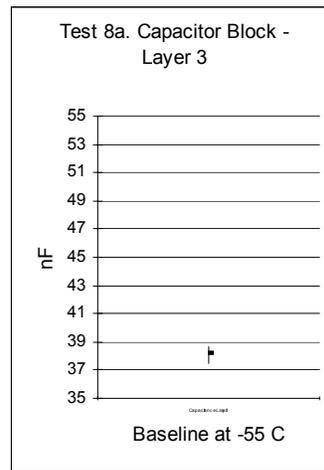
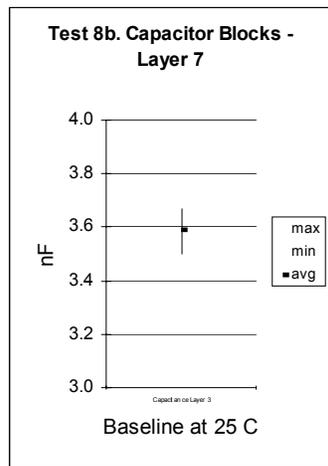
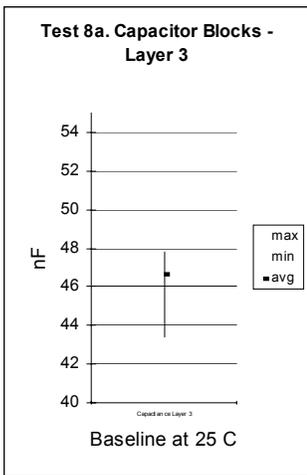
7.0 Test 7 was not performed.

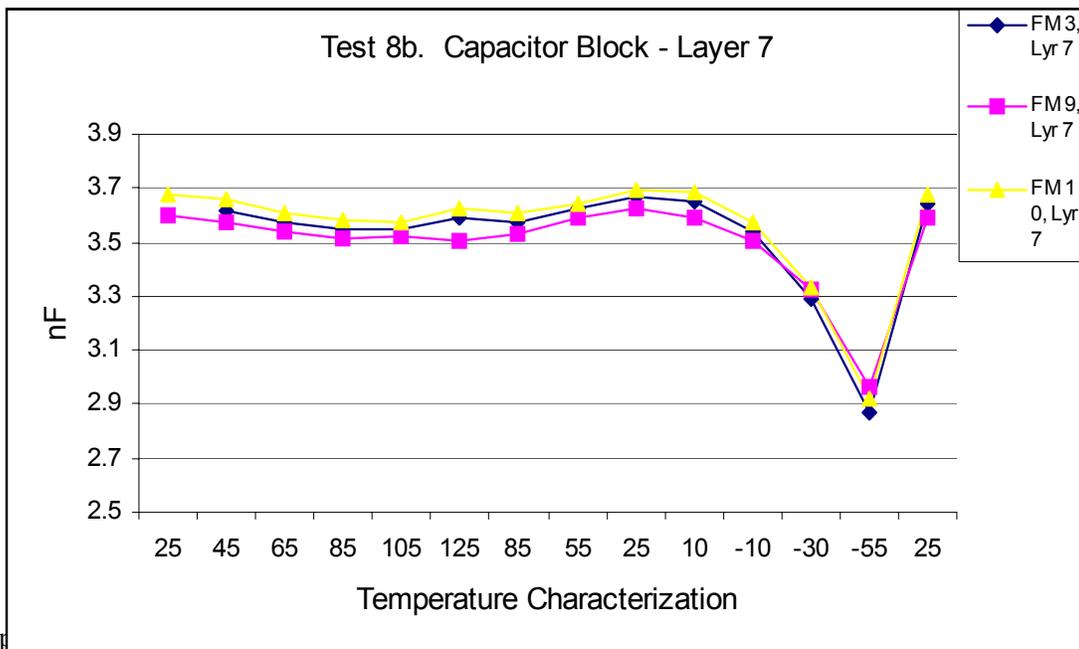
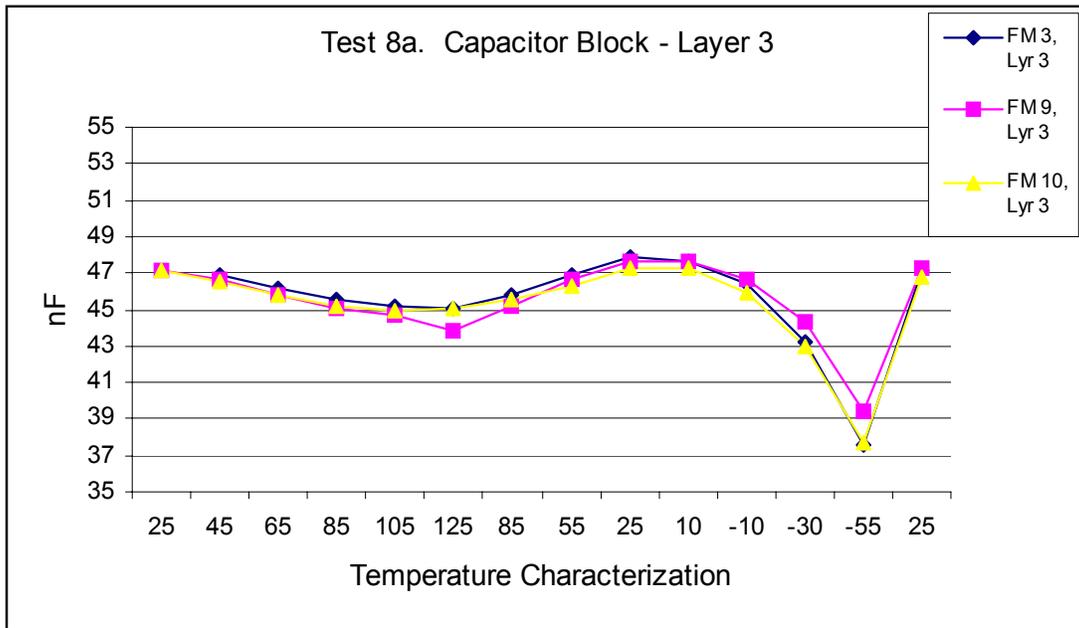
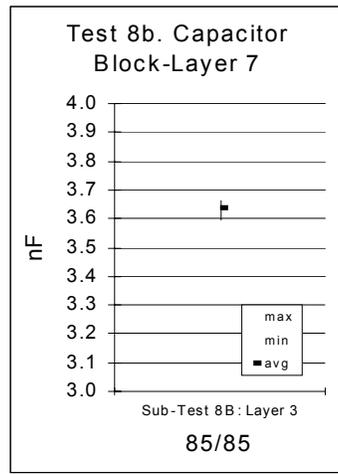
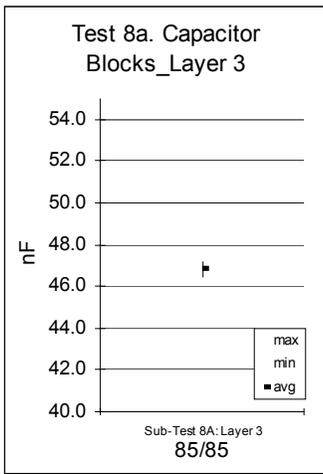
8.0 Capacitor Blocks

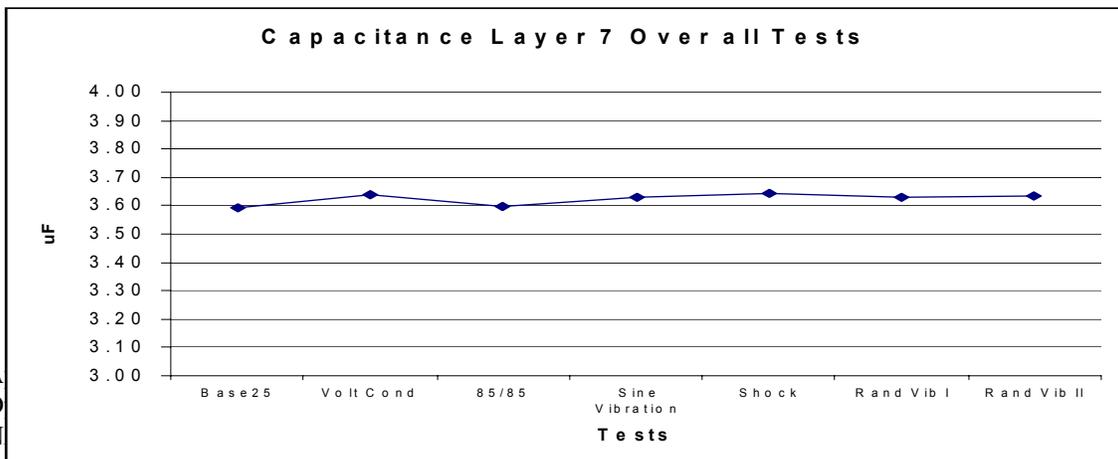
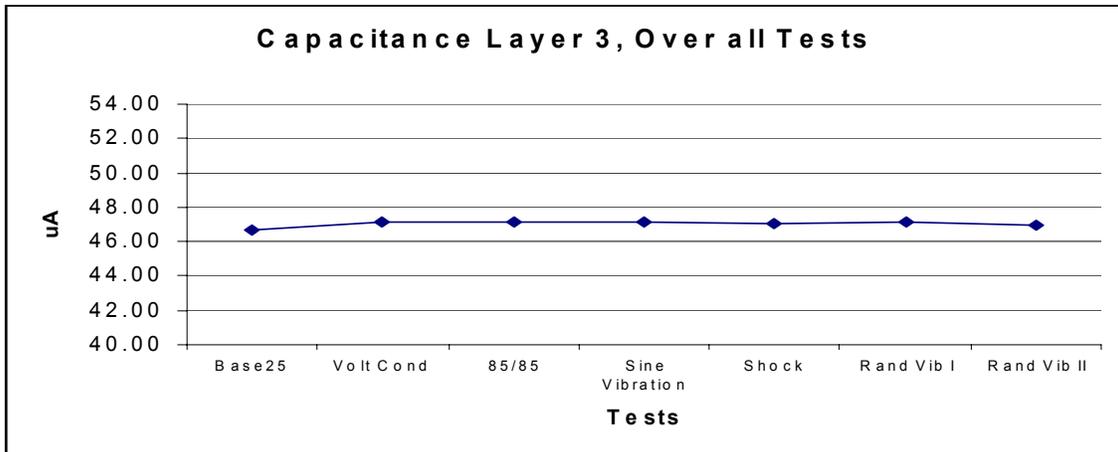
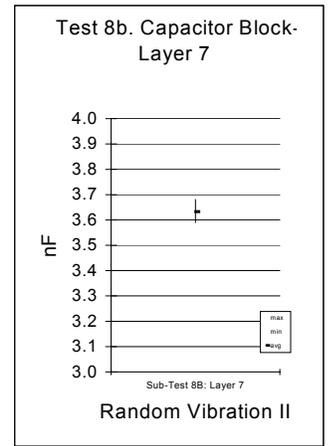
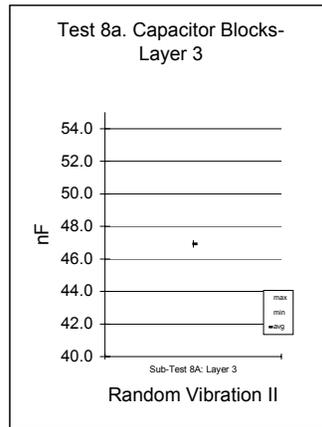
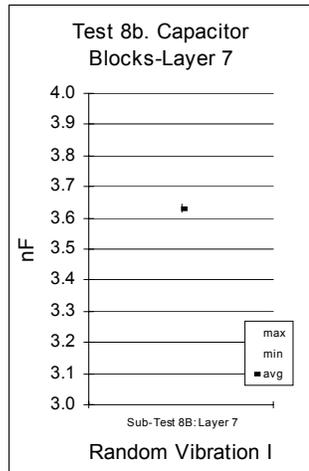
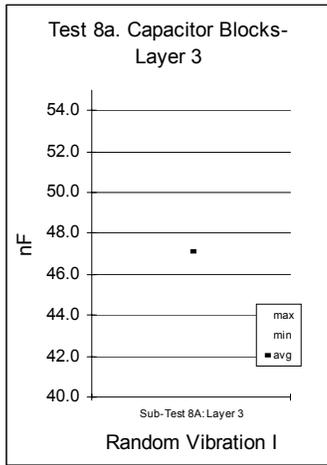
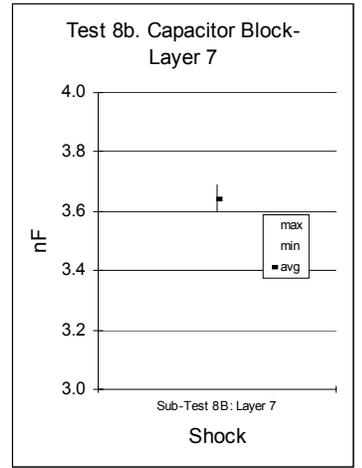
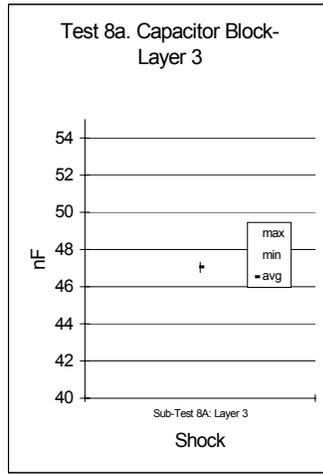
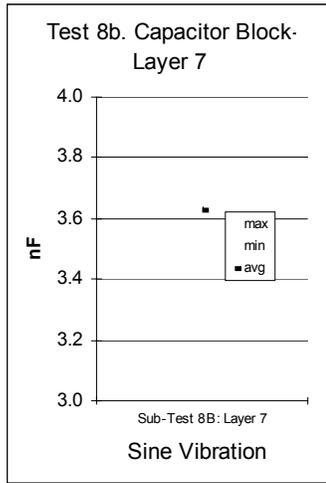
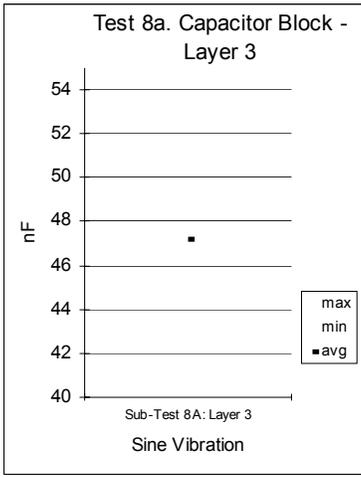
Capacitance was measured for the capacitor blocks on layers 3 and layer 7. The expected values for the capacitors on layer 3 were 40 to 55 nF. The expected values for the capacitors on layer 7 were 3 to 4 nF.

Table 1. Control Sample Values (nF)

Test	Lyr3	Lyr7
Baseline 25°C	47.45	3.61
Baseline 125°C	44.77	3.56
Baseline -55°C	38.24	2.91
Volt Cond. 25°C	47.29	3.62
Final 25°C	47.35	3.63





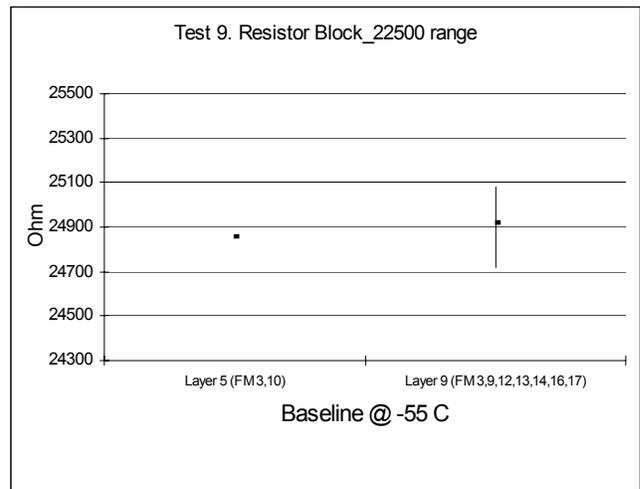
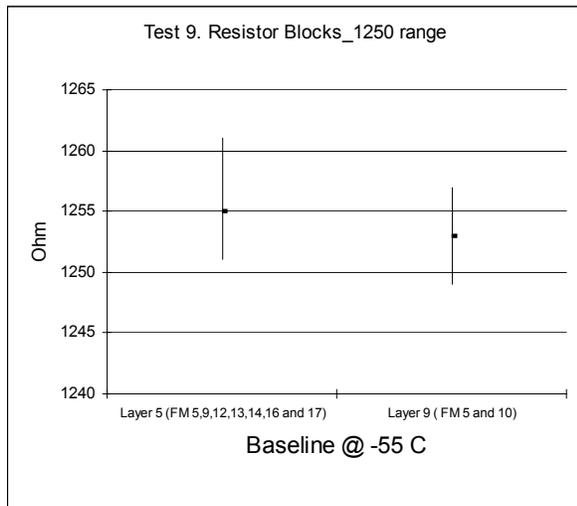
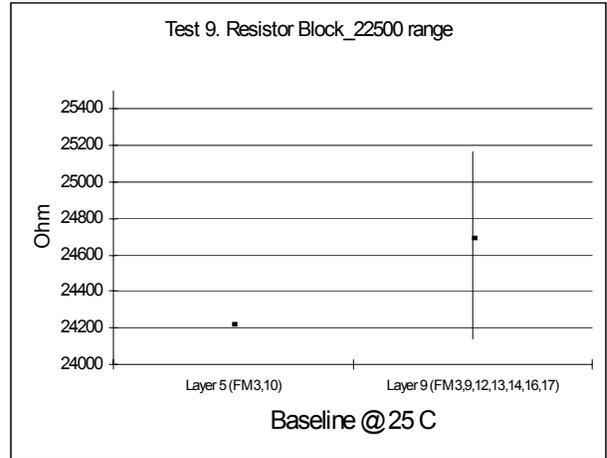
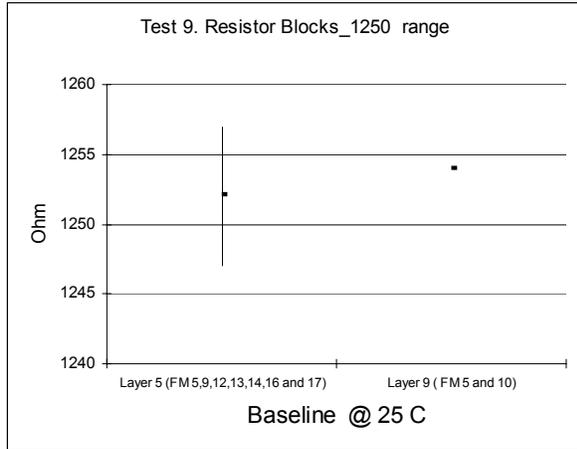


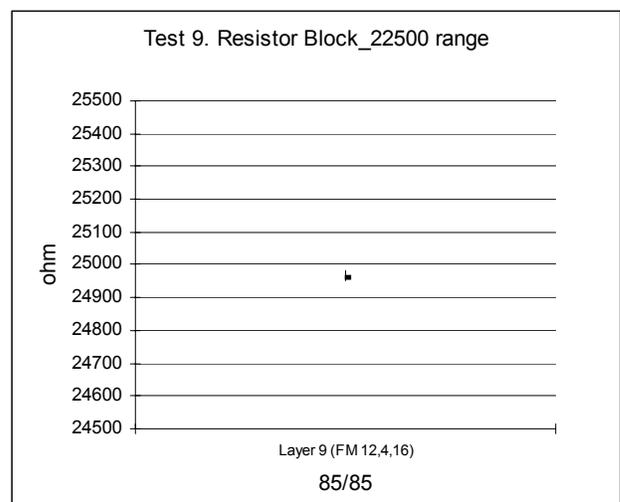
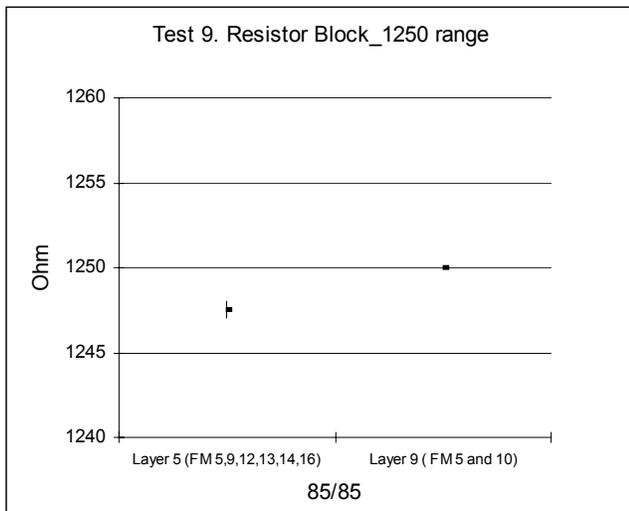
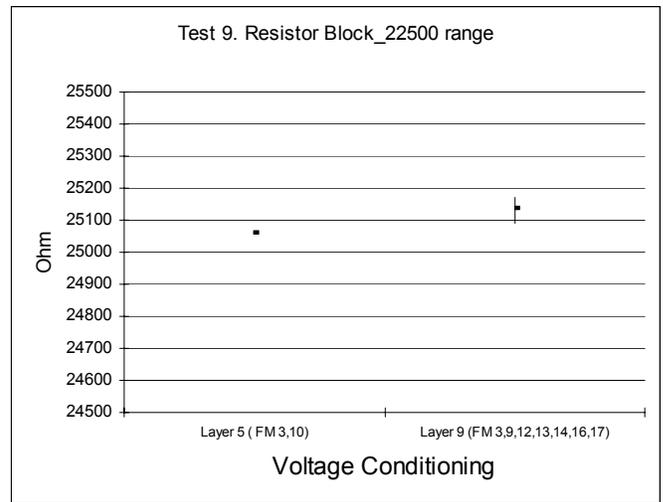
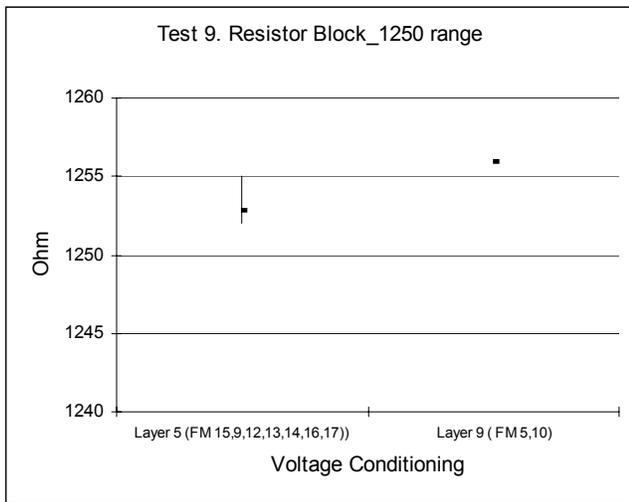
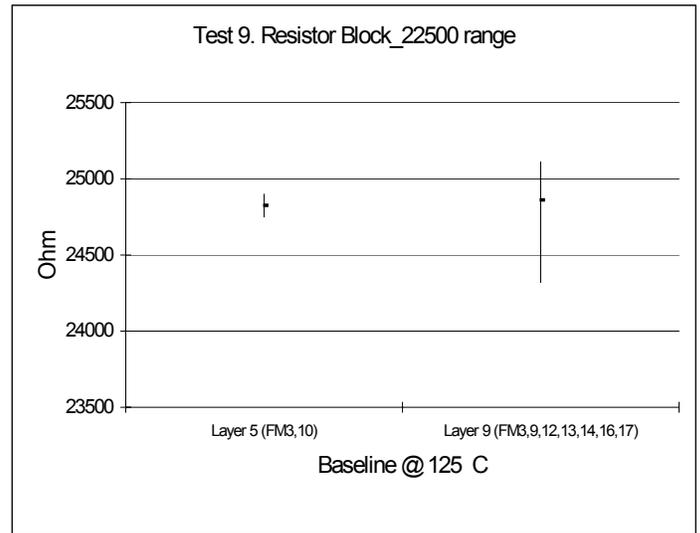
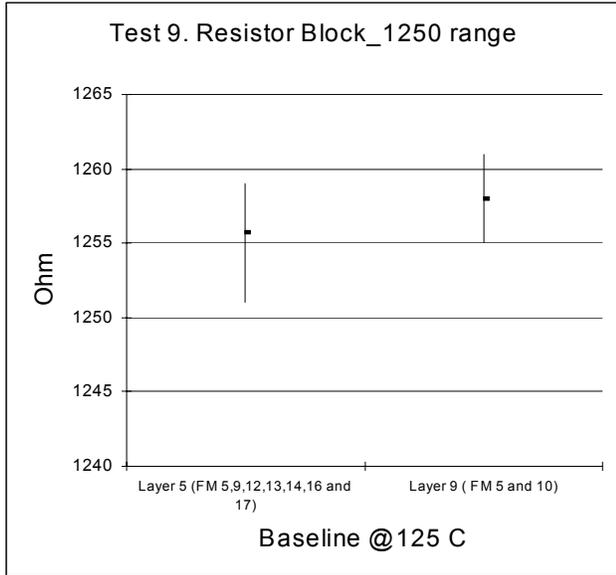
## 9.0 Resistor Blocks

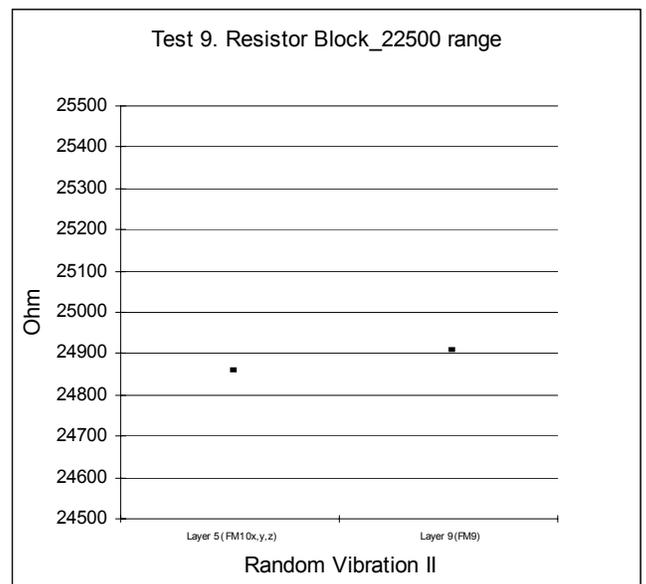
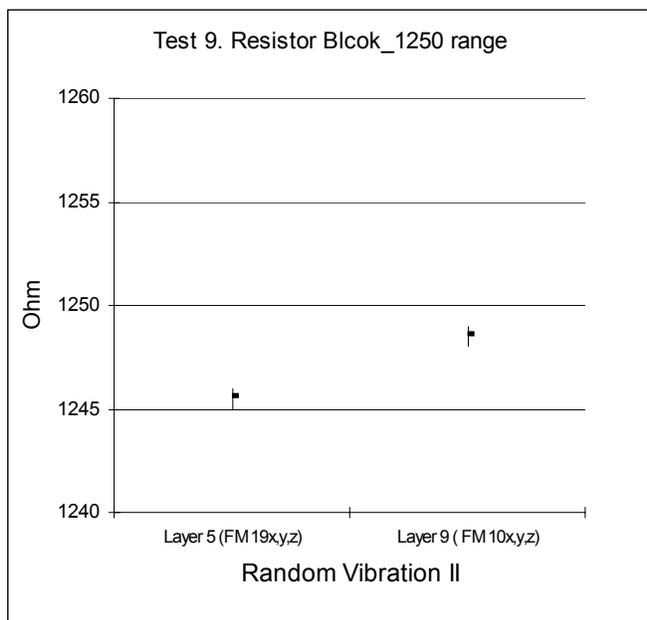
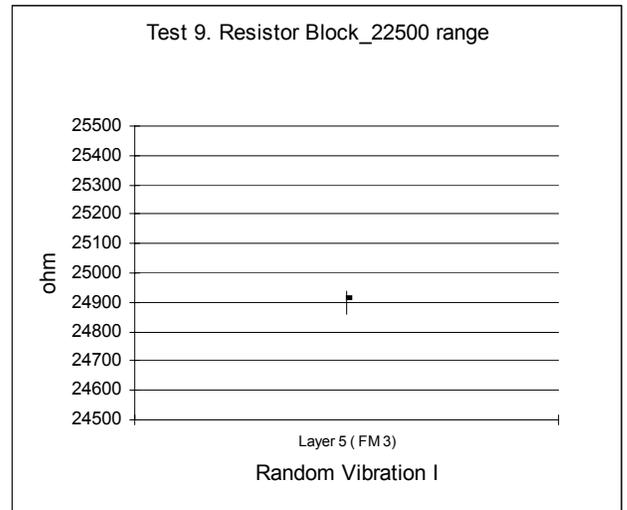
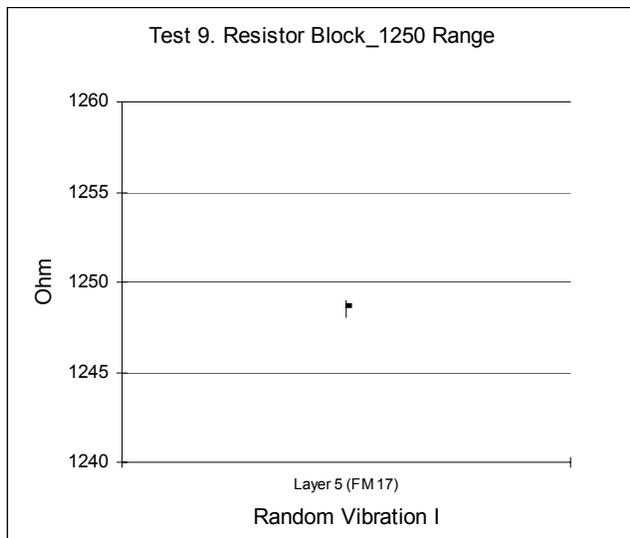
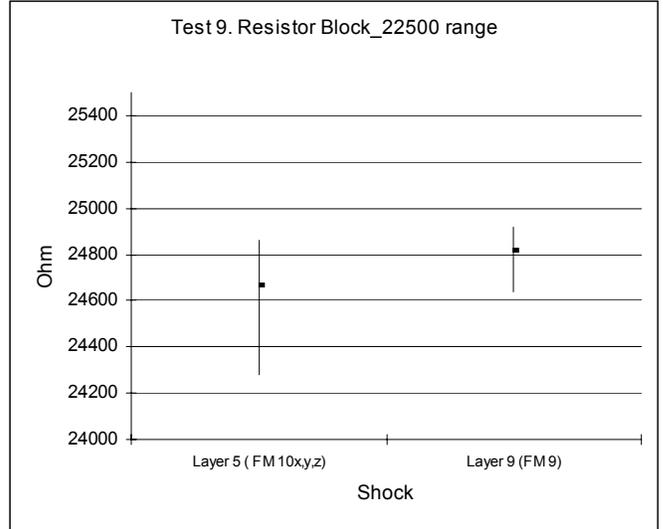
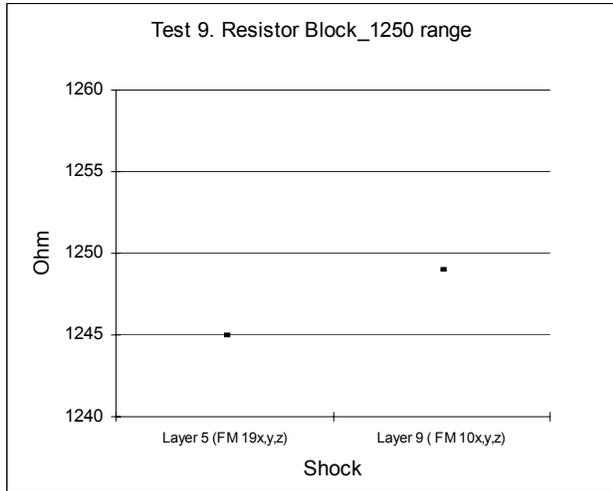
Resistance was measured for the resistor blocks on layers 5 and layer 7. The expected values for the capacitors were 1125 to 1375 Ohms or 22,500 to 27,500 Ohms. The test set-up contributed excess resistance to this measurement so hand measurements were made to achieve this data. No hand measurements were made following the Sine Vibration test however the automated data collected for that test was in family with other automated data and showed no catastrophic failure. The values shown in the graph are points indicating the average value and a line showing the spread of the minimum and maximum value.

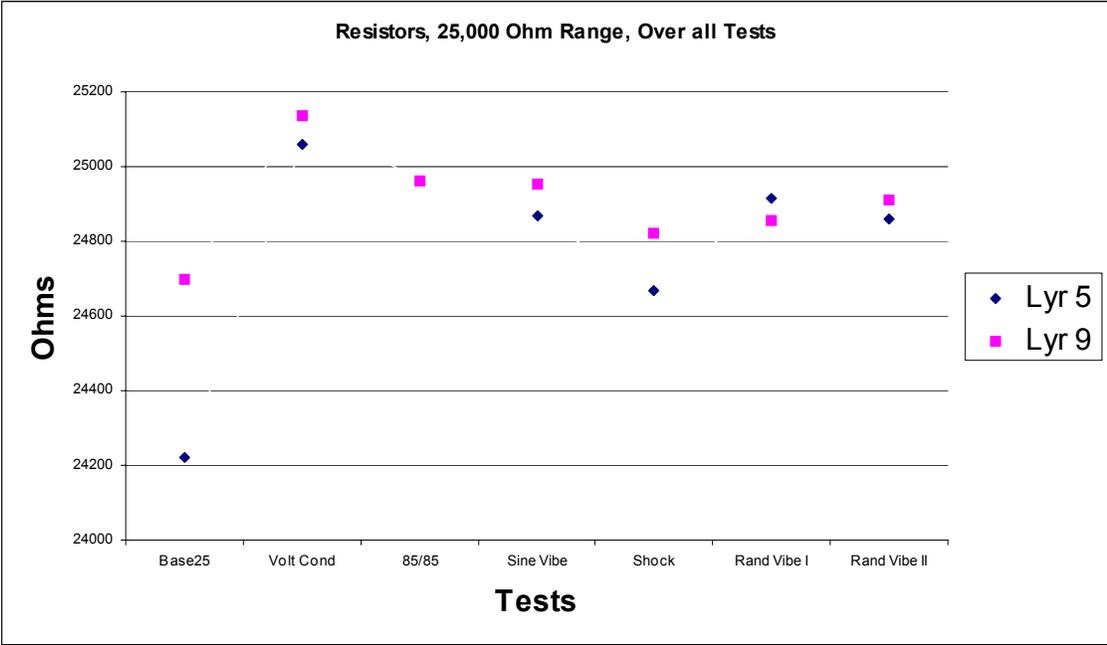
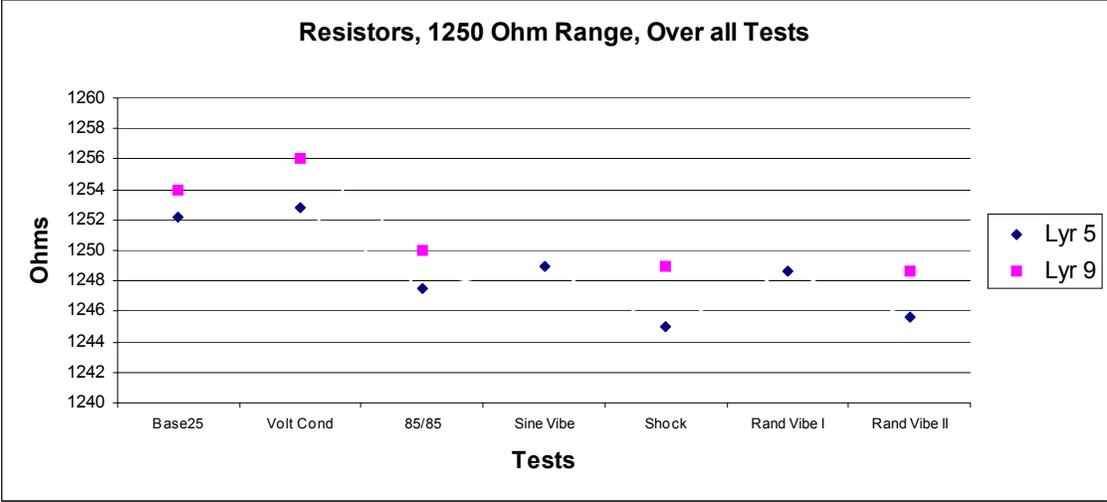
Table 1. Control Sample Values (Ohms)

Test	1250 Range	22,500 Range
Baseline 25°C	1247	24,890
Baseline 125°C	1251	24,950
Baseline -55°C	1251	24,970
Volt Cond. 25°C	1253	25,090
Final 25°C	1247	21,900







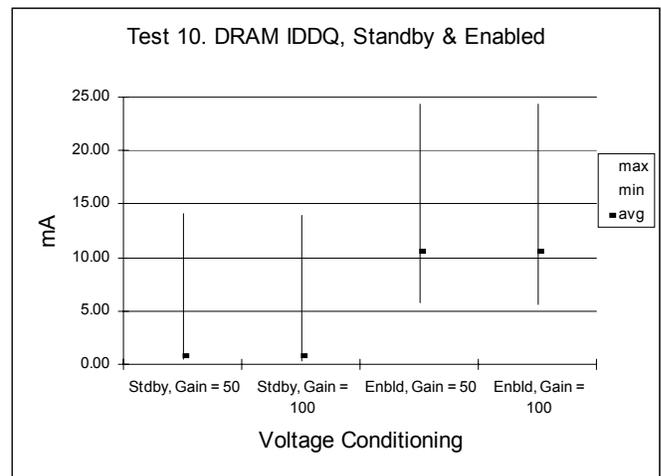
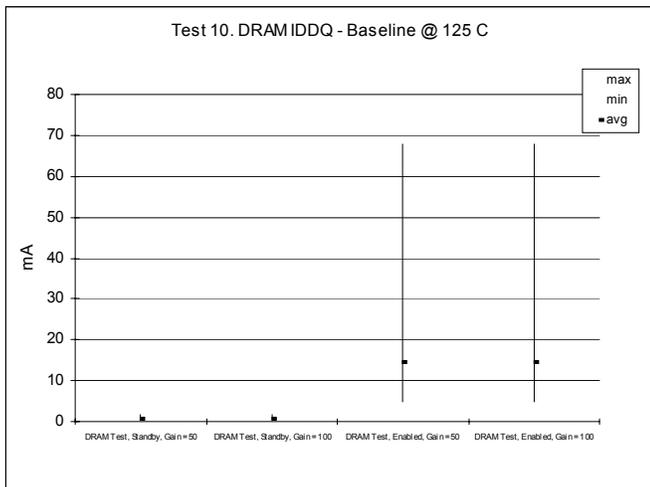
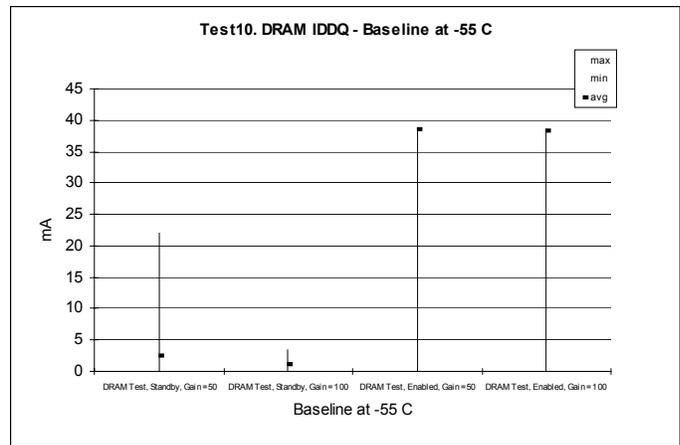
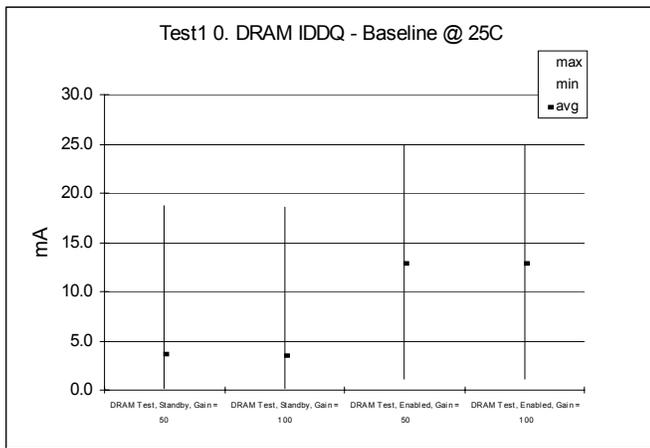


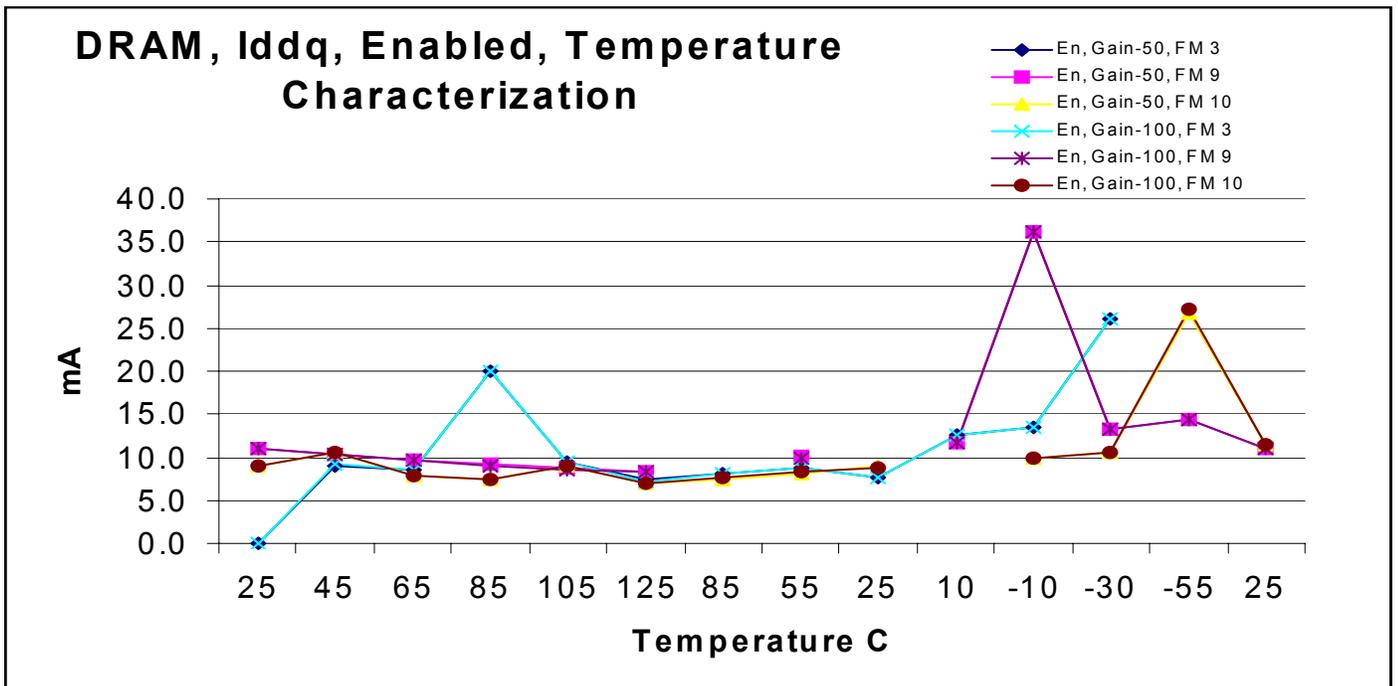
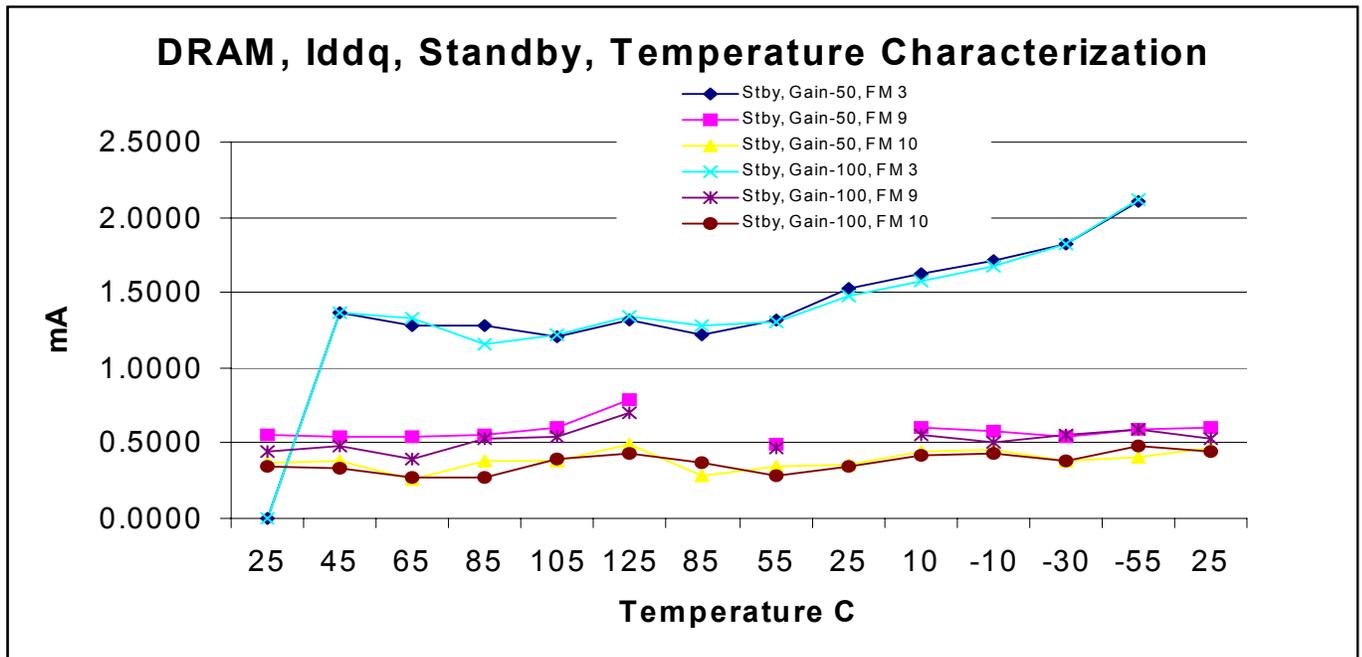
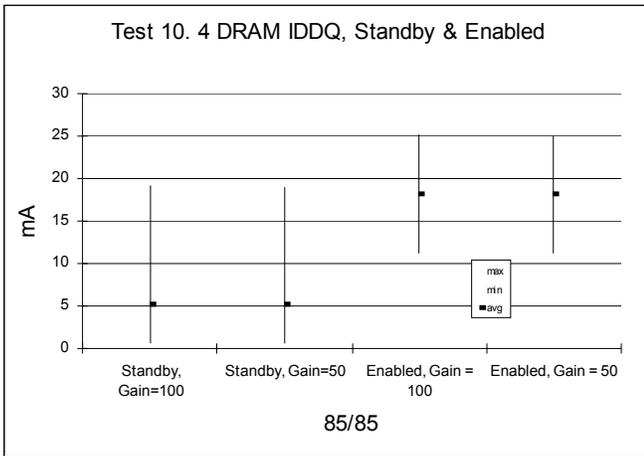
## 10. DRAM

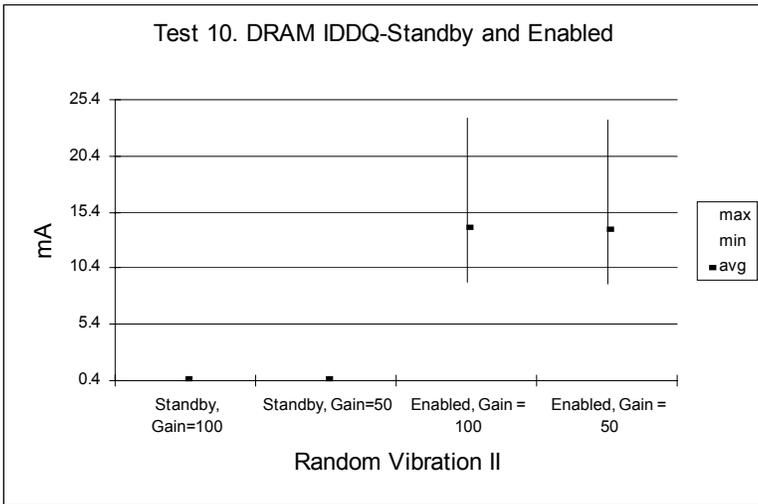
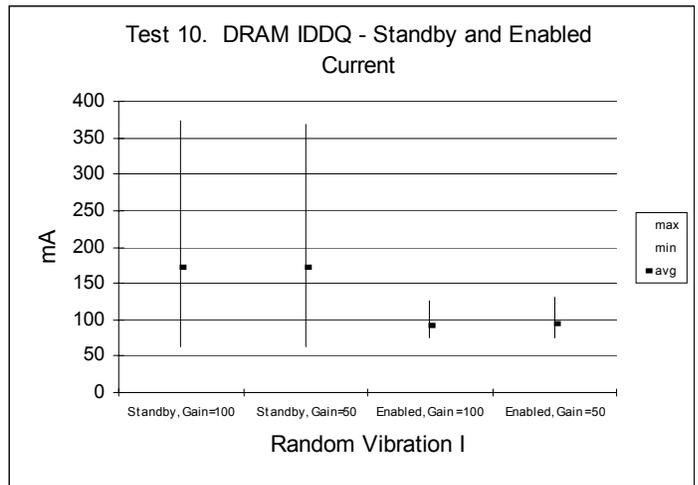
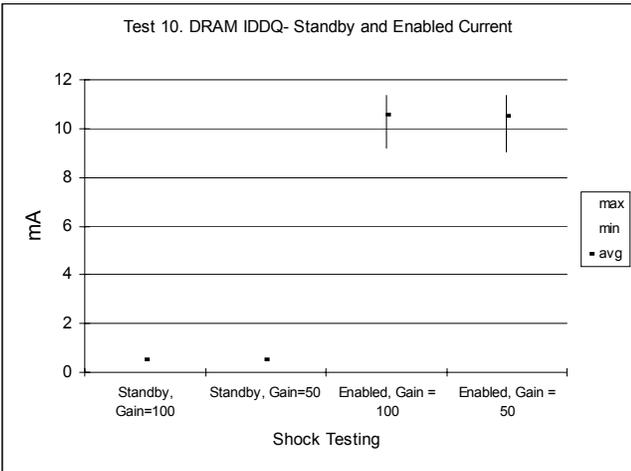
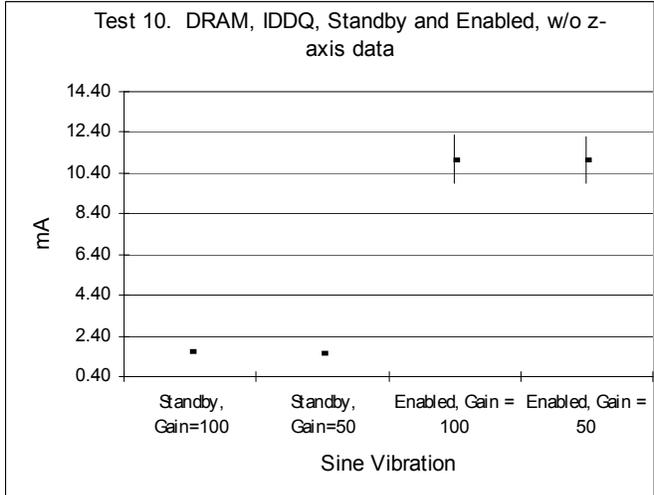
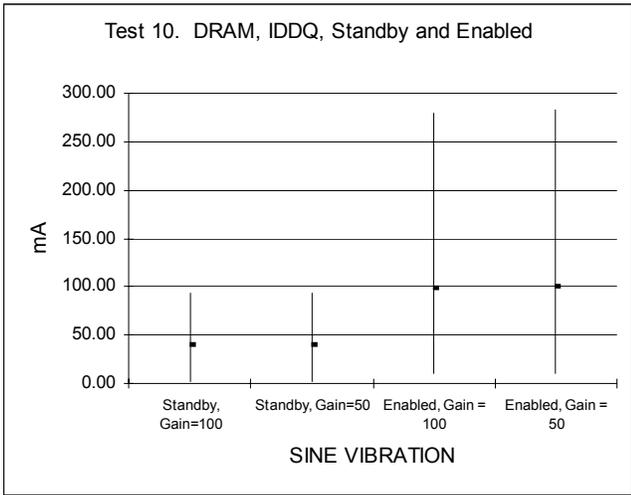
A combined IDDQ was measured for the four DRAM chips both in an enabled and standby state. Gains of 50 and 100 were also used. The expected values were less than 2 mA for the standby condition and less than 480 mA for the enabled condition.

Table 1. Control Sample Values (Ohms)

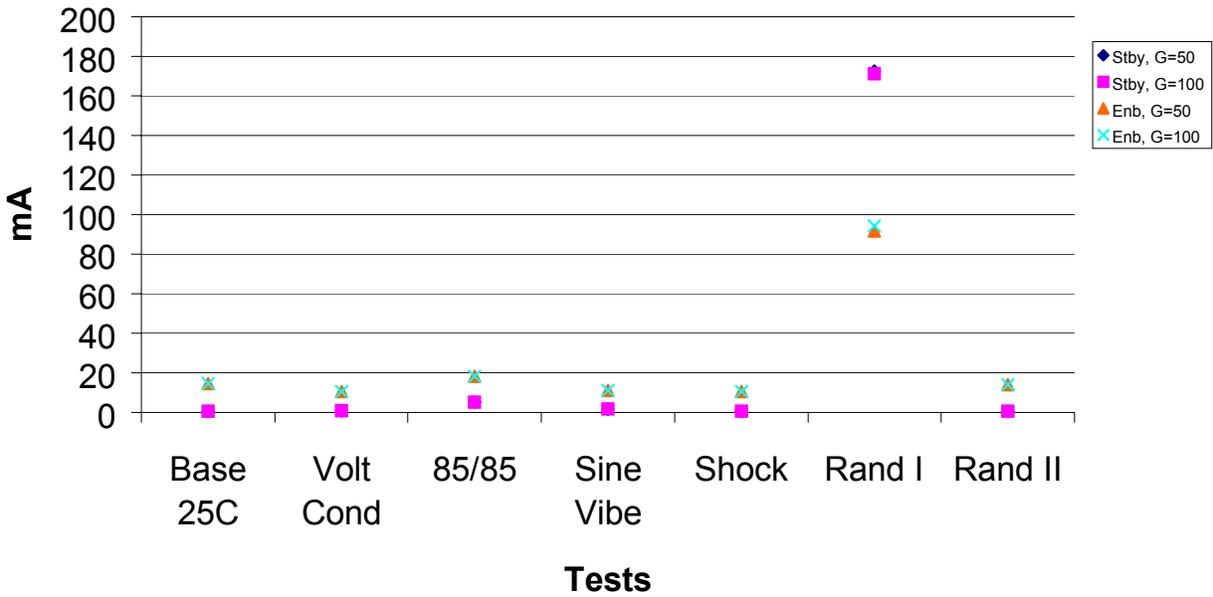
Test	Standby Gain=50	Standby Gain =100	Enabled Gain=50	Enabled Gain =100
Baseline 25°C	0.2	0.2	8.6	8.6
Baseline 125°C	0.3	0.4	7.8	7.8
Baseline -55°C	0.2	0.2	11.0	11.0
Volt Cond. 25°C	0.4	0.4	22.0	21.9
Final 25°C	2.5	2.4	8.7	8.7



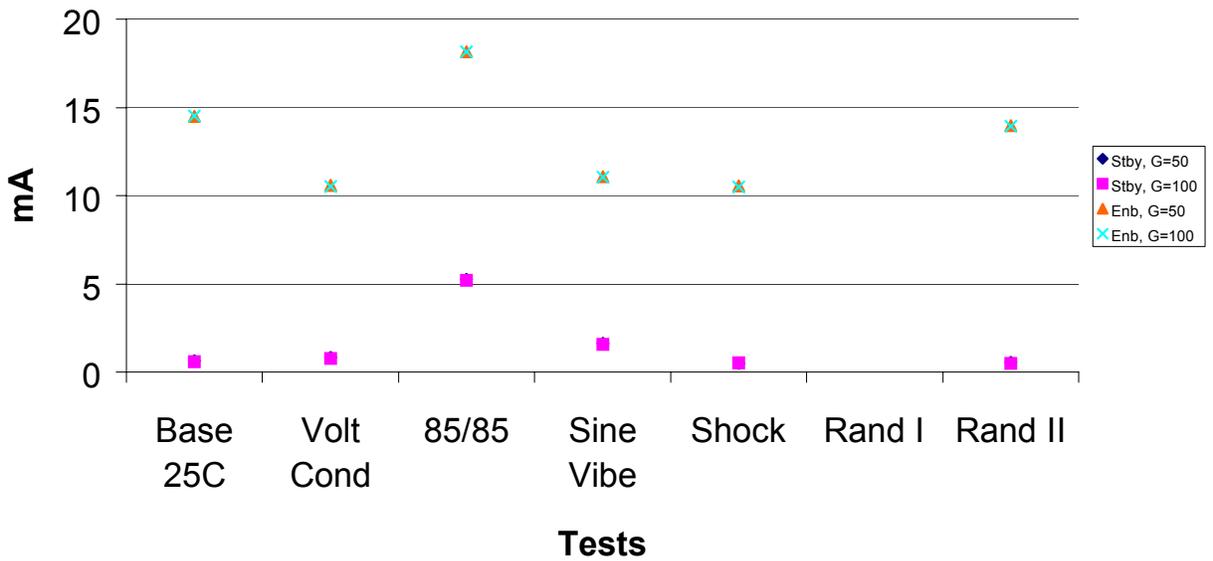




### DRAM, Iddq, Over all Test, w/Post Rand I Data



### DRAM, Iddq, Over all Test, w/o Post Rand I Data



## Appendix III

Appendix III reports what was found from Finite Element Modeling of the subject part and the test boards. The file copy available for this publication does not contain clearly readable plots and those plots cannot be replicated at this time. The text of the report, which is readable, quantifies the expected stress on the solder joints and relates how the analysis was performed.

**Thermal and Dynamic Assessment  
for 3D-Plus MCM-V Module**

**Mark S. Fan**

NASA Technology Validation Assurance Group

Goddard Space Flight Center

Greenbelt, Maryland

September 1, 1999

## **1. INTRODUCTION**

This report outlines the results of thermal and random vibration analyses performed on the surface mount 3D-Plus MCM-V Cube. The 3D-Plus MCM-V Cube is an plastic-encapsulated 3-D stack multichip module manufactured by 3D Plus Electronics Company in France. A general view of the structure of the device is shown in Figs. 1-3. Two major analyses have been performed to assess the reliability of the module, namely, thermal analysis for assessing its conductive thermal performance as well as random vibration analysis for assessing the integrity of surface mount solder attachments.

## **2. THERMAL ANALYSIS**

Thermal conductive analysis was performed under the normal operating conditions to examine the temperature distribution throughout the body of the 3D module. Generally speaking, plastic encapsulated electronic devices are not effective in heat conduction largely because of the low conductivity of the encapsulation material. Thus, a detailed assessment of thermal conduction is of great importance for spaceflight applications.

## 2.1 FEA Model

A 3-D FEA model was built for the thermal analysis (Fig. 4). Due to geometric symmetry, the model represents  $\frac{1}{4}$  of the module. A total of 19404 8-node solid elements is used for this model.

## 2.2 Power Dissipation and Material Properties

Because of the multichip structure, total power dissipation is from several semiconductor chips and passive elements simultaneously during normal operation. Although the module can be biased at several different levels resulting in different values in total power dissipation, the analysis was performed based on a nominal voltage bias, i.e., the total power dissipation was 2.968 W. Table 1 summarizes the voltage and power dissipation from different heat-generating elements.

Table 1

ELEMENTS	POWER (mW)
Resistors	121
Constraint Chip	427
Thermal Chip	1920
TSOP DRAM	500

Material properties used for the analysis are listed in Table 2.

Table 2

MATERIAL	Si	Fe/Ni Alloy	Solder	FR-4	Hysol-4450
CONDUCTIVITY (W/mK)	148	129	50.6	0.2	0.6
YOUNG'S MODULUS (GPa)	110	145	14.9	17	12.5
POISSON'S RATIO	0.28	0.3	0.29	0.3	0.31
DENSITY (kg/m <sup>3</sup> )	2330	8110	8470	1938	1770

### 2.3 Thermal Boundary Conditions

In the analysis, the surface of the PCB to which the module is attached was used as a heat sink, and the temperature rise in the module was based on the heat sink reference temperature.

## 2.4 Temperature Results

Fig. 5 shows the steady-state temperature distribution under the power dissipation conditions listed in Table 1. It is revealed that the maximum temperature rise ( $\Delta T_{\max}$ ) is 50.1 C. Thus, in order to keep the device operating in a safe region, the PCB surface temperature should not be exceeding 65 C.

## **3. DYNAMIC RANDOM VIBRATION ANALYSIS**

Random vibration and dynamic response analyses were also performed for this 3D module. In the dynamic analysis, the device was surface mounted onto a PCB simulating anticipated GSFC lab testing. The PCB (FR-4) is square in shape, with 4.5" length on each side. The thickness of the PCB is 0.062". Fig. 6 shows the PCB and surface mount layout.

The main purpose of the dynamic analysis is to extract the assembly's resonant frequencies and obtain root-mean-square (RMS) dynamic stresses over the random frequency range on the 63:37 solder attachments. In the GSFC test plan, two 3D MCM-V modules were planned to be mounted for random vibration experiment (see Fig. 6), however, our SUN Ultra-10 workstation has only 256 MB RAM and it was unable to perform such a large dynamic FEA simulation. Thus, the simulation had to be performed

by removing one of the modules off the PCB. In Fig. 6, only the module mounted on the left side was included in this dynamic simulation.

In order to accurately simulate the stress concentration in the solder attachments during random vibration, finer mesh must be used for the solder joints and leads. This is the main reason why this FEA model is very big. Fig. 7 shows the details of the finer FEA mesh in one of the corners of the module.

The input acceleration spectral density (ASD) provided by the manufacturer in France was used in the analysis. The acceleration level of this ASD is unusually high, compared to what NASA's random vibration requirements call for the testing of spaceborne sub-assemblies. This ASD is shown in Table 3.

Table 3

FREQUENCY (Hz)	ACCELERATION ( $G^2/Hz$ )
50 – 100	+6 db/oct
100 – 1000	0.8
1000 – 2000	-6 db/oct
Overall G (RMS)	33.8

Boundary conditions used for the dynamic analysis was to simulate GSFC test setup, namely, 5 screws will be used to attach the PCB assembly to the fixture of the vibration test equipment. Four screws are used at the four corners, and the fifth screw will be located at the geometric center of the PCB assembly. These screws will completely restrain the degree-of-freedom in Dx, Dy, and Dz at their mounting locations.

In the random vibration analysis, this ASD was applied to the direction perpendicular to the PCB plane (z-direction). In the first step of the analysis, four eigenmodes were extracted for this PCB assembly. The first four resonant frequencies are:

$$F1 = 1052 \text{ Hz}$$

$$F2 = 1520 \text{ Hz}$$

$$F3 = 1685 \text{ Hz}$$

$$F4 = 1874 \text{ Hz}$$

The modal displacements corresponding to these four eigenmodes are given in Figs. 8 – 11.

As in any vibrational environment, the highest dynamic stresses in the solder attachments occur in the first resonant mode, i.e., at 1052 Hz. Fig. 12 shows the RMS  $\sigma_{zz}$  distribution in the solder joints at 1052 Hz. It is obvious that the highest stress (10.6 MPa) occurs in the corner on the right-hand side, which is consistent with the eigenmodal

displacement shown in Fig. 8. This highest stress is enlarged for better view in Fig. 13. Using the same procedures, we can obtain RMS stress distributions for all the components of the stress tensor. Finally, we can obtain the  $3\sigma$  RMS von Mises stress at that corner solder location with the highest stress concentration:

$$\sigma_{\text{von Mises}} (3\sigma \text{ RMS}) = 34.68 \text{ MPa}$$

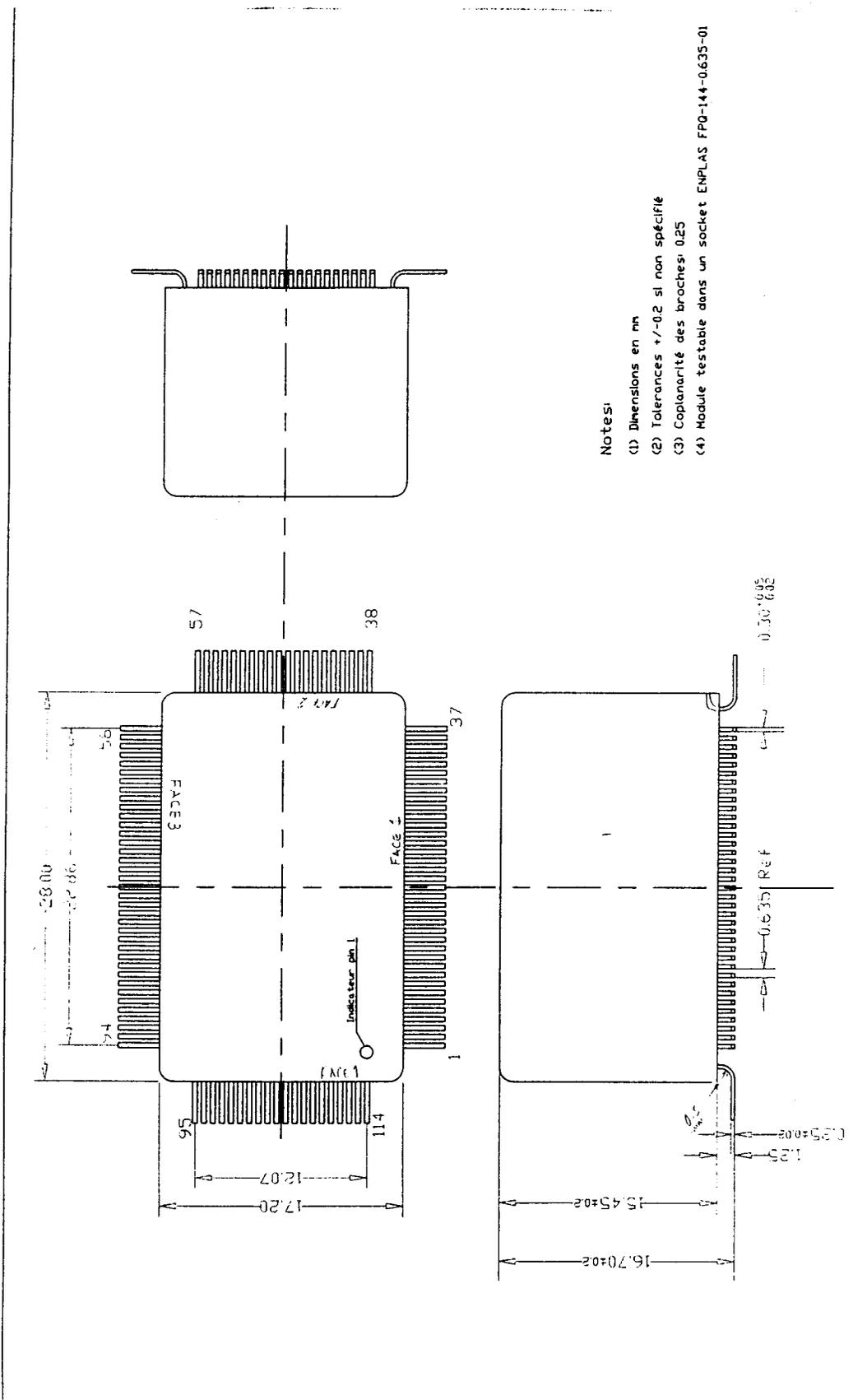
For regular 63:37 eutectic solder, a nominal value of its yielding strength is 16.1 MPa. We see that the highest von Mises stress for that corner joint at 1052 Hz is more than twice the value beyond the yielding point. In our opinion, this solder joint will not be able to survive under such a harsh ASD level largely due to high-cycle solder fatigue.

#### 4. SUMMARY

Thermal, eigenmodal, and random vibration analyses have been performed for the 3D Plus MCM-V Module as a part of the NASA technology evaluation process. Due to large bulk of encapsulation material used for this module, thermal conduction is not as effective comparing with other MCMs used by NASA where ceramic packages are used. Because of the 50 C temperature rise from PCB heat sink, this module should be used with great care when the PCB surface temperature is near 50-60 C.

Due to the center screw mounting for the PCB assembly, the first resonant frequency is more than 1000 Hz. The corresponding von Mises stress at the corner solder

joint (near the PCB edge) is found to be more than twice the value of the eutectic solder's yield strength. Thus, we conclude that this ASD level is too harsh for this particular assembly and should not be used for the testing purposes. If the launch vehicle will indeed deliver such a high  $G_{rms}$ , we then need to redesign the module attachment in order to survive the launch process. If that is the case, we will need to perform a series of FEA simulations to find an optimal scheme for module attachment.



Doc. N°: 3300-0100-2

Fig 1

**CUBE CROSS-SECTION (SIMPLIFIED)** See Doc N°3300-0100 for more details.

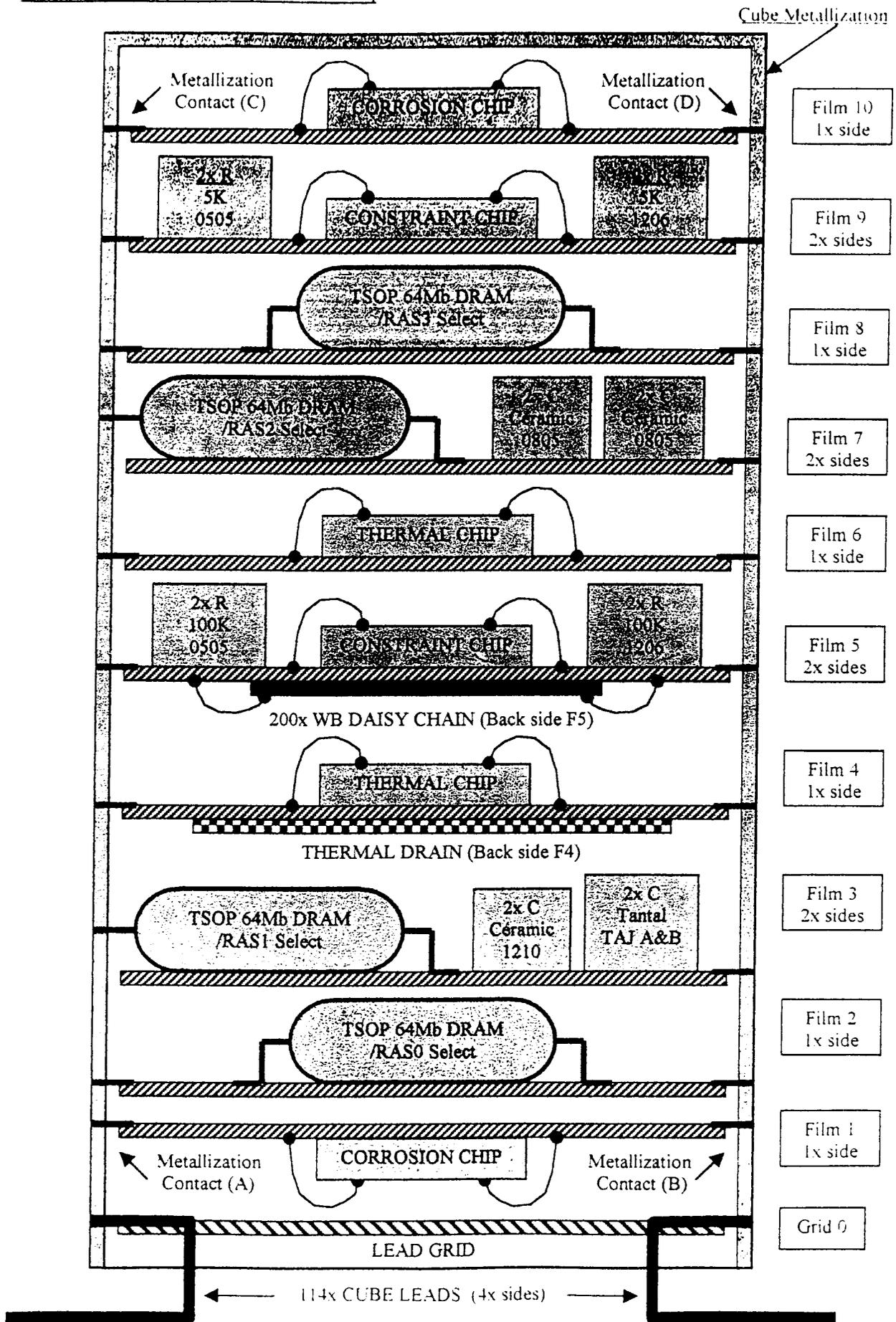


Fig. 2



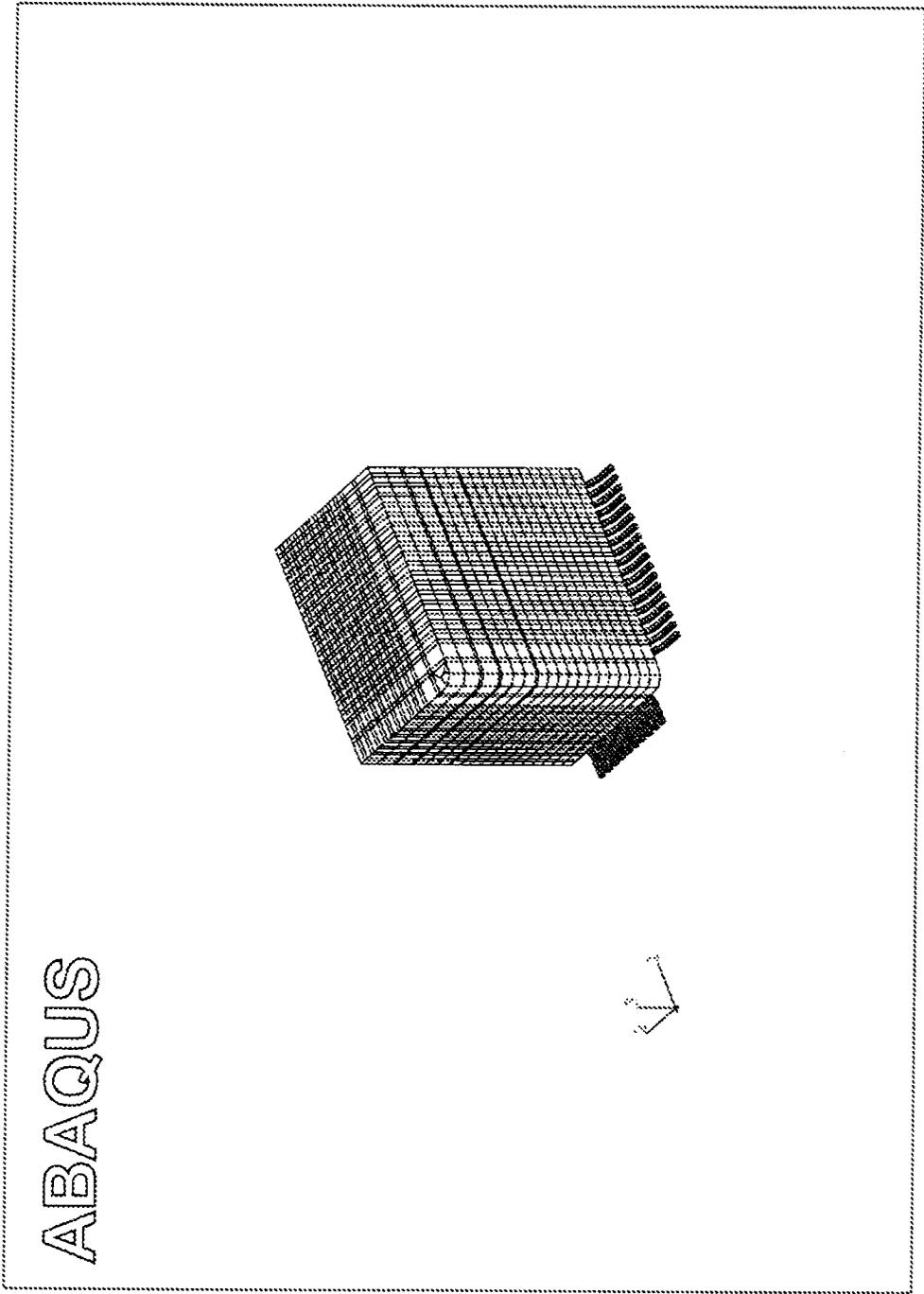


Fig. 4

TMP

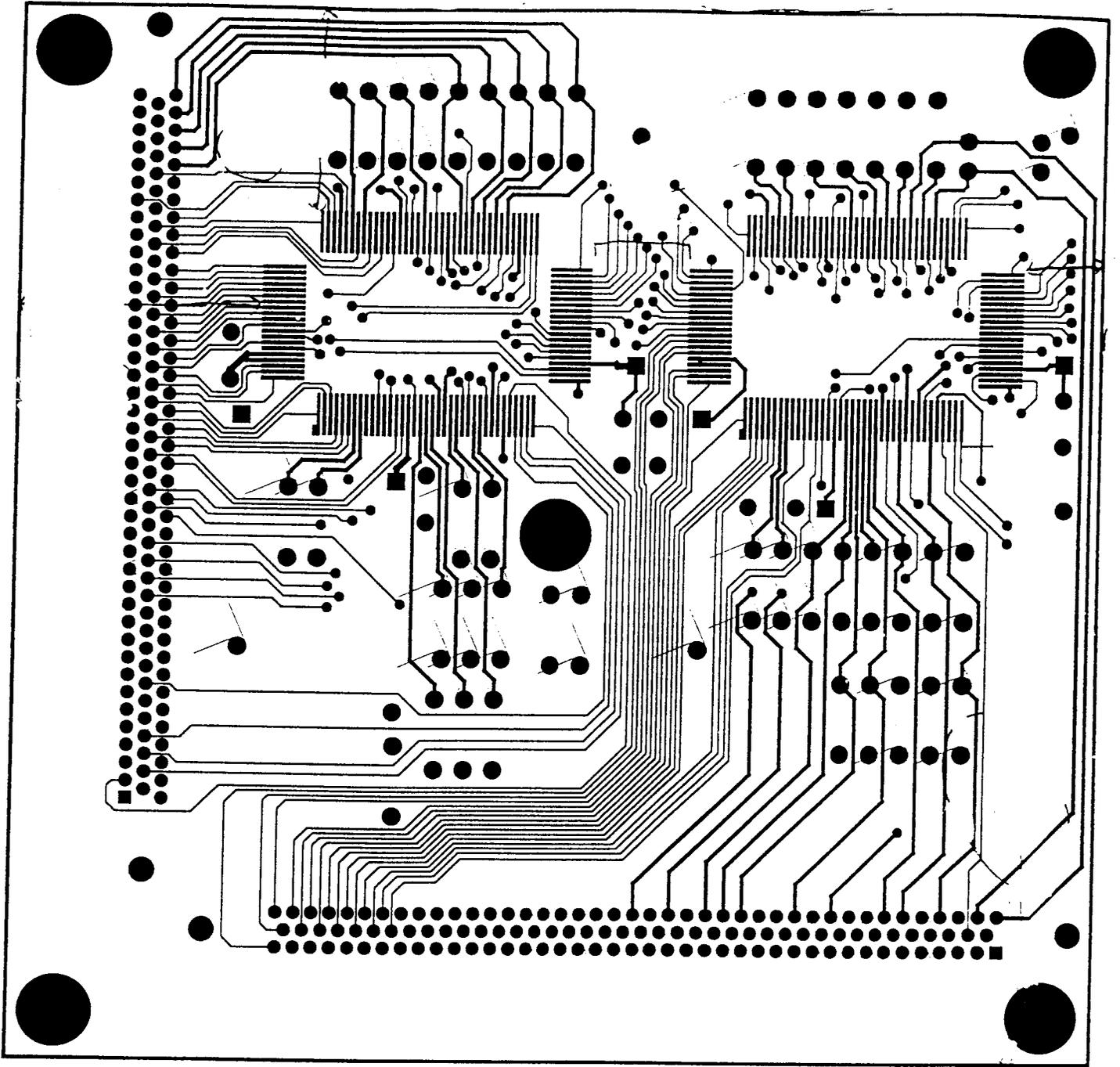


Fig. 6

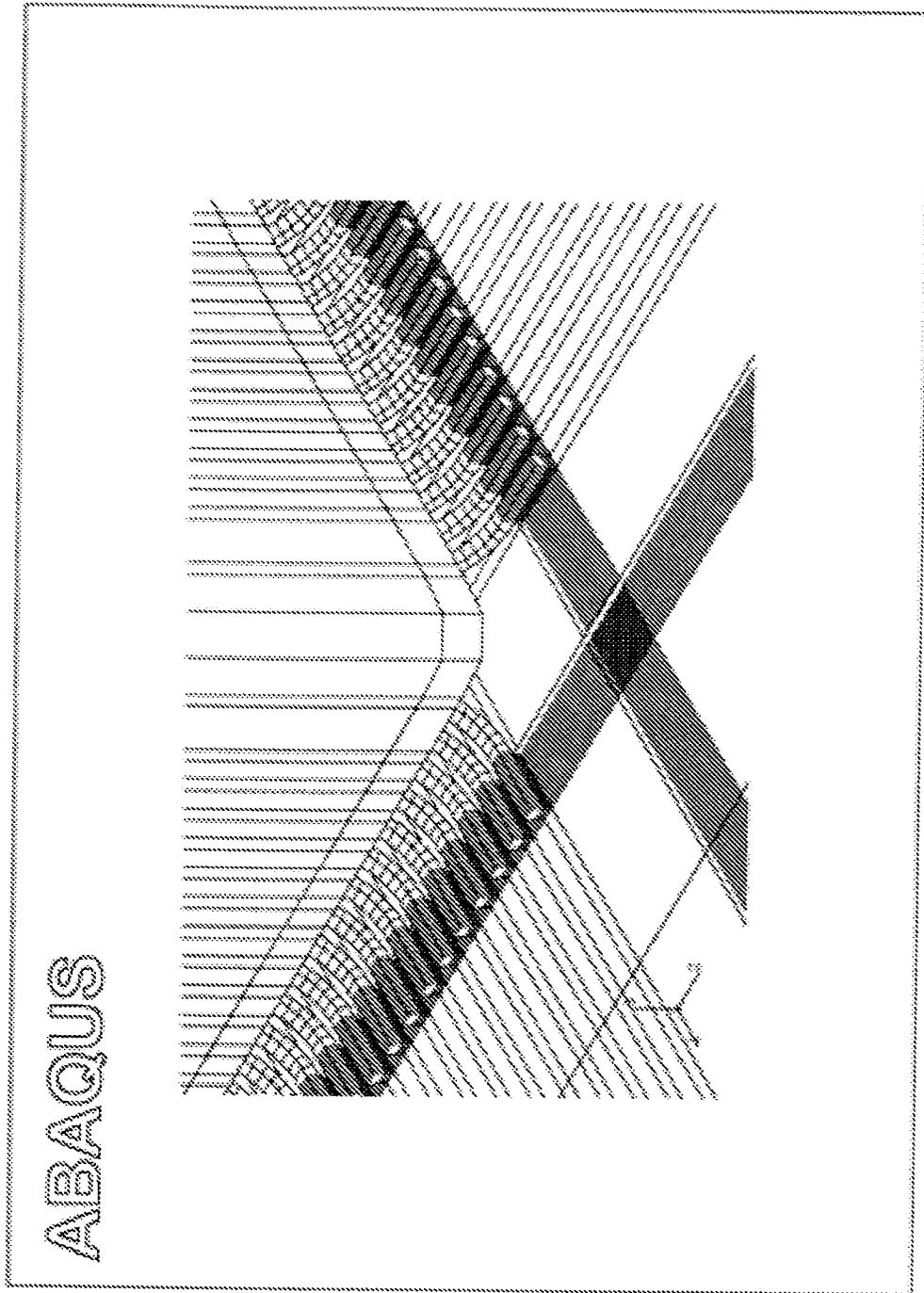


Fig 7

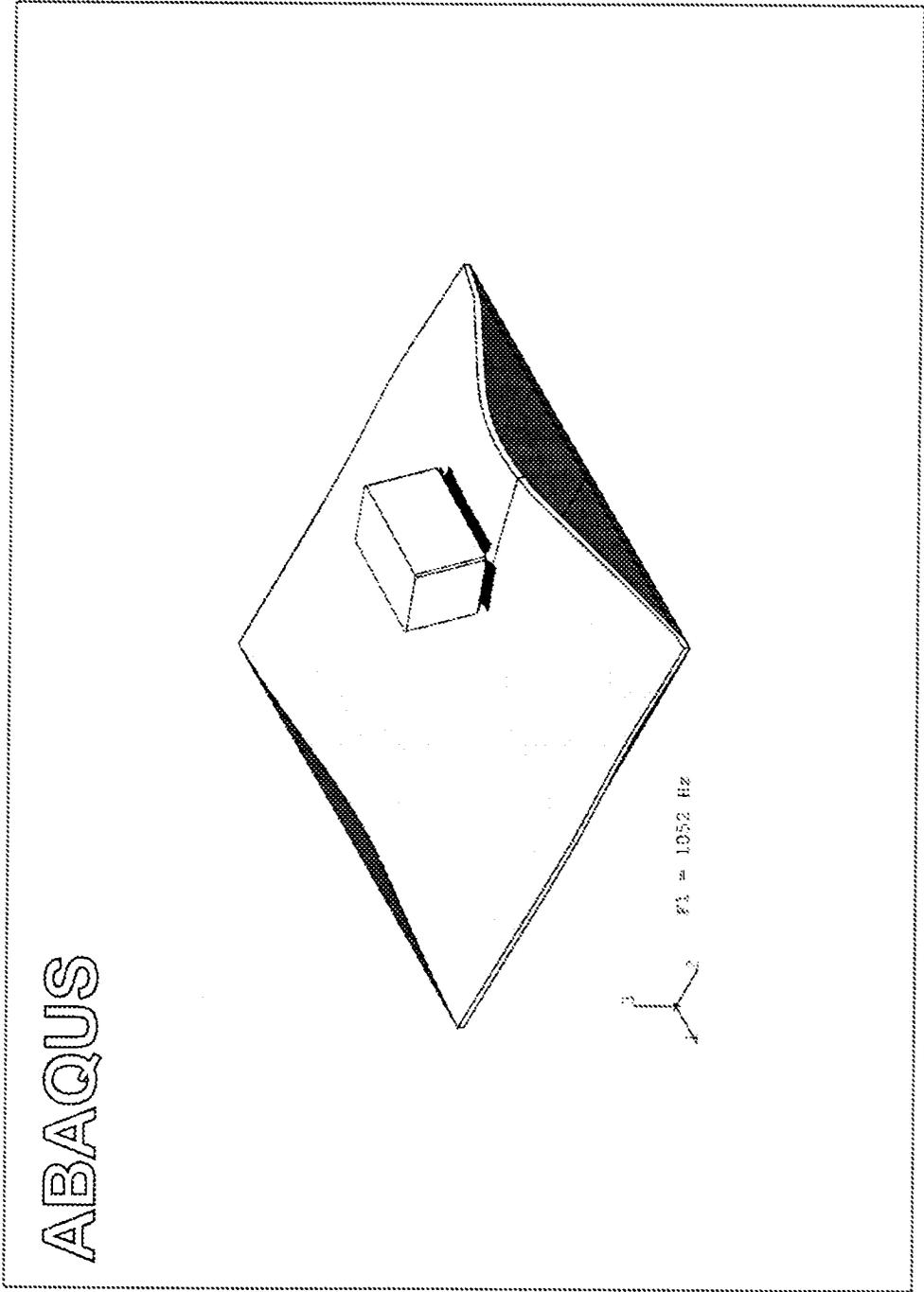


Fig. 8

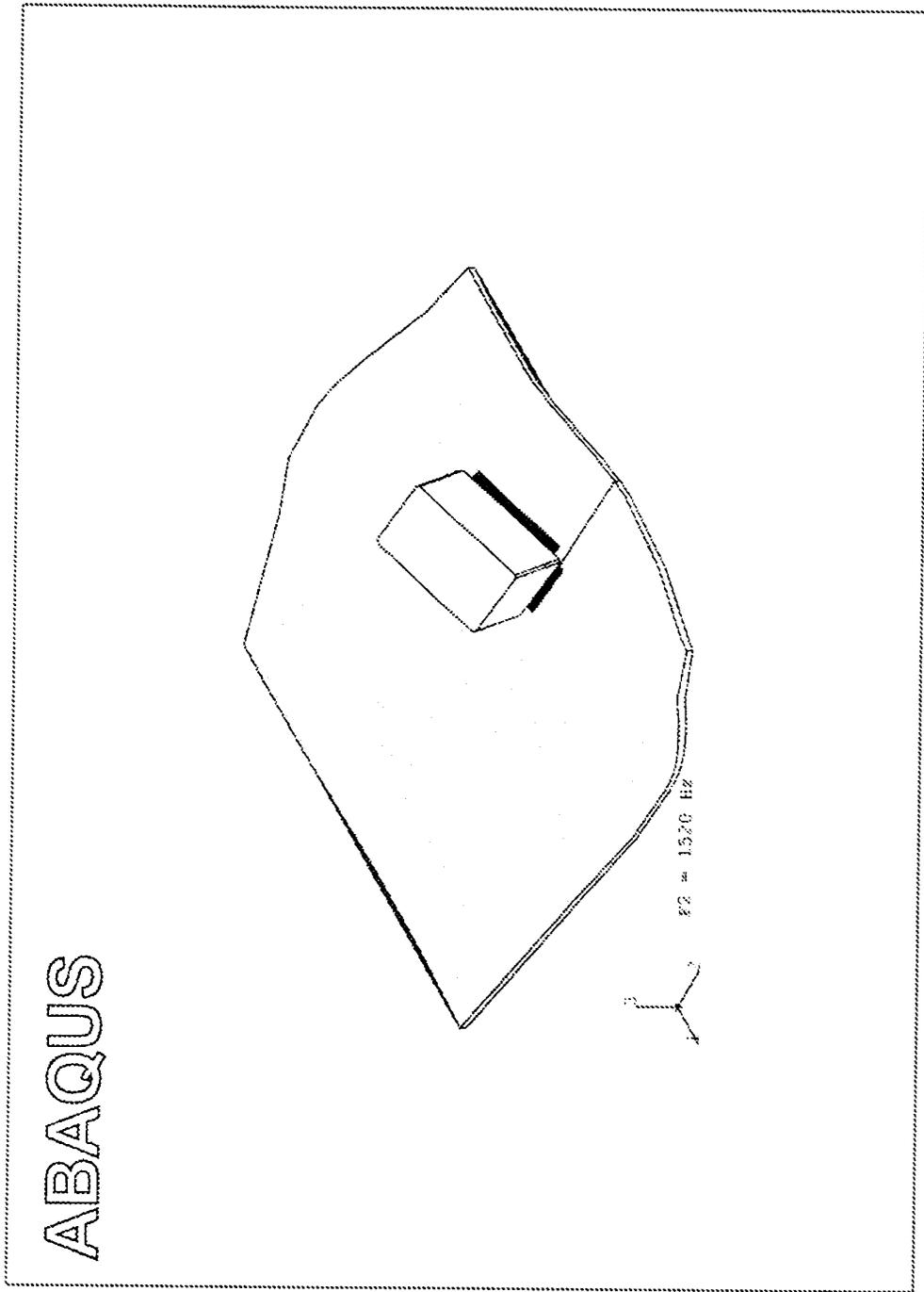


Fig. 9

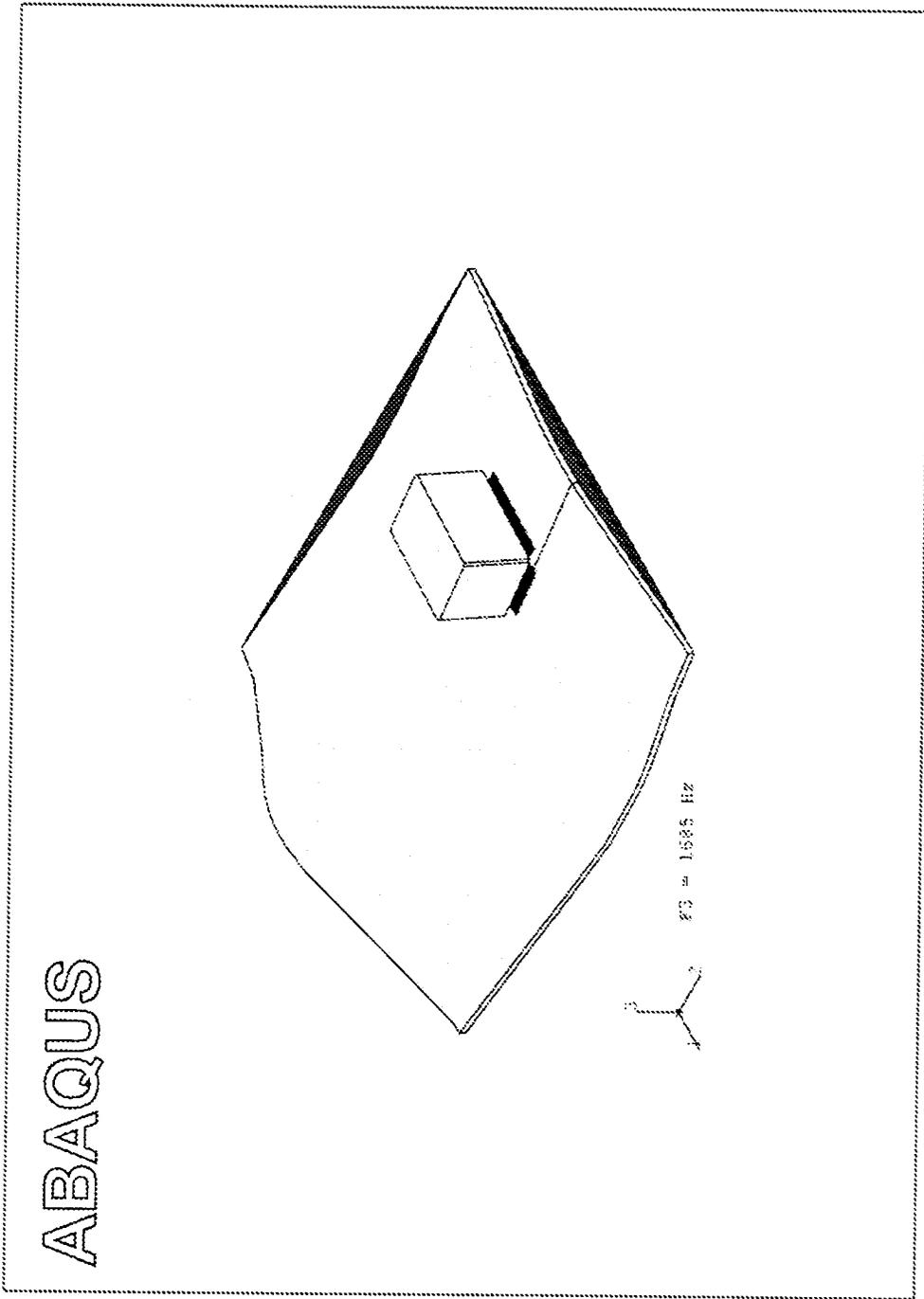
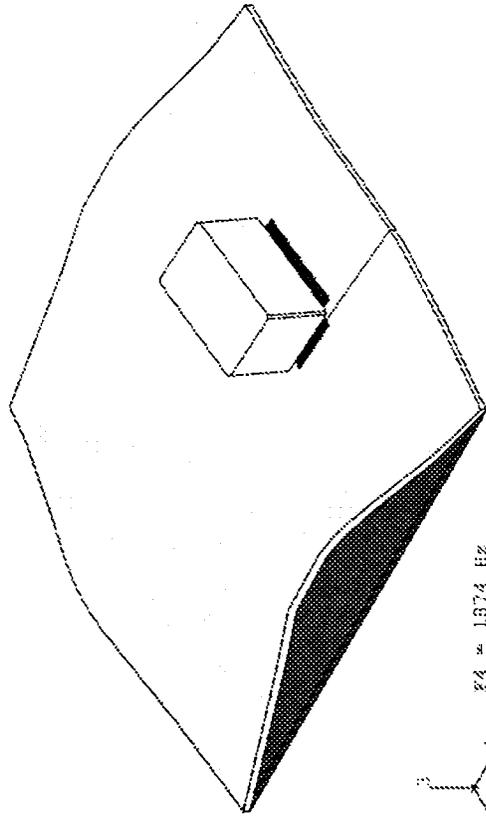


Fig. 1c

ABAQUS



F4 \* 1574 Hz

Fig. 1

ABAQUS



ABAQUS

11/11/11

1

11/11/11

# ABAQUS

