



**NASA John H. Glenn Research Center  
at Lewis Field**



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## **Packaging Technology for 500°C SiC Microsystems**

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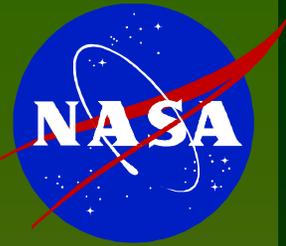


# Packaging Technology for 500°C SiC Microsystems



## Outline

- Background: motivations
- Electrical and mechanical characterization facilities
- Thick-film metallization based electrical interconnections
  - Validation results
- 500°C operable low electrical resistance die-attach
  - Method and evaluation results
- Summary
- High temperature MEMS packaging
  - Thermal mechanical stability of die-attach
- Acknowledgements

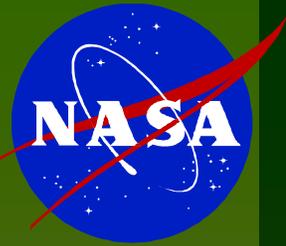


# Packaging Technology for 500°C SiC Microsystems



## Background

- 500°C operable sensors/electronics have many applications in NASA aerospace missions
  - Sensors/electronics for combustion monitoring and control
    - ❖ Pressure sensor, gas chemical sensor, and flow sensor for aeronautic engine diagnosis and control
  - Sensors/electronics for space probes to inner solar planets
    - ❖ Atmosphere profile for Venus
- SiC - excellent high temperature semiconductor
- SiC electronic devices/sensors/MEMS demonstrated ~ 600°C, most in test probe station
  - Systematically validated packaging technology for  $T > 350^{\circ}\text{C}$  not available
- 500°C device packaging technology needed
  - *In situ* device testing and commercialization

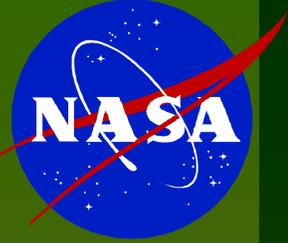


# Packaging Technology for 500°C SiC Microsystems



## NEPP High Temperature SiC Packaging Project

- Collaborating efforts between NASA, industry, university
  - GRC: Material selection, package design and fabrication, testing, SiC device
  - JPL: NDE of die-attach
  - MSFC: Engine test
  - UTRC: Dynamic thermal environment tests, FEA evaluation
  - CWRU: Assistance in fabrication

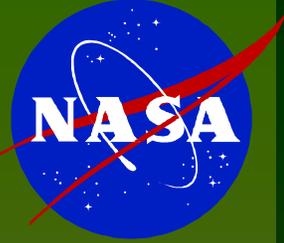


# Packaging Technology for 500°C SiC Microsystems



## High Temperature SiC Microsystem Packaging

- Electrical interconnection system
  - 500°C operable substrates
    - Ceramics:  $\text{Al}_2\text{O}_3$  and AlN
  - 500°C operable electrical interconnection
    - Precious metal thick-film metallization
    - Au wire-bond
  - Conductive die-attach
    - Conductive, low electrical resistance
    - Thermal mechanical stability
- Mechanical system
  - Thermal mechanical reliability of die-attach

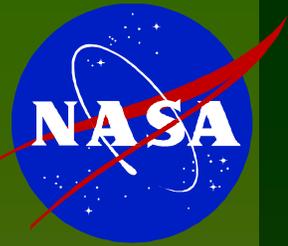


# Packaging Technology for 500°C SiC Microsystems



## Test Facilities

- Testing systems for 500°C packaging materials/  
components tests
  - Electrical/electronic tests
    - Computerized
    - Simultaneous measurement of multi-parameters for  
multi-samples
    - Temperature programming
  - Mechanical/materials tests
    - Die shear ( $T_R - 500^\circ\text{C}$ ) and die tensile ( $T_R$ )
    - Wire loop test ( $T_R$ , 500°C later this year)

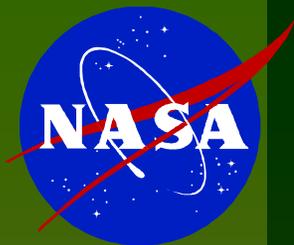


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## Au Thick-film Based Interconnections

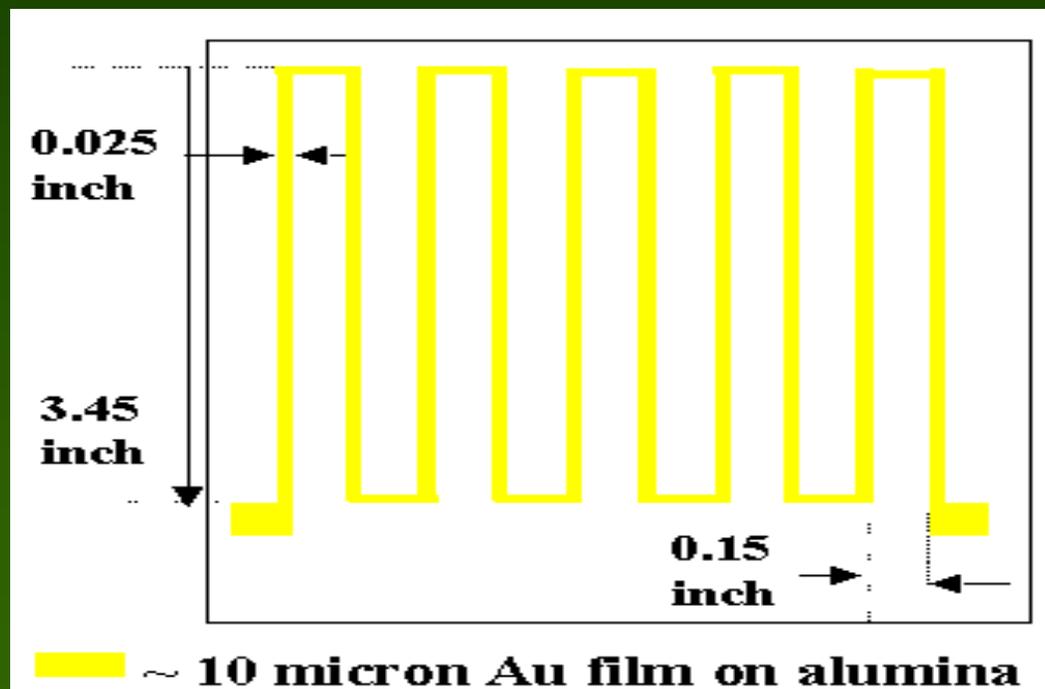
- Au based thick film metallization
  - Screen-printed thick-film wire/pads
  - Good adhesion to various ceramic substrates
  - Stable in corrosive ambience at high temperatures
  - Au thin wire-bond
- Printed thick-film wire/pad and Au wire-bond
- Tested at 500°C with electrical bias

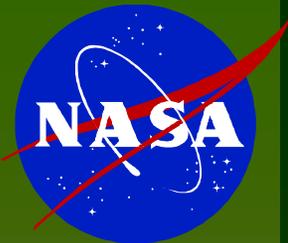


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## Thick Film Based Interconnections

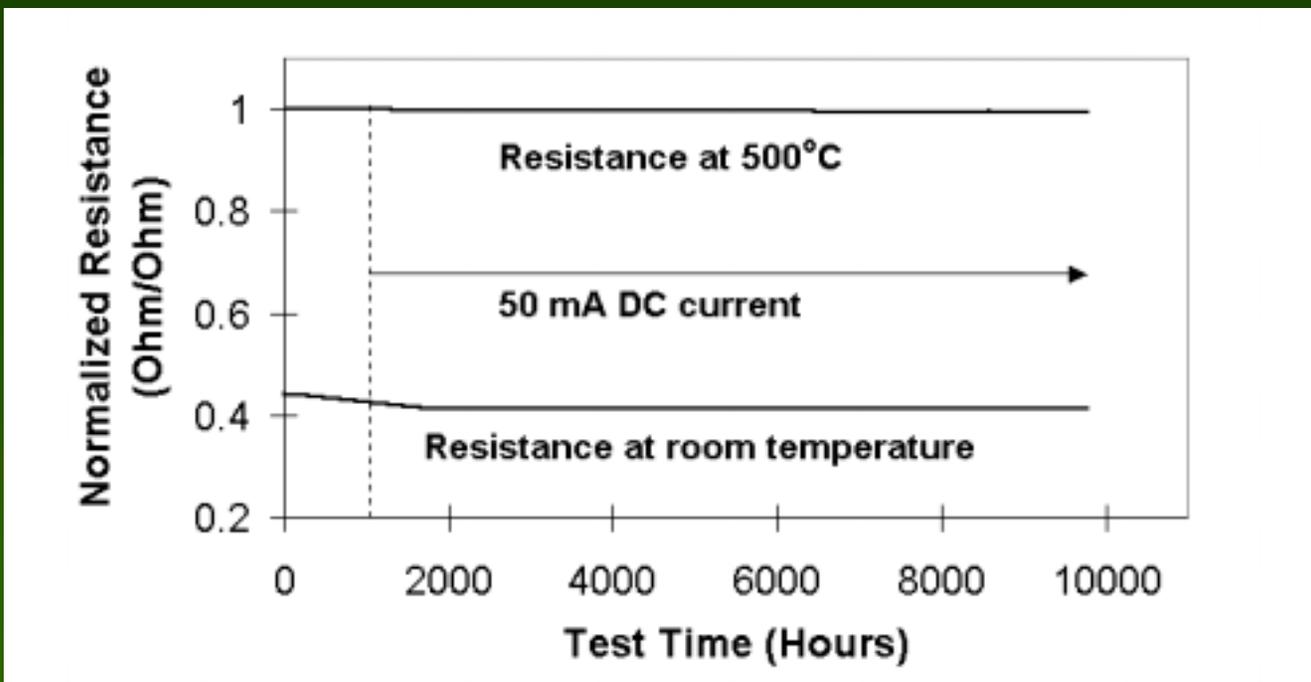


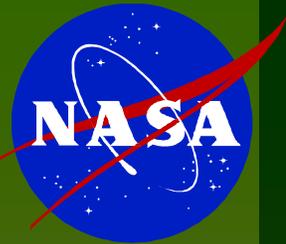


# Packaging Technology for 500°C SiC Microsystems



## Thick Film Printed Wire

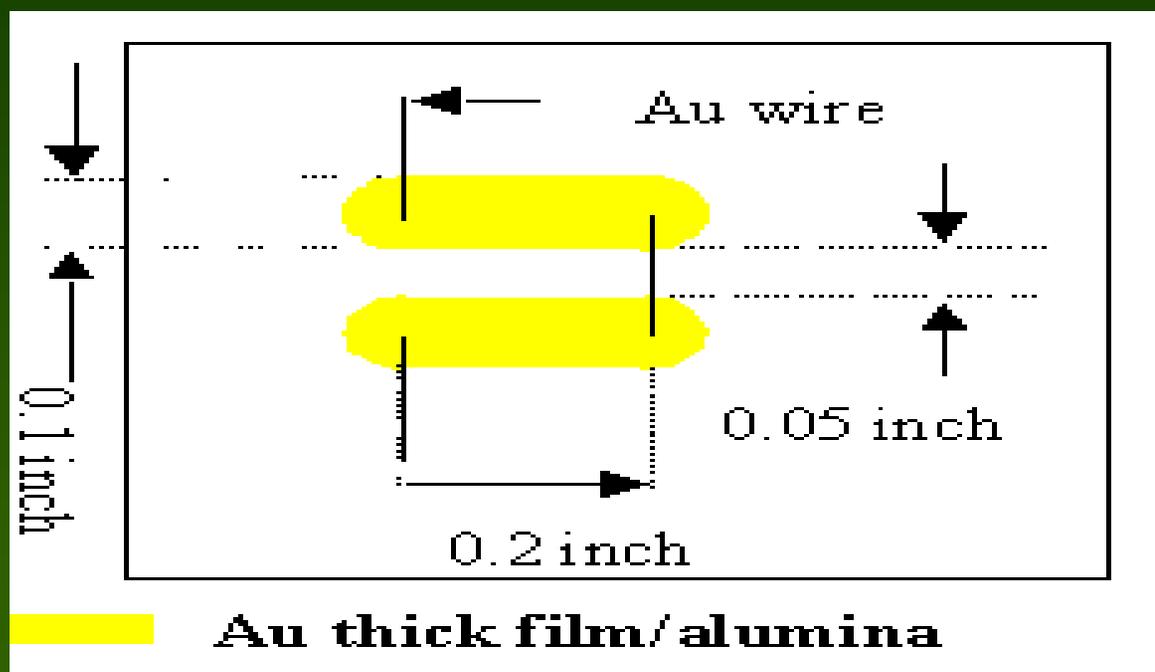




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## Thick Film Based Interconnections



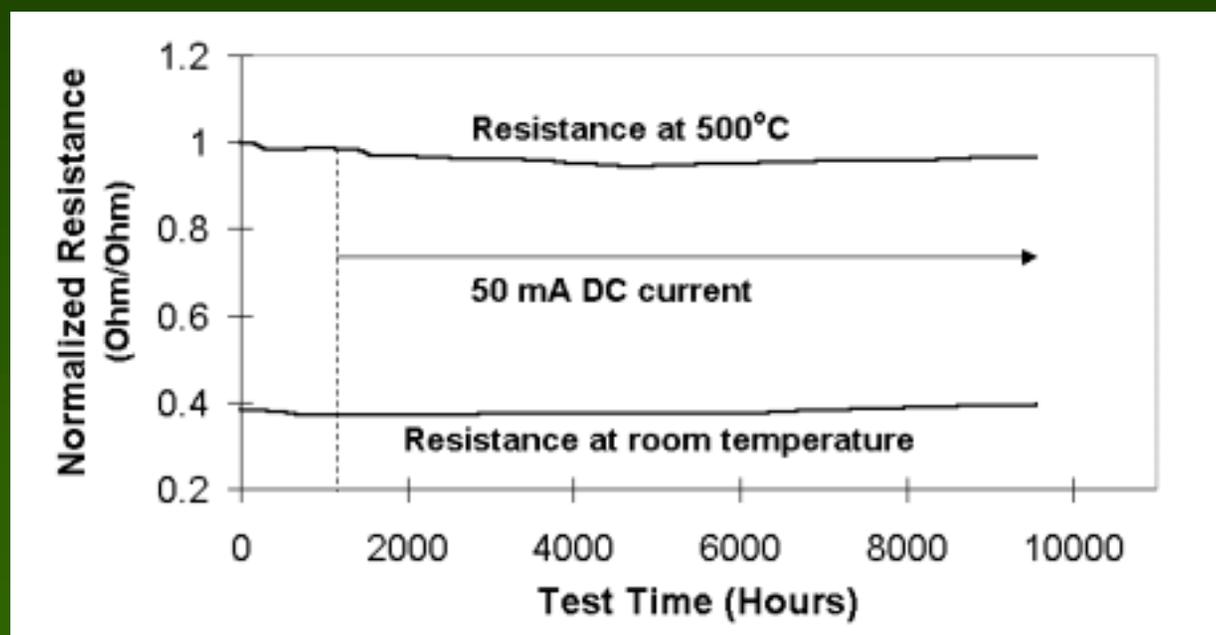
Unit Circuit

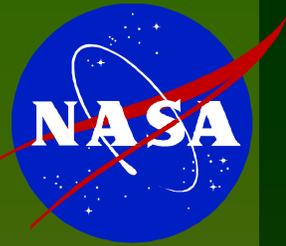


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## Thick-Film Metallization Based Au Wirebond



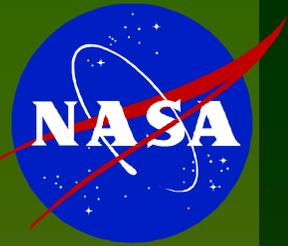


# Packaging Technology for 500°C SiC Microsystems



## Conductive Die-attach

- SiC test device
  - Backside: Ni/4H-SiC ohmic contact after annealing at high temperature in Ar
  - Front-side: Au/Ti/4H-SiC **rectifying** contact
- Au thick-film used as conductive attaching material
  - Two steps process allowing low curing temperature
- AlN substrate: high thermal conductivity and a CTE matches SiC

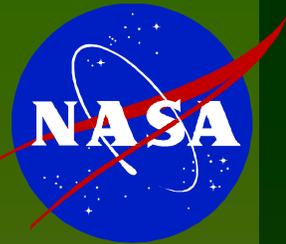


# Packaging Technology for 500°C SiC Microsystems



## Optimized Die-Attach Process

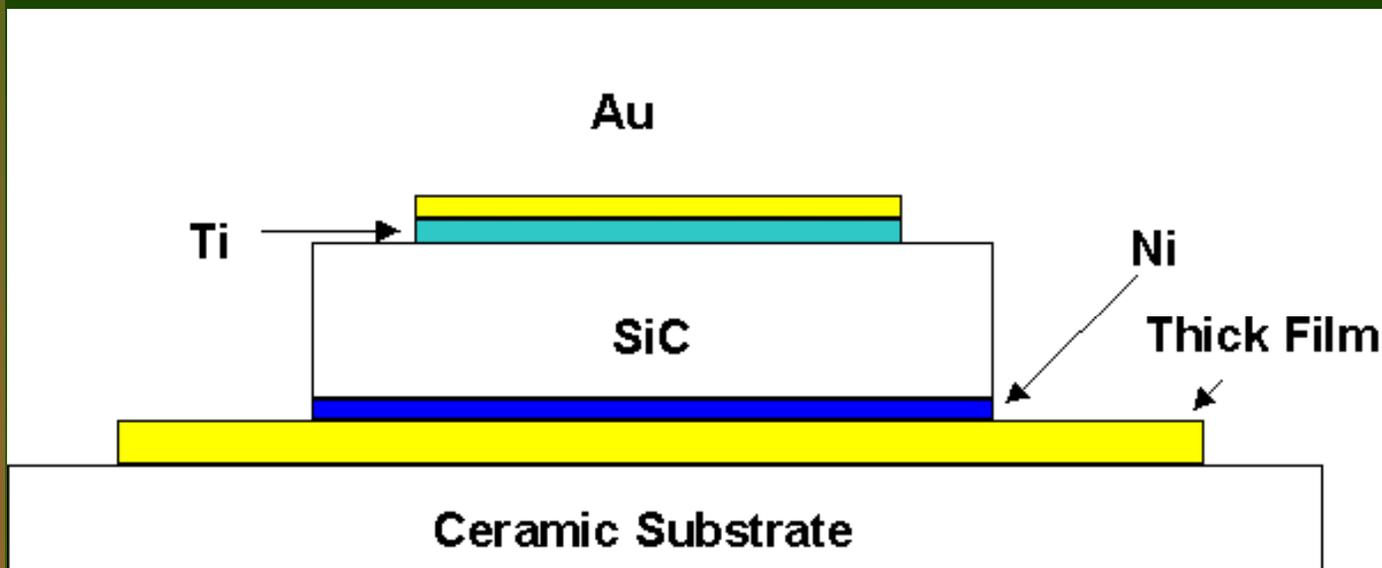
- Thick film suggested be cured at 850°C
  - Best bonding to ceramic substrates
- 850°C may not be comfortable to die
- Optimize thick-film process for die-attach
- Scanning Electron Microscopy (SEM) and Auger Electron Spectroscopy (AES) were used to study the thick film surfaces cured at various temperatures

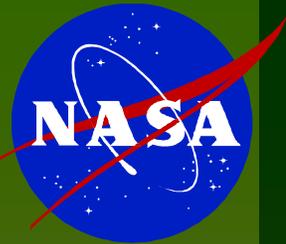


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## Conductive Die-attach Structure





# Packaging Technology for 500°C SiC Microsystems



## Two-Step Thick Film Process

- AES results indicate
  - High curing temperature ( $\sim 850^{\circ}\text{C}$ ) preferred for binder migration to Au/ceramic interface
- SEM results indicate
  - Coherent thick film formation at  $\geq 600^{\circ}\text{C}$
- Best adhesion and low temperature exposure to die
  - First screen-printed layer cured at  $850^{\circ}\text{C}$
  - Die attached at  $600^{\circ}\text{C}$  with minimal amount of thick film materials



# Packaging Technology for 500°C SiC Microsystems

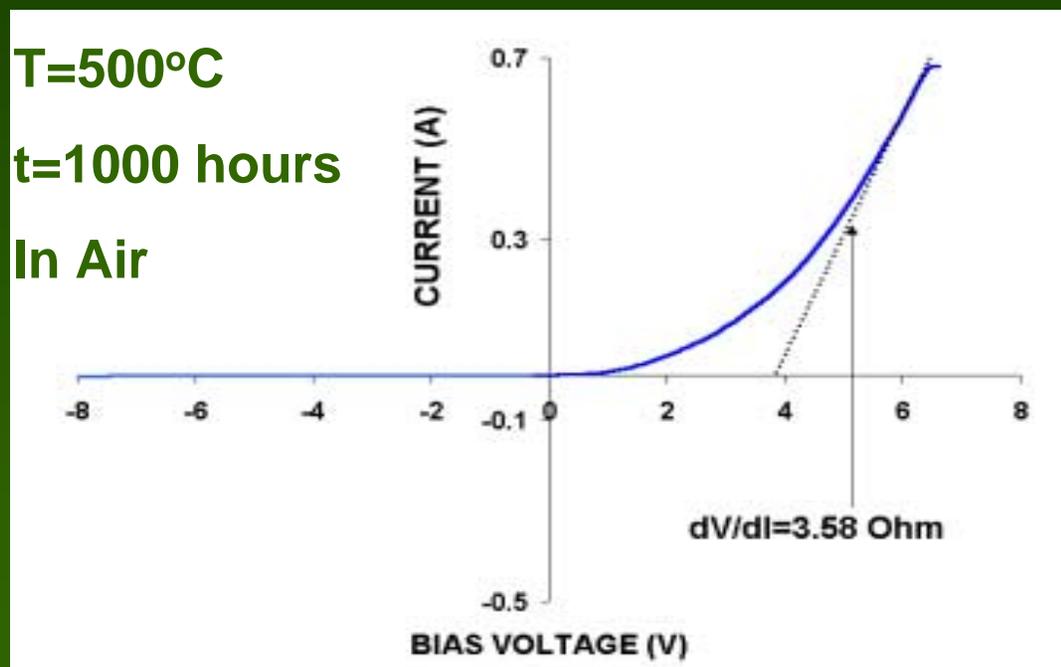


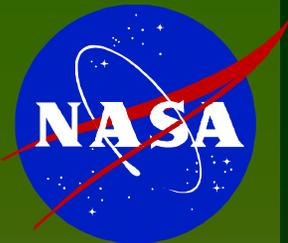
## I-V Curve of an Attached SiC Diode at 500°C

**T=500°C**

**t=1000 hours**

**In Air**

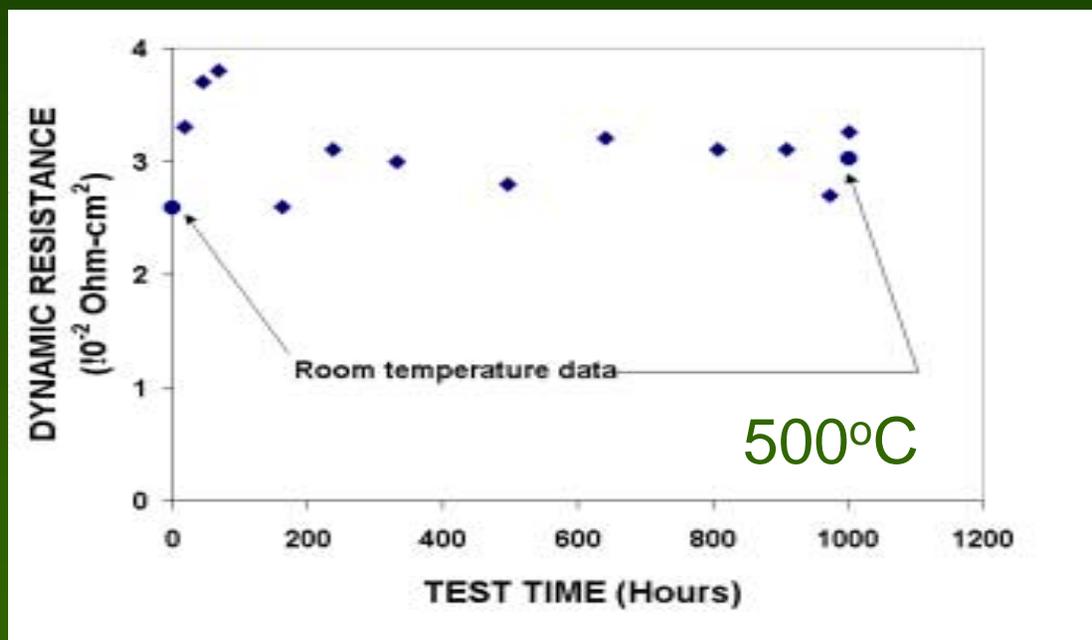


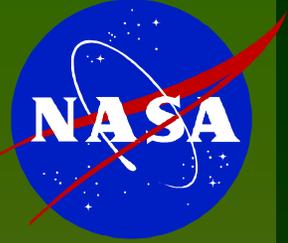


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## Dynamic Resistance of Attached SiC Diode



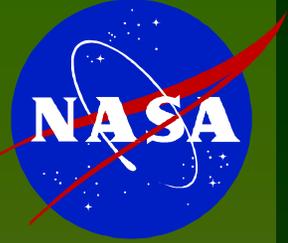


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## Test Results

- Attached SiC test chip
  - Diode I-V curves characterized at both  $T_R$  and 500°C
  - Dynamic resistance of I-V curves indicated die-attach resistance less than  $3.5 \times 10^{-2} \Omega \text{ cm}^2$  at  $T_R$  and 500°C tested for over 1000 hours
  - Sufficient shear strength measured at  $T_R$
- Thick-film based interconnections validated at 500°C
  - Thick film printed wires stable at  $T_R$  - 500°C, with/ without 50mA DC, for ~10000 hours.
  - Thick film metallization based wire bond stable at  $T_R$  - 500°C, with/ without 50 mA DC, for ~10000 hours.



# Packaging Technology for 500°C SiC Microsystems



## 500°C Chip Level Package

- AlN and Al<sub>2</sub>O<sub>3</sub> substrates
- Au thick-film metallization based wire-bond
- Au thick-film based low resistance conductive SiC die – attach scheme
- T<sub>R</sub> - 500°C operable
- Tested in oxidizing environment
- Basic elements electrically tested at T<sub>R</sub> - 500°C for ~10000 hours
- Packaging HT SiC sensors and circuits



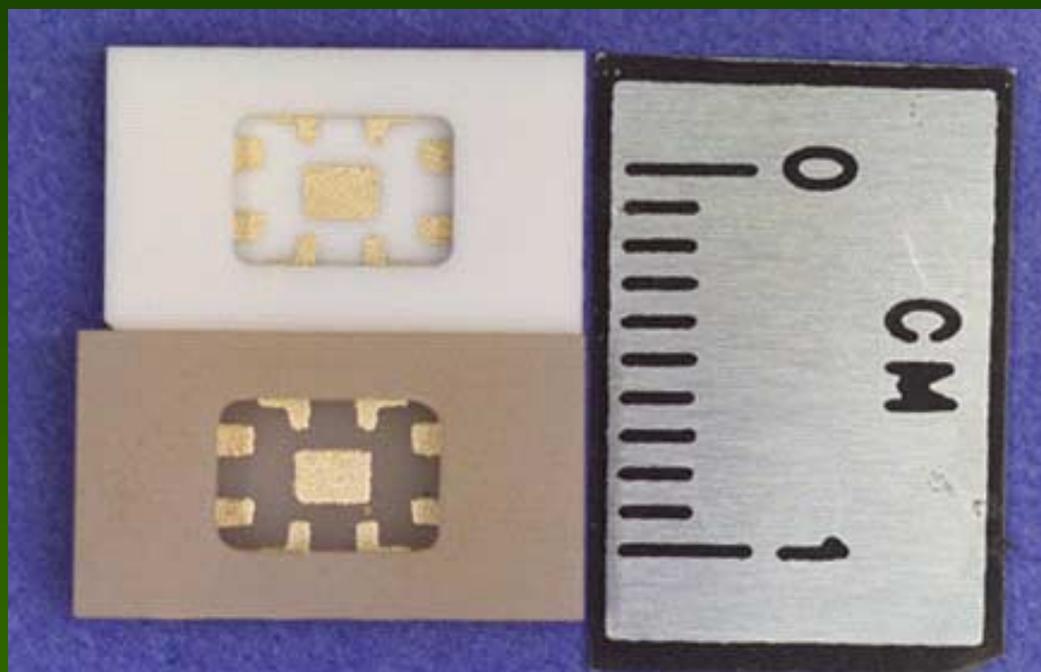
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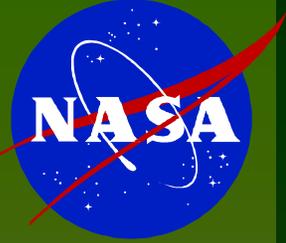


## High Temperature Chip Level Package

$\text{Al}_2\text{O}_3$  based

AlN based



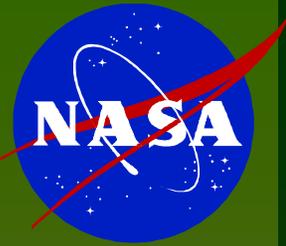


# Packaging Technology for 500°C SiC Microsystems



## Summary

- AlN and 96% Al<sub>2</sub>O<sub>3</sub> selected as substrates
- Au thick-film based interconnections validated at T<sub>R</sub> and 500°C for ~10000 hours with/without DC bias
- Au thick-film based conductive SiC die-attach scheme evaluated for 500°C operation
- Attached SiC diode electrically tested at 500°C for >1000 hours in oxidizing environment
  - The upper limit of die-attach resistance < 3.5\*10<sup>-2</sup> Ω-cm<sup>2</sup> at both T<sub>R</sub> and 500°C



# Packaging Technology for 500°C SiC Microsystems



## High Temperature MEMS Packaging

- Wide operation temperature range
  - ❖  $T_R - 500^{\circ}\text{C}$
- MEMS devices are sensitive to thermal mechanical stress
  - ❖ Device mechanical operation
  - ❖ CTE mismatch of die-attach materials
- Non-electrical interactions between the device and environment
  - ❖ Chemical, mechanical, magnetic, optical
- Thermal mechanical optimization of die-attach is critical to the reliability of packaged devices



# Packaging Technology for 500°C SiC Microsystems



## Acknowledgements

- 2<sup>nd</sup> NEPP Annual Conference Committee
- Thick-film test samples fabricated in Case Western Reserve University
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