

# SSB-1: GUIDELINES FOR USING PLASTIC ENCAPSULATED MICROCIRCUITS AND SEMICONDUCTORS IN MILITARY, AEROSPACE AND OTHER RUGGED APPLICATIONS

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## INTRODUCTION

The military and aerospace electronics industries are experiencing an ever increasing demand for the use of plastic encapsulated microcircuits and semiconductors. While plastic encapsulated microcircuits and semiconductors offer a number of inherent advantages over hermetically sealed ceramic packages, uncontrolled use can introduce a number of technical risks in military and aerospace equipment applications that are not associated with hermetic packaged devices.

The G-12 Solid State Device Committee of the Government Electronics & Information Technology Association (GEIA) developed guidelines for assessing the suitability of plastic encapsulated microcircuits and semiconductors for use in military, aerospace and other rugged applications. EIA Engineering Bulletin *SSB-1, Guidelines for Using Plastic Encapsulated Microcircuits and Semiconductors in Military, Aerospace and Other Rugged Applications* provides:

- Methods for selecting the most suitable device for the application from both an equipment performance and economic perspective
- Means to emulate commercial buying practices by drawing upon qualification and reliability evaluation methods applied by the microelectronics design and manufacturing industry

SSB-1 presently includes four annexes that describe the reliability assessment method, including supporting technical rationale.

- *SSB-1.001 Qualification and Reliability Monitors* recommends minimum qualification and monitoring testing of plastic encapsulated microcircuits and discrete semiconductors.
- *SSB-1.002 Environmental Tests and Associated Failure Mechanisms* provides more detailed information concerning the environmental stresses associated with qualification and reliability monitor tests and the specific failures induced by these environmental stresses.
- *SSB-1.003 Acceleration Factors* provides reference information concerning acceleration factors commonly used by device manufacturers to model failure rates in conjunction with statistical reliability monitoring
- *SSB-1.004 Failure Rate Estimating* provides reference information concerning methods commonly used by the semiconductor industry to estimate failure rates from accelerated test results.

This paper presents the reliability assessment methodology described in SSB-1.

## FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING

Failure-Mechanism-Driven Reliability Monitoring draws upon the concepts and implementation of line controls, process stability and effective monitoring programs in lieu of qualifying a product based solely on a fixed list of tests. A supplier must identify those failure mechanisms that may be actuated through a given product / process change(s), and design and implement reliability tests adequate to assess the impact of those failure mechanisms on system level reliability. In order for this to be effective, the supplier establishes a thorough understanding and linkage to their reliability monitoring program. Statistical Reliability Monitoring (SRM) is a statistically based methodology for monitoring and improving reliability involving identification and classification of failure mechanisms, development and use of monitors, and investigation of failure kinetics allowing prediction of failure rate at use conditions. Failure kinetics are the characteristics of failure for a given physical failure mechanism, such as the acceleration factor, derating curve, activation energy, median life, standard deviation, characteristic life, instantaneous failure rate, etc.

The failure rate of semiconductor devices is inherently low. As a result, the semiconductor industry uses a technique called acceleration testing to assess device reliability. Elevated stresses are used to produce the same failure mechanisms as would be observed under normal use conditions, but in a shorter time period. Acceleration factors are used by device manufacturers to estimate failure rates based on the results of accelerated testing. The objective of this testing is to identify these failure mechanisms and eliminate them as a cause of failure during the useful life of the product.

## ACCELERATION TESTING AND FAILURE MECHANISMS

The following describes tests frequently used in statistical reliability monitoring (SRM) activities for plastic encapsulated microcircuits and semiconductors and identifies the potential failure mechanisms monitored by these tests. This discussion does not include all of the tests typically included in device qualification and reliability monitoring, but focuses on those tests specifically designed to apply to (or have unique implications for) plastic encapsulated microcircuits and semiconductors. EIA JESD-47 Stress-Test-Driven Qualification of Integrated Circuits includes a complete set of reliability stress tests used by the semiconductor industry for qualifying new or changed products.

### *Preconditioning of Surface Mount Devices (EIA JESD-22-A113)*

The advent of surface mount devices (SMDs) introduced a new class of quality and reliability concerns regarding package cracks and delamination. Moisture from atmospheric humidity will enter permeable packaging materials by diffusion and preferentially collect at the dissimilar material interfaces. Assembly processes, used to solder SMDs to printed circuit boards (PCBs), will expose the entire package body to temperatures higher than 200°C. During solder reflow, the combination of rapid moisture expansion and materials mismatch can result in package cracking and/or delamination of critical interfaces within the package. The solder reflow processes of concern are convection, convection/IR, infrared (IR), vapor phase (VPR), and hot air rework tools. The use of assembly processes that immerse the component body in molten solder are not recommended for most SMD components.

IPC/JEDEC J-STD-033, Standard for Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices, describes the standardized levels of floor life exposure for moisture/reflow-sensitive SMDs. This standard also includes handling, packing and shipping requirements necessary to avoid moisture/reflow-related failures. These methods are provided to avoid damage from moisture absorption and exposure to solder reflow temperatures that can result in yield and reliability degradation. By using these procedures, safe and damage-free reflow can be achieved, with the dry packing process, providing a minimum shelf life capability in sealed dry-bags of 12 months from the seal date.

JESD22-A113, Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing, is an industry standard preconditioning flow for nonhermetic SMDs that is representative of a typical industry multiple solder reflow operation. The semiconductor manufacturer should subject these SMDs to the appropriate preconditioning sequence of this test method prior to specific in-house qualification and reliability monitoring to evaluate long term reliability which might be effected by solder reflow.

### *Bias Life Test (EIA JESD-22-A108)*

This test is performed to determine the effects of bias conditions and temperature on solid state devices over an extended period of time. A device is defined as a failure if the parametric limits are exceeded or if functionality cannot be demonstrated under nominal and worst-case conditions.

### *Temperature Cycling (EIA JESD-22-A104)*

Temperature cycling tests the durability of a package undergoing extreme temperature variations over a given period of time. Temperature is usually varied about a mean value with a constant ramp rate followed by a dwell period. This test exposes the package to mechanical stress and accelerates failure modes associated with differing coefficients of thermal expansion between die and encapsulant materials. The dwell period is important because it allows the part to reach thermal equilibrium and for stress relaxation to occur. To conduct a temperature cycling test, a temperature-controlled environmental chamber and a heating unit and cryogenic cooling unit with the ability to meet the ramp rate specifications are required. At the end of the test, the package is tested electrically and examined visually to identify areas of failure.

Failure mechanisms targeted by this test include die cracking, shorts and opens on die, passivation cracks/fracture, voids in die attach, plastic package fracture/cracks, wirebond pad cratering, excessive intermetallics in wirebonds, poor solder joints.

### *Autoclave (EIA JESD-22-A102)*

Autoclave is an environmental test that measures device resistance to moisture penetration and the resultant effects of galvanic corrosion. It is a highly accelerated and destructive test. Conditions employed during the test include 121°C, 100% relative humidity, and 15 psig. Minimum test duration is typically 96 hours. Failure mechanisms targeted by this test include metallization corrosion, moisture ingress and delamination.

Disadvantages of autoclave testing lie in the fact that contaminants in the chamber can induce failures that are not representative of device reliability.

### *Temperature Humidity Bias (EIA JESD-22-A101)*

The Temperature Humidity Bias Life (THB) test is used to test for moisture induced failures. Compared to Highly Accelerated Stress Test (HAST) or autoclave, it requires less severe levels of temperature and relative humidity. The test requires the devices to undergo a constant temperature, elevated relative humidity, and electrical bias (constant or intermittent, based on device type). Once moisture reaches the die surface, the electric potential helps transform the device into an electrolytic cell. This in turn accelerates the corrosion failure mechanism. Electrical tests are performed after the THB stressing to detect parametric drifts associated with corrosion of susceptible parts. Failure mechanisms targeted by this test include electrolytic/galvanic corrosion, delamination, and crack propagation. Common failure sites include interfaces between lead fingers and the encapsulant, wirebonds, bondpads, and die metallization.

THB has become less useful for microcircuits in recent years due to the increased packaging quality of die; reliability tests can run thousands of hours in order to get useful results.

### *Highly Accelerated Stress Test (EIA JESD-22-A110)*

The Highly Accelerated Stress Test (HAST) is performed to evaluate the non-hermetic packaging of solid state devices in humid environments. This test uses a high temperature (usually 130°C), high relative humidity (about 85%), under high atmospheric pressure conditions (up to 3 atm) to accelerate the penetration of moisture through the external protective material or at the seals around the chip leads. Once moisture reaches the die surface (as described for THB), the electric potential helps transform the device into an electrolytic cell. This in turn accelerates the corrosion failure mechanism. This test is intended to precipitate failure mechanisms associated with metallization corrosion, delamination at material interfaces, wirebond failures, and reduced insulation resistance. One should exercise caution when evaluating results of HAST tests performed at temperatures higher than 130°C. Such tests can precipitate different failure mechanisms that would not be seen during normal device operation.

HAST was developed especially for plastic encapsulated solid state devices after it became evident that autoclave and THB tests were no longer generating failures among certain robust PEMS. HAST detects failure mechanisms similar to those detected by THB, but at a greatly accelerated rate. Some device manufacturers substitute HAST testing for THB based on comparisons between lots

with known moisture sensitivity and verifying that failures were due to the same failure mode. Acceleration factors are then applied to derive equivalent THB failure results from HAST test results.

## ACCELERATION FACTORS

This following discussion addresses acceleration factors commonly used by device manufacturers to model failure rates in conjunction with in statistical reliability monitoring (SRM). These acceleration factors are frequently used by OEMs in conjunction with physics of failure reliability analysis to assess the suitability of plastic encapsulated microcircuits and semiconductors for specific end use applications.

### Thermal Effects (Arrhenius)

$$A_f = \exp\left[\frac{E_a}{k} \cdot \left(\frac{1}{T_u} - \frac{1}{T_t}\right)\right]$$

$A_f$  = acceleration factor

$E_a$  = activation energy, typical value for a given failure mechanism or derived from empirical data

$k$  = Boltzman's Constant ( $8.6171 \times 10^{-5}$  eV)

$T_u$  = use environment junction temperature (in °K)

$T_t$  = test environment junction temperature (in °K)

The Arrhenius Life-Temperature Relationship [1] is widely used to model product life as a function of temperature. This relationship is used to express both a single failure mechanism's sensitivity to temperature and a product's thermal acceleration factor. When used to estimate the reliability of a product, the form above is used to express that product's reliability with respect to temperature and as a function of time. Device manufacturers use the Arrhenius equation to derive acceleration factors for High Temperature Operating Life, High Temperature Steady State Life and Data Retention (for non-volatile memory devices) from this equation.

Time-to-failure estimates using the Arrhenius equation are very sensitive to the activation energy value. For example, the effect of a 0.05eV variation in activation energy on time-to-failure at 70°C is:

$$t_f = \frac{\exp^{(E_a+0.05)/kT}}{\exp^{E_a/kT}} \approx 5$$

EIA/JEP122, Failure Mechanisms and Models for Silicon Semiconductor Devices, describes the basic thermal acceleration equation in detail and provides guidance in selecting thermal activation energies used to estimate system failure rates for the Sum-of-the-Failure-Rates Method. EIA/JEP122 includes a single value for each as a worst-case likely value for use as an industry suggestion to provide consistency and comparisons.

The following table, from EIA/JEP122, is a first order listing of thermal activation energies assigned to general classifications of failure mechanisms applicable to microcircuits. If one has only superficial knowledge of the physical processing employed and has no other way of obtaining the characteristics of the failure mechanism, but knows that the failure falls under one of the categories on this table, then the selection of the typical value for thermal activation energy will provide the basis for a reasonable

estimate of that failure mechanism's effect on the microcircuit failure rate. If one has more knowledge of the specific process and material used, EIA/JEP122 includes more detail to some of the specific materials and processes listed here.

## First Order Activation Energies

General Failure Mechanism Class	Typical (eV)	
Surface / Oxide	1.0	
Charge Loss (dynamic memory)	0.6	
Dielectric Breakdown	Field > 0.04 micron thick	0.3
	Field ≤ 0.04 micron thick	0.7
Metallization	Electromigration (Aluminum, alloys, and multi-layer aluminum)	0.6
	Corrosion – Chlorine	0.70
	Corrosion – Phosphorus	0.53
Wafer Fabrication	Chemical contamination	1.00
	Silicon / crystal defects	0.50

### Non-Volatile Memory Data Retention

One should exercise caution where the Arrhenius Life-Temperature Relationship is used to derive acceleration factors for data retention time-to-failure. Based on the work of DeSalvo et al [2], the Arrhenius relationship does not give the proper relationship for data retention life versus temperature. The Arrhenius relationship generally defines the rate of diffusion as a function of temperature. Since many failure mechanism in semiconductor devices are attributed to the effect of mobile ions, the Arrhenius relationship provides a good model for calculating the acceleration of these affects due to increased temperature, and visa versa, relating observed failure rates at high temperatures to expected life times at lower temperatures.

DeSalvo et al argue that the Arrhenius relationship does not properly model data retention in floating-gate non-volatile memory devices, because the data loss is due to charge loss, which obeys the Fowler-Nordheim transport. Cogent analysis of historical data demonstrates how the newly proposed "T-Model" fits existing data. The Arrhenius model, however, is shown to require different activation energies to fit the data at different test temperatures. Choosing the wrong activation energy for a given temperature can drastically exaggerated results.

The data retention time-to-failure using the "T-Model" is calculated by the equation:

$$t_R = t_0 \cdot \exp\left(-\frac{T}{T_{0DR}}\right)$$

$t_R$  = data retention time to failure

$t_0$  = data retention time in reference conditions

$T$  = temperature

$T_{0DR}$  = data-retention characteristic temperature

We can derive the acceleration factor to extrapolate data retention time-to-failure as follows:

$$A_f = \frac{t_{Ru}}{t_{Rt}} = \frac{t_0 \cdot e^{-\left(\frac{T_u}{T_0}\right)}}{t_0 \cdot e^{-\left(\frac{T_t}{T_0}\right)}} = e^{\left(\frac{T_t - T_u}{T_0}\right)}$$

### Voltage Acceleration for Microcircuits

A voltage acceleration factor [3] is often used in combination with the Arrhenius relationship for failure mechanisms which are known to be accelerated by voltage (i.e. time dependent dielectric breakdown, gate oxide defects, charge gain, etc.):

$$A_{fv} = \exp[\beta \cdot (V_t - V_u)]$$

$V_t$  = Test Voltage

$V_u$  = Use Voltage

$\beta$  = Voltage Acceleration Constant (empirically derived)

An overall acceleration factor is derived from the product of the Arrhenius Life-Temperature Relationship and voltage acceleration factor:

$$A_{ftv} = A_{ft} \cdot A_{fv}$$

### Temperature - Humidity Effects (Hallberg - Peck)

$$A_f = \left(\frac{RH_t}{RH_u}\right)^3 \cdot \exp\left[\frac{E_a}{k} \cdot \left(\frac{1}{T_u} - \frac{1}{T_t}\right)\right]$$

$A_f$  = acceleration factor

$RH_u$  = use environment relative humidity

$RH_t$  = test environment relative humidity

$E_a$  = activation energy, 0.90eV

$k$  = Boltzman's Constant (8.6171 x 10<sup>-5</sup> eV)

$T_u$  = use environment junction temperature (in °K)

$T_t$  = test environment junction temperature (in °K)

This equation is often used to estimate acceleration factors for temperature-humidity and bias effects when applied to HAST test results, and for temperature-humidity effects when applied to autoclave (unbiased). This model is also used for HAST testing performed without bias, a condition preferred by some users to approximate dormant storage under a variety of long term storage conditions. Peck [4] described a relationship between temperature, humidity and life for electrolytic corrosion of aluminum metallization. Peck concluded that this relationship allows the establishment of very-short-time tests to replace 1000-hour Temperature Humidity Bias (THB) testing and suggested using this relationship to extrapolate autoclave test results. This relationship has the following form.

$$t_t = A \cdot (\%RH)^n \cdot \exp\left(\frac{E_a}{kT}\right)$$

where  $t_t$  is time-to-failure,  $n = -2.66$ ,  $E_a = 0.79\text{eV}$ ,  $A$  is a constant (the temperature humidity failure rate in reference conditions)

Subsequent to this study, Hallberg and Peck [5] found that data taken from several publications optimally fit this equation with  $n = -3.0$  and  $E_a = 0.90\text{eV}$ . Recent studies indicate that some devices have higher activation energies associated with temperature-humidity effects. Tam [6], for example, found better correlation with  $E_a = 0.95\text{eV}$  from his own test results for one specific device. The use of  $E_a = 0.90\text{eV}$  is most common and, therefore, generally recommended except where a device manufacturer may have empirical data to substantiate a higher activation energy for specific devices.

Hallberg and Peck concluded that HAST testing should replace THB in order to improve feedback as well as shipment times, and that moisture life extrapolation from THB can be accomplished from the following equation.

$$A_f = \left(\frac{0.85}{RH}\right)^3 \cdot \exp\left[10,444 \cdot \left(\frac{1}{[T + 273]} - \frac{1}{358}\right)\right]$$

where  $T$  is in °C,  $RH$  is in % and  $E_a = 0.90\text{eV}$

This equation may also be applied when extrapolating autoclave (unbiased) test results.

One should exercise caution when evaluating results of HAST tests performed at very high temperatures. Such tests can precipitate different failure mechanisms that would not be seen during normal device operation. Sinnadurai [7] advocated an upper limit of 130°C for the validity of HAST testing of PEMS. In an extreme example, Sinnadurai argues that at 140°C and 100% RH the polymer of a plastic package would progressively de-bond and the exterior terminations of the package would suffer electrolytic damage. The JEDEC standard test method, JESD22-A110, includes test conditions of 110°C at 85% RH and 130°C at 85% RH. Further, JESD22-A110 cautions that moisture reduces the effective glass transition temperature of the molding compound and that stress temperatures above the effective glass transition temperature may lead to failure mechanisms unrelated to standard 85°C/85% RH stress.

Brizoux, et al [8], of Thompson-CSF derived a model for temperature and humidity effects. Though the use of this model is not widely reported, it is presented here for completeness. This model is based on Peck's law and the Thompson-CSF functional failure model, which assumes temperature and power supply voltage conditions activate functional failures. In contrast to Hallberg's and Peck's work, Thompson-CSF found that temperature-humidity acceleration can be represented by Peck's law, with  $n = -2.66$  and  $E_a = 0.7\text{eV}$ . Using the reference conditions of 55°C junction temperature, 50% relative humidity and voltage at nominal + 10%, the Thompson-CSF model is expressed in the following form.

$$A_f = \exp\left[\frac{0.7}{k} \cdot \left(\frac{1}{T_j} - \frac{1}{328}\right)\right] \cdot \left(\frac{RH_j}{50}\right)^{2.66} \cdot \exp(V - 1.1V_n)$$

$A_f$  = acceleration factor

$T_j$  = junction temperature (in °K)

$k$  = Boltzman's Constant

$RH_j$  = relative humidity at the die surface

$V$  = power supply voltage

$V_n$  = nominal power supply voltage

where  $T_j = T_a + \theta_{ja}P$  ( $T_a$  is ambient temperature,  $\theta_{ja}$  is junction to ambient thermal resistance,  $P$  is dissipated power)

Bias effects are incorporated in this model. When there is no bias, or when test voltage equals the nominal voltage for the device, this portion of the equation goes away. This model also addressed the notion that during operating conditions, the relative humidity at the die surface ( $RH_j$ ) is lower than ambient relative humidity due to junction temperature heating effects. When the difference between the junction and ambient temperature increases, the die dries and the rate of acceleration decreases. Thompson-CSF models this corrective term using the following psychrometric law.

$$RH_j = RH_a \cdot \exp\left[\frac{0.43}{k} \cdot \left(\frac{1}{T_j} - \frac{1}{T_a}\right)\right]$$

where  $RH_a$  is ambient relative humidity,  $T_j$  is junction temperature (in °K) and  $T_a$  is ambient temperature (in °K)

#### Thermo-mechanical Effects (Coffin-Manson)

$$A_f = \left(\frac{\Delta T_t}{\Delta T_u}\right)^m$$

$A_f$  = acceleration factor

$\Delta T_t$  = thermal cycle temperature change in the test environment

$\Delta T_u$  = thermal cycle temperature change in the use environment

$m$  = constant, typical value for a given failure mechanism or derived from empirical data

The Coffin-Manson Relationship [9] is an effective method to model the effects of low-cycle fatigue induced by thermal stressing upon microcircuit and semiconductor package reliability. This relationship is based on the inverse power law [10] originally used to model fatigue of metals subjected to thermal cycling and has been used for mechanical and electronic components, solder and other connections, and metals fatigue life. The typical number of cycles to failure ( $N$ ) as a function of the temperature range ( $\Delta T$ ) of the thermal cycle is expressed as

$$N = A / (\Delta T)^B$$

where  $A$  is the number of cycles to failure in reference conditions and  $B$  is characteristic of the specific metal and the test method.

The acceleration factor for the Coffin-Manson Relationship is the ratio of the temperature swing under accelerated conditions to the temperature swing under service conditions, raised to the power given by a Coffin-Manson exponent ( $m = 1/B$ ) specific to each failure mechanism.

Dunn and McPherson [11] used this equation to analyze accelerated conditions for fractured-intermetallic bond and chip-out bond failures ("cratering") and derived Coffin-Manson exponents for these failure mechanisms. Blish and Vaney [12] subsequently applied

this approach to thin film cracking, failures due to passivation film cracks induced by thermal stress. Blish [13] observed from several studies that Coffin-Manson exponents for integrated circuit failure mechanisms tend to lie in one of three relatively narrow ranges:

Failure Mechanism	$m$
Ductile Metal Fatigue	~ 1 - 3
Commonly Used IC Metal Alloys & Intermetallics	~ 3 - 5
Brittle Fracture	~ 6 - 8

Blish reviewed a large number of papers in a critical fashion to extract a useful set of reliability modeling parameters in a single table. SN diagrams (Stress vs. Number of cycles to fatigue failure) from Materials Science literature were used to advantage for prediction of integrated circuit failure rates caused by cyclic thermal stresses. A number of thermal fatigue data sets were examined to infer how the Coffin-Manson exponent varies depending upon which failure mechanism is active. Some of the materials shown in this table are not relevant to integrated circuit reliability, but are presented here for historical and technical perspective. Similar failure mechanisms are grouped together.

#### Coffin-Manson Exponents

Author(s)	Mechanism	$m$
Halford	316 Stainless Steel	1.5
Morrow	316 SS, WaspAlloy, 4340 Steel	1.75
Norris, Landzberg	Solder (97Pb/3Sn) Crossing 30°C	1.9
Kotlowicz	Solder (37Pb/63Sn) Crossing 30°C	2.27
Li, Hall	Solder (37Pb/63Sn) T < 30°C T > 30°C	1.2 2.7
Mavori	Solder (37Pb/3Ag & 91Sn/9Zn)	2.4
Scharr	Cu & Leadframe Allows (TAB)	2.7
Dittmer	Al wire bonds	3.5
Dunn, McPherson	Au <sub>4</sub> Al fracture in wire bonds	4.0
Peddada, Blish	PQFP Delamination / Bonds Failure	4.2
Mischke	ASTM 2024 Aluminum Alloy	4.2
Hatanka	Copper	5.0
Blish	Au Wire Downbond Heel Crack	5.1
Egashira	ASTM 6061 Aluminum Alloy	6.7
Blish	Alumina fracture-Bubble memory	5.5
Zelenka	InterLayer Dielectric Cracking	5.5 ± 0.7
Hagge	Silicon fracture	5.5
Dunn, McPherson	Si fracture ("cratering")	7.1
Blish, Vaney	Thin Film Cracking	8.4

## Examples of Major Market Segment Environmental Ranges

Major Market Segment	Op Life	Power On (Hrs / Week)	Cycles / Day	Moisture @ Low Power	Op Temp (Ambient In Enclosure)	Storage Temp
<b>Indoor:</b> PC/ Desktop, Server, Workstation, Consumer	5 – 10 yrs	60 – 168	Env. Cycle: 1-2 Power Cycle: 2-4	30° -36°C @ 85-92% RH	0° to 40°C	-40° to 50°C
<b>Consumer Portable:</b> Notebook PCs, PDAs, Cel Phones, etc.	5 – 10 yrs	60 – 168	Env. Cycle: 2-4 Power Cycle: 4-6	30° -36°C @ 85-92% RH	-18° to 55°C	-40° to 55°C
<b>Other:</b> Automotive, Telecom switching, Unattended outside, etc.	7 – 25 yrs	20 – 168	Env. Cycle: 2-4 Power Cycle: 2-10	30° -36°C @ 85-92% RH	-55° to 125°C	-40° to 55°C

### USE CONDITION BASED RELIABILITY EVALUATION

The SEMATECH Reliability Technology Advisory Board (RTAB) developed a reliability evaluation methodology based on the use conditions a component is expected to encounter in its market applications [14]. One of the most critical steps in the process is defining environmental, lifetime and manufacturing use conditions since it provides the basis for all follow on activities that lead to establishing baseline performance. Determining the target market segment for a product establishes the use environment and lifetime appropriate for the technology.

It is important to note that semiconductor manufacturers derive baseline performance estimates for use conditions associated with their predominant market segment(s). The table, prepared by the SEMATECH RTAB, encompasses the majority of specific conditions within each major market segment. When assessing the suitability of a device for a specific application, it is essential to account for differences between the use environment and the environment the manufacturer used for reliability evaluation.

To illustrate this point, here is a specific example comparing reliability assessment results for a benign use environment versus results for a more stressful environment such as those encountered in many military, aerospace, and other rugged applications.

Upon reviewing a device manufacturer's product reliability report, we note that this manufacturer extrapolates HAST test results for temperature-humidity-bias induced failure mechanisms assuming use conditions of 70°C junction temperature and 17.6% relative humidity. For one product technology, the manufacturer publishes a failure rate estimate of 5 Failures-In-Time (FITs), or Mean-Time-To-Failure (MTTF)  $\approx$  22,500 years.

If, however, we recalculate the failure estimate for a use environment of 85°C junction temperature and 90% relative humidity (with all other elements of the failure rate calculation remaining equal), the result becomes 2431 (FITs), MTTF  $\approx$  47 years.

### FAILURE RATE ESTIMATING METHODOLOGY

The most frequently used reliability measure for semiconductor devices is the failure rate ( $\lambda$ ). For constant failure rate, the failure rate is the ratio of the number of failures to the product of the number of devices on test and the interval in hours (i.e.  $\lambda$  = number of failures / number of devices / number of test hours). The standard method for reporting long term failure rates for semiconductor devices is to express failure rate in Failures-In-Time (FITs), or the fraction of the number of failures per billion ( $10^9$ ) device-hours.

To project from a sample to the population in general, one must establish confidence intervals. The application of confidence intervals is a statement of how "confident" one is that the sample failure rate approximates that for the population. To obtain failure rates at different confidence levels, it is necessary to make use of specific probability distributions. The chi-square distribution ( $\chi^2$ ), which relates observed and expected frequencies of an event, is frequently used to establish confidence intervals. The relationship between failure rate and the chi-square distribution is as follows:

$$\lambda = \frac{\chi^2(\alpha, d.f.)}{2 \bullet A_f \bullet t} \bullet 10^9$$

$\lambda$  = failure rate (Failures-In-Time)

$\chi^2$  = chi-square function

$\alpha$  = (100 - confidence level) / 100

d.f. = (2n + 2) degrees of freedom

n = number of failures

$A_f$  = acceleration factor

t = (sample size x total test time) device-hours

When estimating failure rates, device manufacturers use acceleration factors to extrapolate acceleration test results to use conditions. The following table presents chi-square distribution functions ( $\chi^2$ ) for 60% and 90% confidence levels, those most frequently used by device manufacturers:

Chi-Square ( $\chi^2$ ) Distribution Functions			
Failures (n)	d.f. (2n+2)	Confidence Level ( $\alpha$ )	
		60%	90%
0	2	1.833	4.605
1	4	4.045	7.779
2	6	6.211	10.645
3	8	8.351	13.362
4	10	10.473	15.987
5	12	12.584	18.549
6	14	14.685	21.064
7	16	16.780	23.542
8	18	18.868	25.989
9	20	20.951	28.412
10	22	23.031	30.813
11	24	25.106	33.196
12	26	27.179	35.563
13	28	29.249	37.916
14	30	31.316	40.256

In order to derive the overall failure rate for a product, failure rates of potential failure mechanisms are estimated separately, then added together. This is known as the Sum-of-the-Failure-Rates method:

$$\lambda_{Total} = \sum \lambda_i = \lambda_1 + \lambda_2 + \dots + \lambda_n$$

where  $\lambda_{Total}$  represents the overall failure rate and  $\lambda_i$  represents the failure rate for each failure mechanism.

#### Example

In this example we will illustrate failure rate calculation for temperature-humidity-bias effects extrapolating HAST test results. Upon reviewing a device manufacturer's product reliability report, we note the following for HAST test extrapolation for temperature-humidity-bias induced failure mechanisms:

Use Condition Junction Temperature ( $T_u$ ): 70°C or 343°K

Use Condition Relative Humidity ( $RH_u$ ): 17.6%

Test Condition Junction Temperature ( $T_t$ ): 130°C or 438°K

Test Condition Relative Humidity ( $RH_t$ ): 85%

Total Device-Hours ( $t$ ): 38,102 (sample size x total test time)

Number of Failures ( $n$ ): 1

Confidence Level ( $\alpha$ ): 60%

The manufacturer uses the Hallberg - Peck model to estimate the acceleration factor for temperature-humidity-bias effects:

$$A_f = \left( \frac{RH_t}{RH_u} \right)^3 \cdot \exp \left[ \frac{E_a}{k} \cdot \left( \frac{1}{T_u} - \frac{1}{T_t} \right) \right]$$

$$= \left( \frac{0.850}{0.176} \right)^3 \cdot \exp \left[ \frac{0.9}{8.6171 \cdot 10^{-5}} \cdot \left( \frac{1}{343} - \frac{1}{438} \right) \right]$$

$$= 10,445$$

Using the table, the chi-square distribution function ( $\chi^2$ ) for one failure at a confidence level of 60% is 4.045. The failure rate estimate becomes:

$$\lambda_{th} = \frac{\chi^2(\alpha, d.f.)}{2 \cdot A_f \cdot t} \cdot 10^9$$

$$= \frac{4.045}{2 \cdot 10,445 \cdot 38,102} \cdot 10^9$$

$$= 5.082 \approx 5 \text{ FIT}$$

This corresponds to a MTTF  $\approx$  22,500 years.

Let us recalculate the failure rate estimate for a use environment of 85°C junction temperature and 90% relative humidity. This use environment results in a temperature-humidity acceleration factor of 22. If we replace the acceleration factor of 10,445 with 22 in the above equation, the failure rate becomes 2431 FIT or, MTTF  $\approx$  47 years.

#### Deriving Acceleration Test Parameters from Use Condition Parameters and Sub-System Failure Rate Requirements

One can reverse this methodology to derive test parameters necessary to achieve a specific failure rate allocation for a particular end use environment. In this example, cyclic thermal stress conditions over the anticipated product life are shown in the table.

We plan to perform Temperature-Cycling test from -55°C to 125°C ( $\Delta T_t = 180^\circ\text{C}$ ) to qualify the device for thermo-mechanically induced defects.

Using the Coffin-Manson Relationship with a conservative value for the constant ( $m = 3$ ), we estimate the number of failure free test cycles associated with each condition.

Service Conditions	Temperature Change ( $\Delta T_u$ )	Number of Cycles ( $N$ )
(a) 20 Yr. Controlled Storage	10°C	7,300
(b) 2 Yr. Uncontrolled Storage	60°C	730
(c) 90 Days Operating	60°C	90

(a): 20 Years Controlled Storage:

$$A_{fa} = \left( \frac{\Delta T_t}{\Delta T_u} \right)^m = \left( \frac{180}{10} \right)^3 = 5,832$$

$$N_{a'} = \frac{N_a}{A_{fa}} = \frac{7,300}{5,832} = 1.25$$

(b): 2 Years Uncontrolled Storage:

$$A_{fb} = \left( \frac{\Delta T_t}{\Delta T_u} \right)^m = \left( \frac{180}{60} \right)^3 = 27$$

$$N_{b'} = \frac{N_b}{A_{fb}} = \frac{730}{27} = 27.03$$

(c): 90 Days Operating:

$$A_{fc} = \left( \frac{\Delta T_t}{\Delta T_u} \right)^m = \left( \frac{180}{60} \right)^3 = 27$$

$$N_{c'} = \frac{N_c}{A_{fc}} = \frac{90}{27} = 3.33$$

The minimum number of failure free cycles in our -55°C to 125°C Temperature-Cycling test, therefore, is:

$$N_{Total} = N_{a'} + N_{b'} + N_{c'}$$

$$= 1.25 + 27.03 + 3.33 = 31.61 \approx 32$$

#### Voltage Derating for Discrete Semiconductor Devices

When estimating overall failure rates for discrete semiconductor devices, the amount of derating needs to be considered. An example would be the use of either a 200V 1A part, or a 900V 1A part in a 175V 0.5A application for a rectifier. In both cases, the junction temperature ( $T_j$ ) will be determined by the amount of current (0.5 amps), the junction to ambient thermal resistance, the nominal ambient temperature, and the forward voltage of the device. In the case of voltage, however, there is a marked difference in stress for 25V derating versus 825V derating. Other application considerations can significantly effect the amount of stress applied to a device. For example, a transient voltage suppressor (TVS) does not operate during normal assembly operation. Because of these issues, stress factors should be used in determining the effect of derating on overall failure rate.

In the case of a 200V rated device used in a 175V application, the electrical stress ratio ( $V_s$ ) is 0.875. The table shown here provides electrical stress factors for low frequency diodes [15]. Using the table, the corresponding stress factor ( $\Pi_s$ ) is  $V_s^{2.43} = 0.723$ .

In the case of a 900V rated device used in a 175V application, the electrical stress ratio ( $V_s$ ) is 0.194. Using the table, the corresponding stress factor ( $\Pi_s$ ) is 0.05.

The overall failure rate becomes:

$$\lambda = \frac{\chi^2(\alpha, d.f.)}{2 \cdot A_f \cdot t} \cdot 10^9 \cdot \Pi_s$$

Transient Suppressor, Voltage Regulator & Voltage Reference Applications	
Electrical Stress	$\Pi_s$
$V_s < .3$	0.54
$.3 < V_s \leq .4$	0.11
$.4 < V_s \leq .5$	0.19
$.5 < V_s \leq .6$	0.29
$.6 < V_s \leq .7$	0.42
$.7 < V_s \leq .8$	0.58
$.8 < V_s \leq .9$	0.77
$.9 < V_s \leq 1.0$	1.0
Other Low Frequency Diode Applications	
Electrical Stress	$\Pi_s$
$V_s \leq .3$	0.05
$.3 < V_s \leq 1$	$V_s^{2.43}$

( $V_s$  = Voltage Applied / Voltage Rated)

#### Sub-System Level Analysis

One can derive a sub-system level failure rate estimate from the cumulative failure rates for all devices in the sub-system. A complete sub-system level failure rate estimate would, of course, include other factors (e.g. derating, assembly manufacturing process, etc.) in addition to the cumulative failure rates for all components. For the purpose of this paper, however, we will confine our discussion to device level failure rate calculations discussed earlier.

Upon reviewing device manufacturers' product reliability reports for each device used in the sub-system, we note the test conditions, device-hours and number of failures from the applicable acceleration tests. We use sub-system level (e.g. circuit board) thermal analysis results to establish use condition junction temperatures ( $T_u$ ) for each device. Using the methods described earlier, we calculate the failure rates associated with each environmental effect and then derive an overall failure rate for each device. Finally, we sum the failure rates all of the devices to estimate the sub-system level failure rate. The table illustrates a sub-system level failure rate estimate.

Sub-System Analysis		Thermal Effects (Ea = 0.7)					Temperature-Humidity Effects (Rh <sub>u</sub> = 0.5)					TOTAL (α = 60)			
		T <sub>u</sub>	T <sub>t</sub>	t <sub>0</sub>	n	λ <sub>t</sub> (FIT)	T <sub>t</sub>	RH <sub>t</sub>	t <sub>0</sub>	n	λ <sub>th</sub> (FIT)	λ <sub>Total</sub> (FIT)	MTTF (Hours)	MTTF (Years)	
Octal Buffer/Driver	U36	91	165	1,900,000	0	11.146	85	0.85	814,000	0	370.447	381.621	2.62E+06	299	
Octal Buffer/Driver	U41	79	165	1,900,000	0	5.212	85	0.85	814,000	0	139.408	144.648	6.91E+06	789	
Supply Vltg Supervisor	U17	100	165	39,108,000	1	2.047	85	0.85	16,410,000	11	502.779	504.826	1.98E+06	226	
Real Time Clock	U2	90	150	1,020,000	0	37.671	85	0.85	1,100,000	0	253.314	291.007	3.44E+06	392	
Line Buffer/Driver	U103	92	165	2,600,000	0	8.658	85	0.85	1,976,000	0	165.072	173.748	5.76E+06	657	
FPGA	U8	102	150	3,370,000	2	79.029	130	0.85	141,900	0	190.105	269.170	3.72E+06	424	
Flash Memory	U104	86	165	5,972,952	7	23.797	121	1	58,800	0	147.276	562.018	1.78E+06	203	
Flash Memory	U105	83	165	5,972,952	7	19.669	121	1	58,800	0	115.280	456.505	2.19E+06	250	
Flash Memory	U106	79	165	5,972,952	7	15.180	121	1	58,800	0	82.622	345.833	2.89E+06	330	
Flash Memory	U107	75	165	5,972,952	7	11.646	121	1	58,800	0	58.765	262.058	3.82E+06	436	
RS-232 Driver/Rcvr	U18	93	125	1,608,840	0	95.755	121	1	307,488	0	49.104	144.888	6.90E+06	788	
Registered Transcvr		U196	91	155	2,600,000	0	12.559	85	0.85	1,976,000	0	152.603	165.179	6.05E+06	691
Registered Transcvr		U197	89	155	2,600,000	0	11.103	85	0.85	1,976,000	0	130.250	141.370	7.07E+06	807
E-PROM		U35	91	145	178,988	0	287.173	121	1	4,320	0	2988.334	3369.260	2.97E+05	34
FPGA		U26	96	145	423,433	1	362.421	121	1	18,816	0	1011.791	1374.441	7.28E+05	83
<b>TOTAL</b>						<b>1412.744</b>					<b>16765.038</b>	<b>18191.157</b>	<b>5.50E+04</b>	<b>6</b>	

## REFERENCES

- [1] W. Nelson, "Accelerated Testing: Statistical Models, Test Plans, and Data Analysis," John Wiley & Sons, 1990.
- [2] B. De Salvo, G. Ghibaudo, G. Pananakakis, G. Reimbold, F. Mondond, B. Guillaumot, and P. Candelier, "Experimental and Theoretical Investigation of Nonvolatile Memory Data-Retention," *IEEE Transactions on Electron Devices*, Vol. 46, No. 7, p.1518-1524, July 1999
- [3] EIA/JEDEC Publication 122, *Failure Mechanisms and Models for Silicon Semiconductor Devices*
- [4] D. Stewart Peck, "Comprehensive Model for Humidity Testing Correlation," *24th Annual Proceedings of the International Reliability Physics Symposium*, IEEE, 1986, pp. 44-50.
- [5] Ö. Hallberg and D. Stewart Peck, "Recent Humidity Accelerations, a Base for Testing Standards," *Quality and Reliability Engineering International*, Vol. 7, 1991, pp. 169-180.
- [6] S. M. Tam, "Demonstrated Reliability of Plastic-Encapsulated Microcircuits For Missile Applications," *IEEE Transactions on Reliability*, Vol. 44, No.1, 1995 March, pp. 8-13.
- [7] N. Sinnadurai, "Plastic Packaging Is Highly Reliable," *IEEE Transactions on Reliability*, Vol. 45, No. 2, pp.184-193, June 1996.
- [8] M. Brizoux, G. Deleuze, R. Digout and M. Nallino, "Plastic Encapsulated ICs In Military Equipment Reliability Prediction Modeling," *Quality and Reliability Engineering International*, Vol. 8, pp. 195-211, 1992
- [9] W. Nelson, "Accelerated Testing: Statistical Models, Test Plans, and Data Analysis," John Wiley & Sons, 1990.
- [10] S. S. Manson, "Thermal Stress and Low-Cycle Fatigue," McGraw-Hill Book Co., New York, 1966.
- [11] C. F. Dunn and J. W. McPherson, "Temperature Cycling Acceleration Factors for Aluminum Metallization Failure in VLSI Applications," *28th Annual Proceedings of the International Reliability Physics Symposium*, IEEE, 1990, pp. 252-258.
- [12] R. C. Blish II and P. R. Vaney, "Failure Rate Model for Thin Film Cracking in Plastic ICs," *29th Annual Proceedings Intentional Reliability Physics Symposium*, 1991, pp. 22-29.
- [13] R. C. Blish II, "Temperature Cycling and Thermal Shock Failure Rate Modeling," *35th Annual Proceedings of the International Reliability Physics Symposium*, IEEE, 1997, pp. 110-117.
- [14] R. Blish, Ph.D., S. Huber, N. Durrant, "Use Condition Based Reliability Evaluation of New Semiconductor Technologies," SEMATECH Tech Transfer Document 99083810A-XFR, August 20, 1999.
- [15] MIL-HDBK-217F, *Reliability Prediction of Electronic Equipment*

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