

Hot-Carrier Degradation of 2-Volt Silicon-On-Insulator (SOI) Transistors

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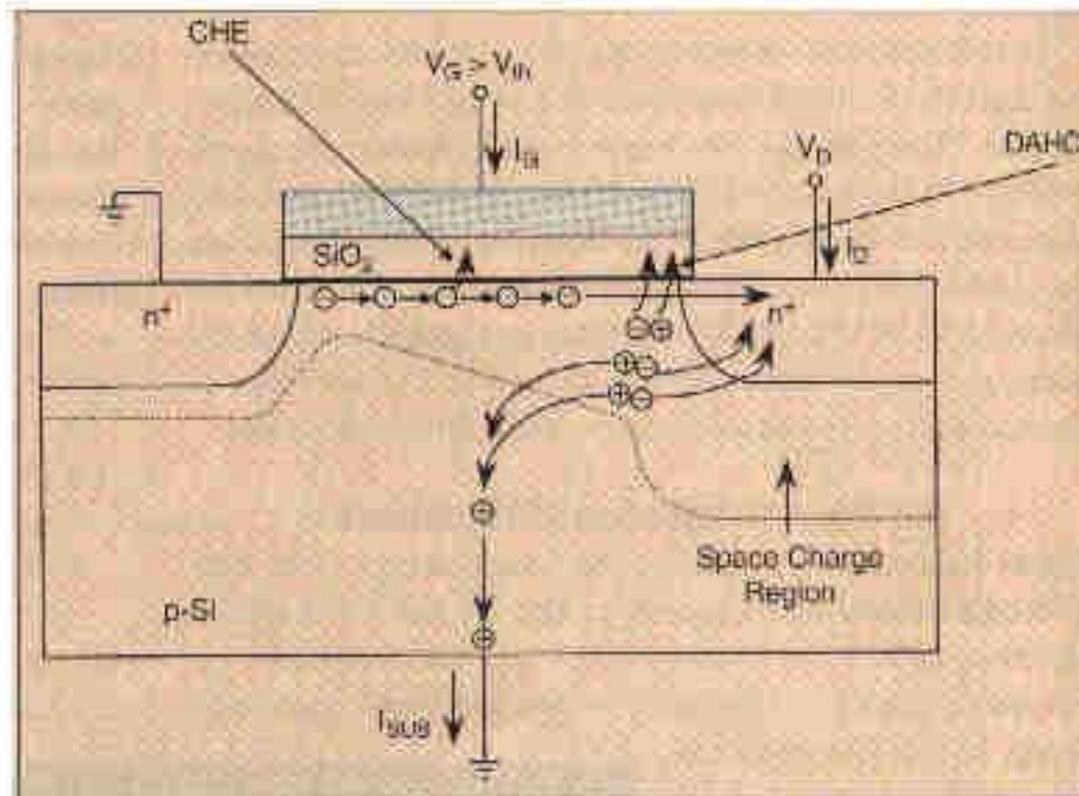


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Outline

- Review of hot-carrier effects as function of drain voltage
 - Hot-carrier generation
 - Oxide and interface traps
 - Trap generation and charging
 - Degradation effects
 - Time dependence
- Silicon-On-Insulator
 - FD-SOI transistor structure
 - Interface coupling
 - Stress experiments
 - Lifetime
- Conclusions & Suggestions for SOI Wafer Screening
- Plans & Collaborators

Classical Hot-Carrier Generation in MOSFETs



Sugiharto et al.,
IEEE Circuits & Devices,
Sept. 1998

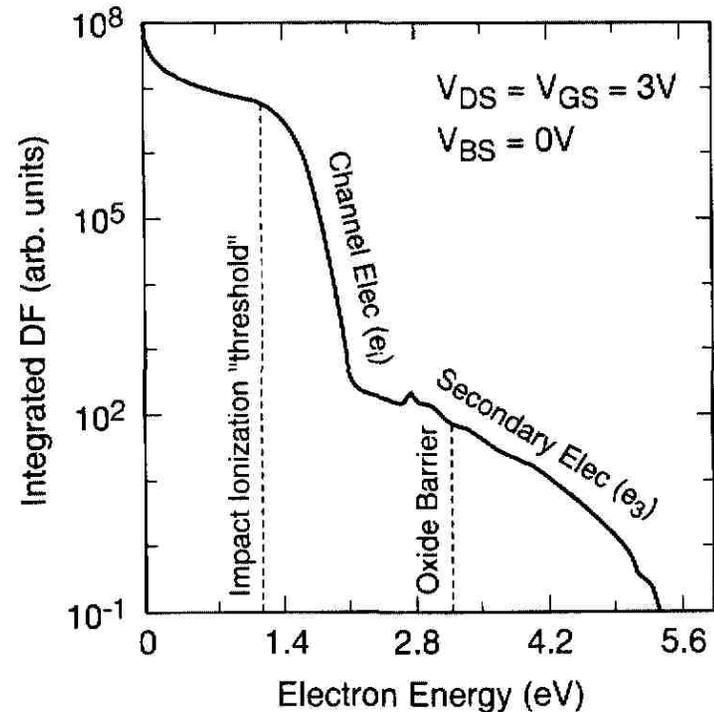
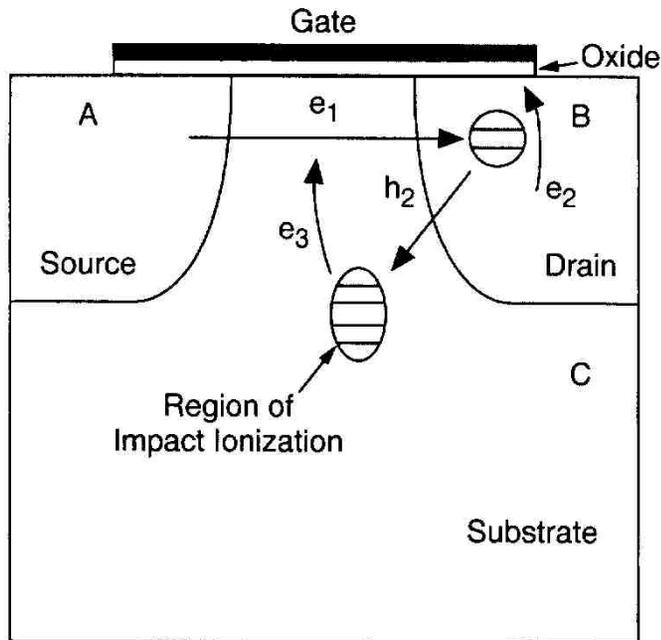
Channel Hot-Electron (CHE) generation → low flux

- Drain Avalanche Hot-Carrier (DAHC) generation → high flux. Impact ionization energy $\Phi_i = 1.1$ eV.

Oxide and Interface Traps

- Hot carriers with enough energy may create traps either in the gate oxide or at the silicon/oxide interface.
- They may also fill existing traps.
- Oxide barrier energies:
 - Electrons $\Phi_c = 3.2$ eV
 - Holes $\Phi_h = 3.6$ eV
- Available energy gain of carriers limited by drain voltage.
 - Carriers may overcome barrier with less average energy due to Boltzmann tails. Electrons may enter oxide for $V_d > 2.7$ V.
- Trap generation energy:
 - $\Phi_t \approx 0.3 \dots 0.5$ eV
 - Must be added to barrier energy for oxide traps
- Carriers may tunnel into traps close to interface

Generation of Electrons with Average Energy $> eV_d$



- High-energy secondary electron generation through drain-bulk junction feedback [Bude 1995]

Degradation Effects

- Threshold voltage shift due to field shielding by trapped charge. Negative charges make $\Delta V_t > 0$.
- Transconductance degraded by increased Coulomb scattering of channel carriers.

Time and Drain Voltage Dependence of Degradation

- Trap creation: Power time law

$$\Delta \propto \exp(-a/V_d) \times t^n$$

$n = 1$ reaction limited, $n = 1/2$ diffusion limited

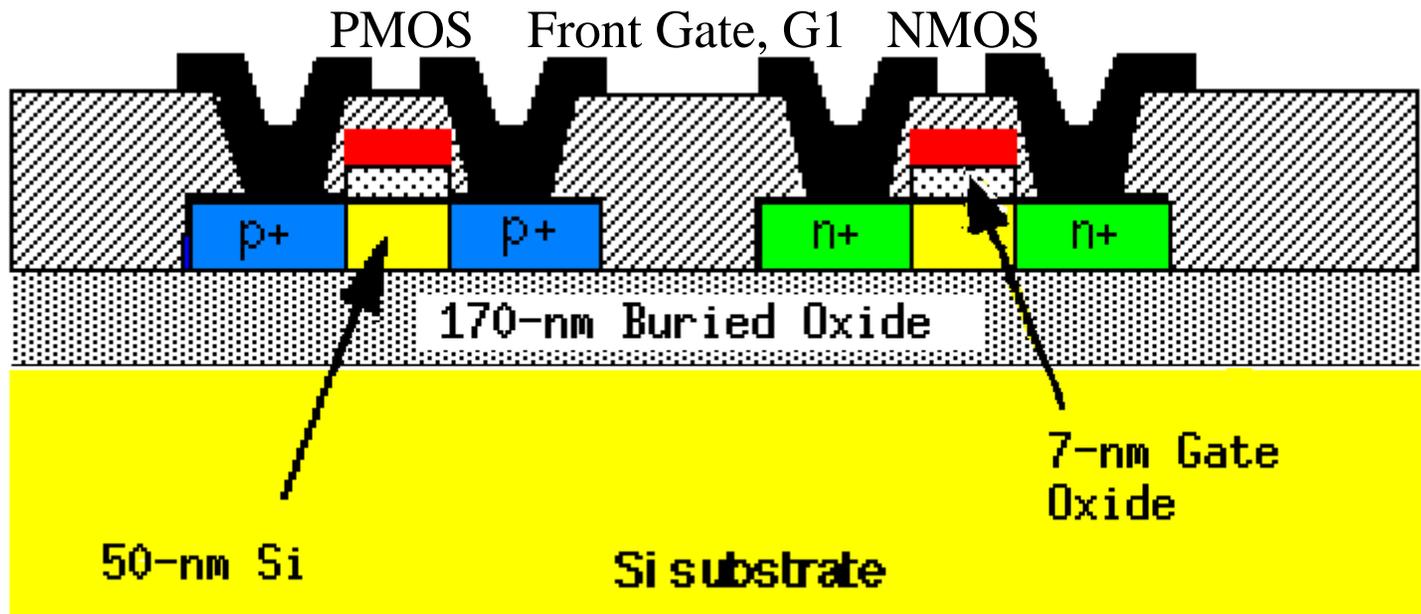
- Trap filling: Logarithmic time law

$$\Delta \propto (V_d - V_0) \times \log(t/t_0)$$

[Q. Wang, M. Brox, W.H. Krautschneider, and W. Weber, “Explanation and model for the logarithmic time dependence of p-MOSFET degradation”, IEEE Electron Device Letters 12, 218 (1991)]

Silicon-On-Insulator

(MIT/LL Fully-Depleted 0.25- μm SOI-CMOS)

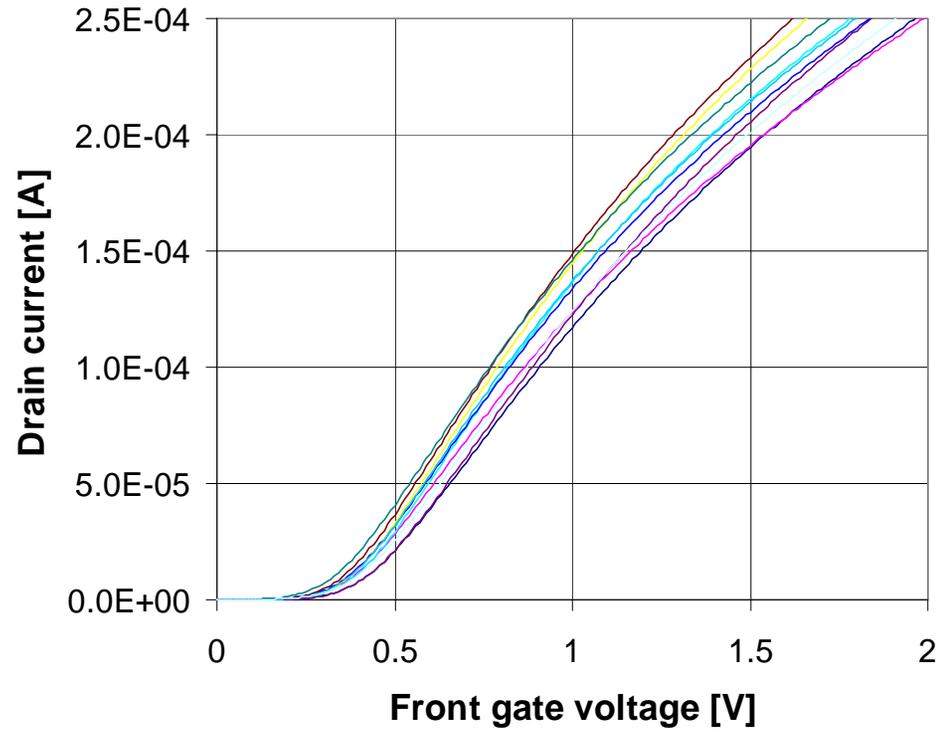


Back Gate, G2

Buried Oxide (BOX) = SIMOX (Separation by Implanted Oxygen)

This paper: NMOS only. Source grounded in all experiments.

I_d vs. V_{g1} Characteristics of NMOSFETs



Threshold voltage standard deviation:

$$\sigma = 25 \text{ mV}$$

Oxide Interface Coupling Effects on Threshold Voltage

Front threshold voltage with depleted back interface:

$$V_{th1,dep2} = V_{th1,acc2} - K1 (V_{g2} - V_{g2,acc})$$

Coupling Factor:

$$K1 = T_{ox1} / (T_{ox2} + T_{si} / 3)$$

Changes after stress:

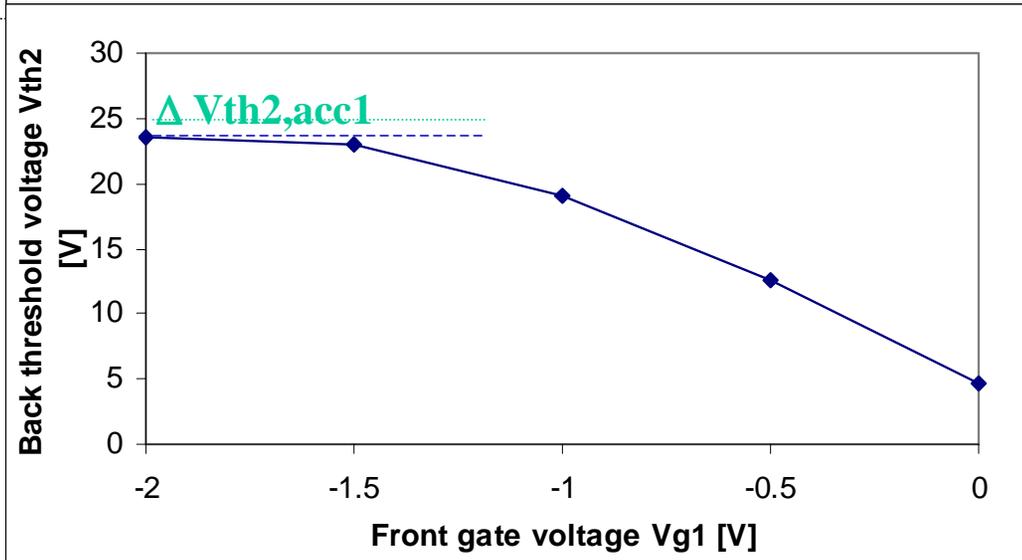
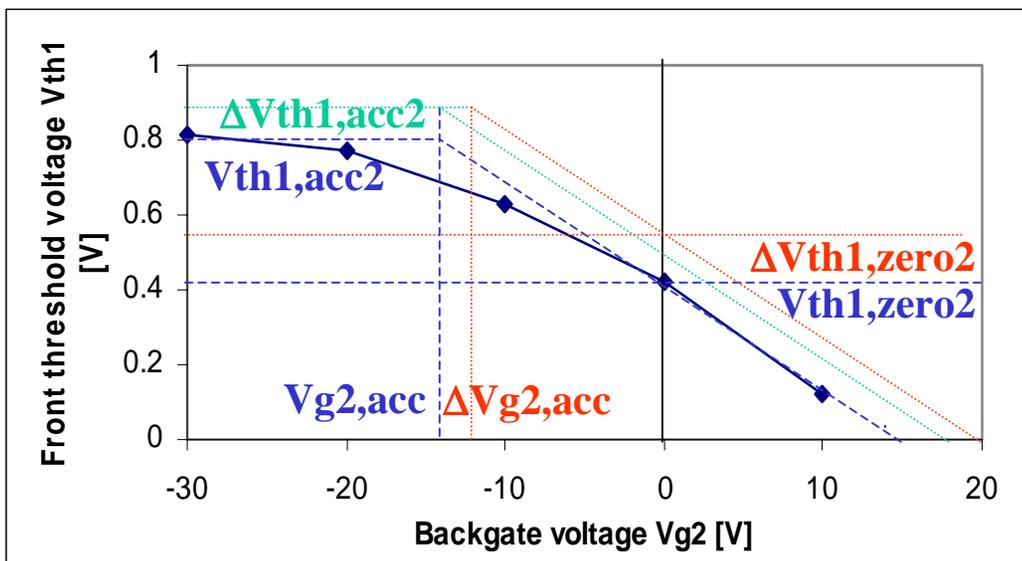
$$\Delta V_{th1,zero2} =$$

$$\Delta V_{th1,acc2} + K1 \Delta V_{g2,acc}$$

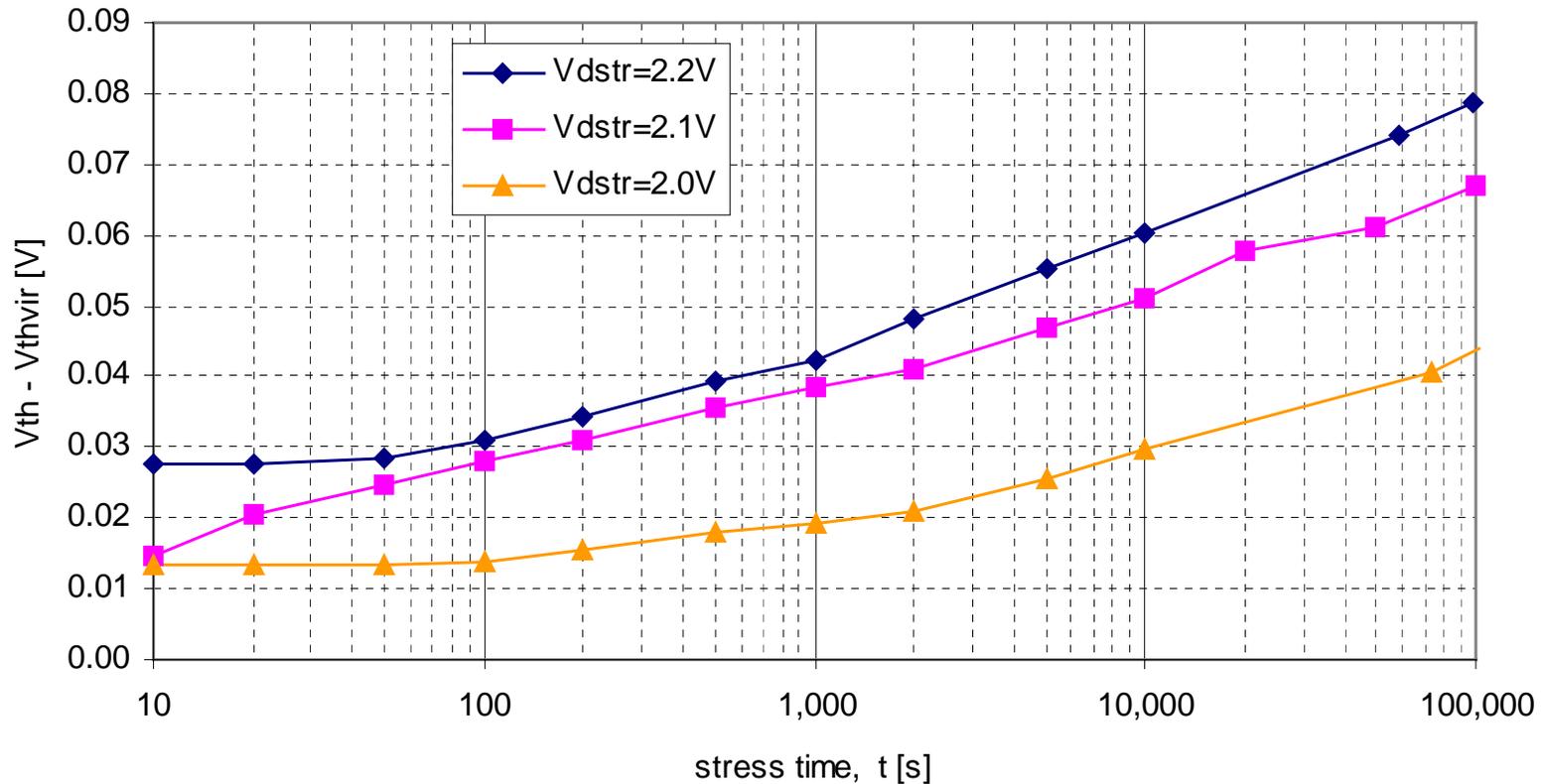
Banna et al. 1998:

$$\Delta V_{g2,acc} = \Delta V_{th2,acc1}$$

Stress-induced charges at both interfaces cause front threshold voltage shift at zero back bias

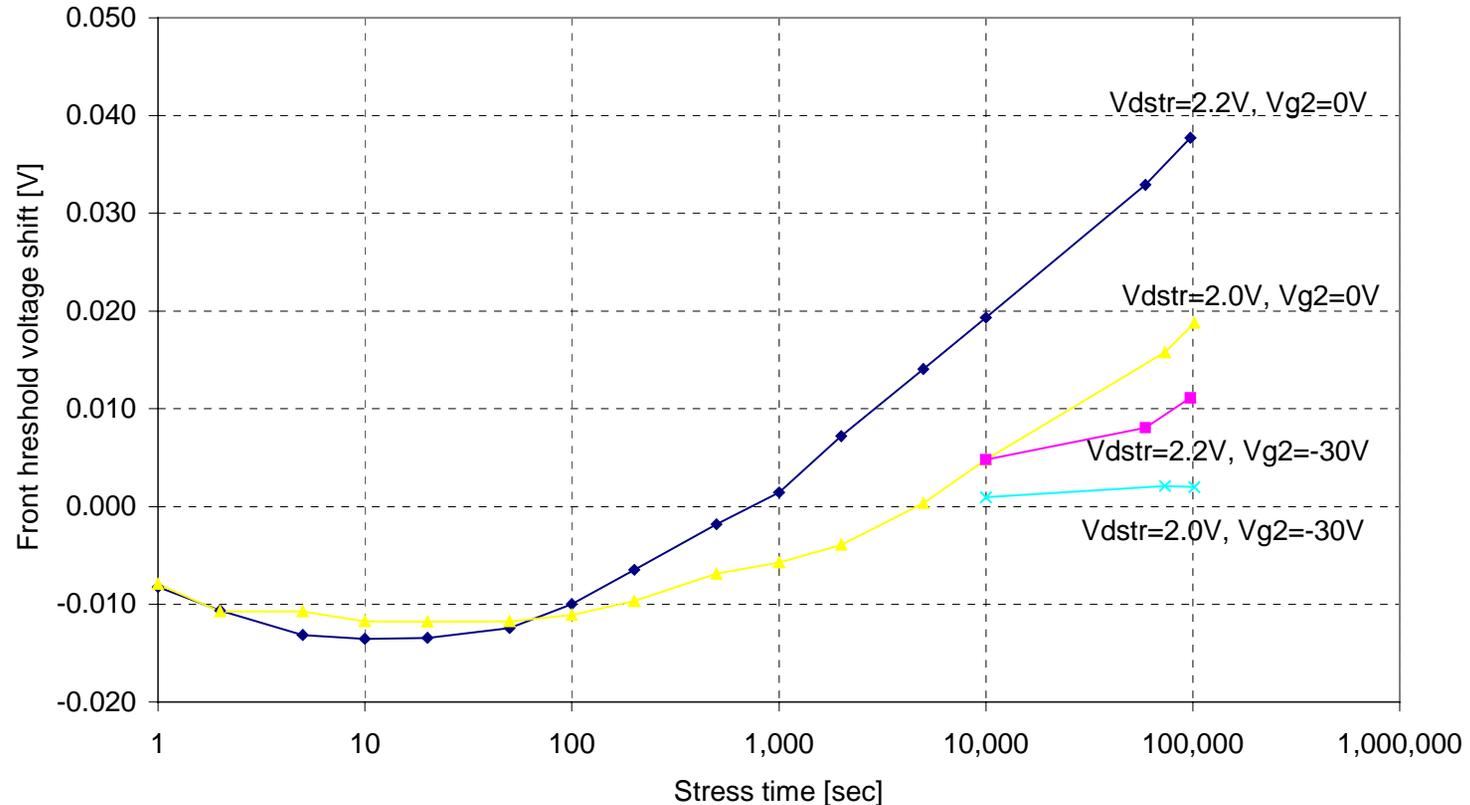


Evolution of (Front) Threshold Voltage Shift with Different Stress Drain Voltages



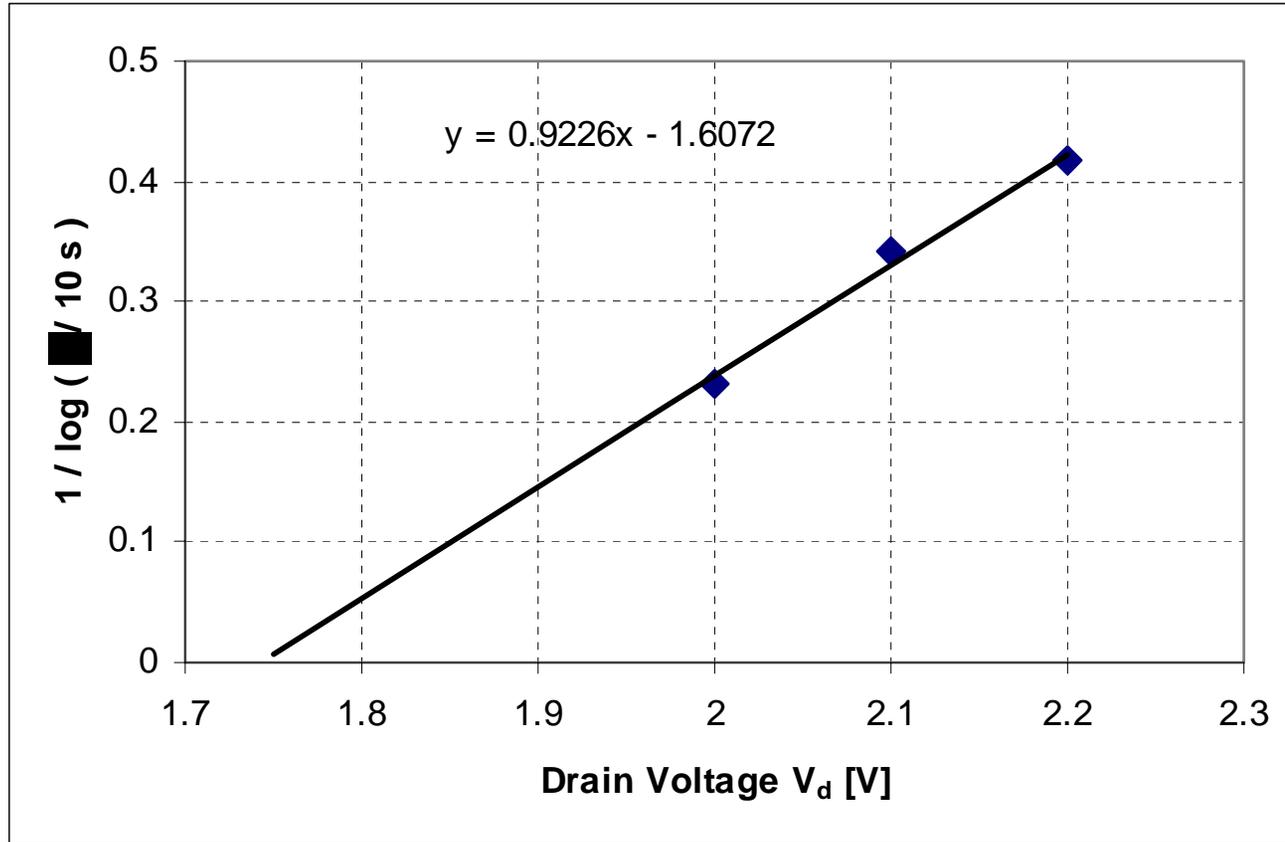
$V_{g2} = 0 V$, $V_{g1str} = 1 V$. First and third sample already degraded by pretest.

Biasing Back into Accumulation ...



... Eliminates Most of Front Threshold Voltage Shift
→ Mostly Back Interface Degraded

Lifetime τ ($\Delta V_{th} = 50 \text{ mV} = 2 \sigma$)



$$\text{Log} (\tau / 10 \text{ s}) = 1.08 / (V_d - 1.74 \text{ V}) \Rightarrow \tau \rightarrow \infty \text{ for } V_d \rightarrow 1.74 \text{ V}$$

Conclusions

- Investigated lot of 0.25-mm PD-SOI N-MOSFETs had a ($\Delta V_{th} = 2\sigma$) - lifetime of only 55 h at the target operating voltage of 2.0 V.
- Degradation due to hot electrons from front-channel operation charging BOX interface.
- Time and drain voltage dependence of degradation suggests filling of existing traps at BOX interface.
- Safe operation predicted for $V_d \leq 1.74$ V .
- SOI substrates must be screened for their susceptibility to hot-carrier effects.

Suggestions for SOI Wafer Screening

- Point-contact diode:
 - Probe thin-film Si surface (ground)
 - Apply charge-pumping to back gate (Si-substrate) area contact.
 - Measure interface trap distribution.
 - Difficulty: Needs simulation to predict hot-carrier effects.
- Point-contact transistor:
 - Probe thin-film Si surface with source and drain probes.
 - Apply stress voltage.
 - Measure back gate threshold voltage shift.
 - Difficulty: Dual probe with 0.25- μm separation must be microfabricated, cf. recording heads.

Plans

- **Study hot-carrier degradation at low temperatures (less scattering \Rightarrow higher energies \Rightarrow enhanced degradation)**
- **Survey wafer qualification procedures**
- **Test SOI circuits at low temperatures**

Collaborators

- Anne Vandooren, UC Davis / JPL / Motorola
- Sorin Cristoloveanu, ENSERG Grenoble
- Jagdish Patel, JPL
- Bernard Rax, JPL
- Ashok Sharma, GSFC
- Richard Patterson, GRC