

Controlled PEMs, A High Density Packaging Solution for Space

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Abstract

TRW is recognized as a world class leader in high reliability microelectronics packaging technologies for space applications. A controlled insertion of plastic encapsulated microcircuits (PEMs) is demonstrated and highlights how this technology can provide a superior integrated circuit (IC) packaging solution over traditional ceramic-based assemblies. Space qualified insertion of Plastic Ball Grid Array (PBGA) packages addressing high I/O packaging needs is the focus of this publication. Space-qualification of a laminate-based area array packaging technology responds to the ever increasing demand for reliable, cost effective, high density interconnect (HDI) solutions. At present there are no industry-approved procedures for space level processing or procurement of PEMs. Through active management of IC packaging and space flight hardware design, PBGA procurement and use in high reliability space applications is demonstrated. TRW space programs will benefit from aggressive insertion of JEDEC standard plastic ball grid array packages to achieve higher performance designs with dramatically increased circuit densities, while reducing electronic product's size, weight, power, and cost [1]. A proven methodology for controlling the design, fabrication, assembly, test, and qualification is reviewed.

Key Words: input/output (I/O), plastic encapsulated microcircuits (PEMs), plastic ball grid array (PBGA), ceramic quad flat pack (CQFP), ceramic ball grid array (CBGA), ceramic column grid array (CCGA), hermetic, high density interconnect (HDI), dual sequentially laminated (DSL)

Introduction

Suitability of PEMs for high reliability space programs is a subject with relatively few recent publications given the advances made in the technology and the inherent size and weight benefit of plastic packaging. Establishing program benefits while managing risk is the required charter for any new technology insertion and is presented in detail here. Even as evidence of plastic parts for space usage emerges, very little data is getting published. Furthermore, users of plastic packages for past or present space flight missions are reluctant to share experiential information and empirical data; presumably more for risk perception reasons than for competitive ones. While actual publications are scant, interest in this area is growing as evidenced at a recent Space Parts Working Group meeting [2], where a number of presentations were made relating to PEMs. Aerospace contractors, in the face of parts obsolescence issues and increasing demand for higher density packaging solutions, will be forced to take a much closer look at plastic. This paper

summarizes related work at TRW, and endorses the use of controlled PEMs for space. Milsatcom AEHF is the first planned space insertion target.

The subject of this paper is a focused one and does not address use of COTS PEMs or plastic packaging in general. On the contrary, a specific family of plastic parts, controlled PEMs in the form of a plastic ball grid array, is the packaging technology evaluated in this report. This area array IC packaging technology warrants a dedicated reliability publication due to the unique properties of PBGAs and the solutions this advanced packaging technology offers. For one, it is with certainty that peripheral leaded monolithic packages can no longer keep pace with high I/O (eg. >320 signal) CMOS IC technology advancements. Multichip solutions, or a single chip area array packaging scheme needs to be adopted.

A controlled PBGA is defined as a microelectronics assembly produced through an approved manufacturing flow using approved materials and processes. PBGA fabrication and assembly for space use must start with a known

pedigree organic laminate substrate and a known pedigree integrated circuit die. The die is physically attached to the substrate and electrically interconnected using wirebonds. The substrate provides trace interconnect to I/O leads in the form of solder balls. The assembly is then encapsulated in a high purity, low ionic content plastic that makes direct contact with the die and interconnect.

PBGAs differ from hermetically sealed packages since they feature no cavity and no hermetic seal formed by glass, metal, or ceramic materials. This key difference highlights the need to assess Reliability Without Hermeticity (RWOH) for plastic systems. TRW has evaluated the performance of hundreds of plastic ball grid arrays through detailed design, fabrication, assembly, and hardware testing. Significant performance variability impacting part durability and reliability has been observed from different PBGA vendors. Differences in PBGA design and construction including material and process selection are the performance discriminators.

PBGA body sizes to 35 mm and 416 I/O have been space-qualified. The qualification envelope is being expanded to include parts to a 45mm body size and over 800 signal I/O. Package construction in all cases is cavity up, with perimeter row solder balls for signal, power, and ground. A center array of solder balls for thermal management is also present directly under the die. The largest IC packaged to date measured just over 15mm square. Both dam and fill liquid encapsulant and overmolded structures were evaluated. Figure 1 shows representative PBGA design and construction.

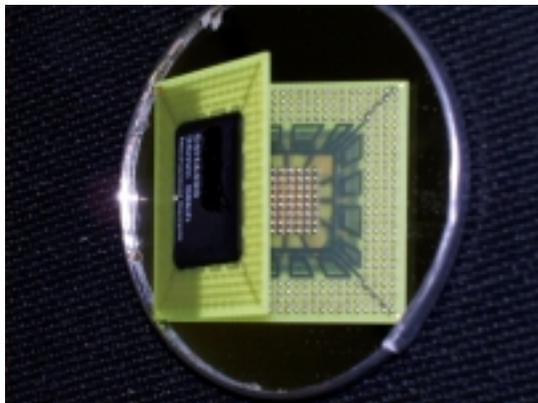
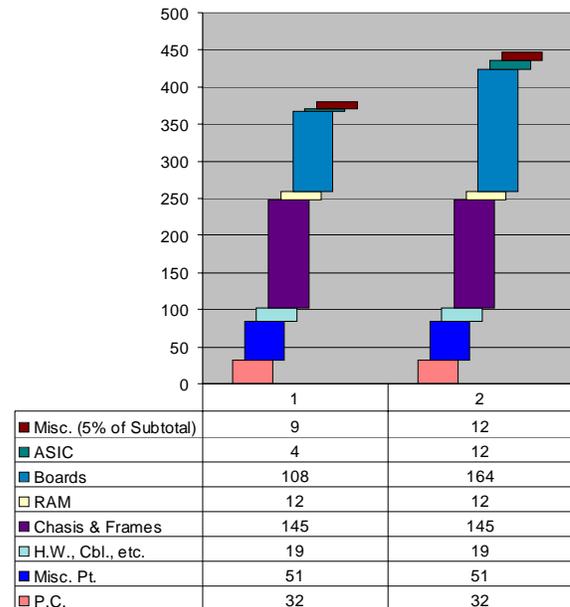


Figure 1. 35mm "Cavity-Up" PBGA

Background

PBGA packages provide a more reliable solution for dense digital products. Composite CTE for the PBGAs recorded at 14-19 ppm is closely matched to the board assembly CTE of 16-18 ppm for

polyimide glass resulting in a higher reliability structure [3]. Plastic parts avoid the pitfalls of their ceramic based counterparts; Ceramic Ball Grid Arrays (CBGA) and Ceramic Column Grid Arrays (CCGA), such as managing the CTE mismatch to the board, the heavier weight and associated stresses on the rigid solder joint, and the higher development and production costs. PBGA based board assemblies demonstrate better performance through vibration testing and are easier to produce. CBGA and CCGA packages weigh 3-4 times a comparable PBGA and may require a constrained core board technology to mitigate stresses relating to CTE mismatches adding significant weight to the subsystem design. Figure 2 illustrates this point with a net 68 pounds weight savings on a digital subsystem employing ASICs packaged in PBGAs versus ceramic based area array packages.



**PBGA 380 lbs. CBGA / CCGA
448 lbs.**

Figure 2. Space Subsystem Weight Comparison

PBGAs provide numerous benefits at all levels of interconnect for the desired product, but their design, construction with particular emphasis on material selection, and their implementation including assembly, handling, and storage must be explicitly controlled. These topics are briefly discussed in the following sections.

ASIC Design and Fabrication – Digital ASIC fabrication is performed at subcontractors facilities including QML certified radiation hardened CMOS foundries. Device characterization impacting first

level of interconnect packaging choices are fully understood and include electrical, thermal, mechanical, and radiation characteristics.

Design and Construction – The ball grid array package design is optimized to provide the required performance at the lowest size, weight, and cost. JEDEC standard parts are used, and established design rules are followed.

Materials and Process Requirements - PBGA materials [4] must withstand mass reflow soldering operations. This implies relatively high temperature laminates and high purity die attachment adhesives and die encapsulants that must not outgas at unacceptable levels. Long term reliability requires the encapsulant to shield the die from moisture. Epoxy encapsulants absorb moisture and may fracture during reflow operations if not kept dry. Viscous drag of a poorly chosen encapsulant can break the wires. Low viscosity encapsulants must be specified to avoid this problem. The thermal-expansion rates of metal wire, silicon die, laminate material, and encapsulant generally differ. Care must be taken to choose an overall material system that enables wire bonds to survive all anticipated thermal excursions.

Most PBGAs employ standard Sn 63 tin-lead-solder balls that collapse during reflow attachment to the printed wiring board. By contrast, ceramic BGAs employ higher temperature, non-collapsible 90/10 Pb/Sn solder. Solder-ball and solder-mask composition should be chosen to optimize the adhesion of the solder balls to the laminate and to the host printed wiring board.

Assembly Requirement - ASIC packaging yielding a reliable space-qualified PBGA assembly needs to be controlled. Assembly houses that routinely perform plastic packaging need to be audited to thoroughly characterize their standard materials and processes and the approved process flow needs to be enforced. Component level qualification testing must be performed with an emphasis on moisture ingress as the primary failure mechanism of interest.

Test Requirements - The PBGA can be reliably tested using an appropriately sized BGA socket and device adapter board. Testing an area array subassembly is no more demanding than a leaded device.

Handling and Storage - PBGA assemblies are placed in high temperature matrix shipping and handling trays, and vacuum bagged with a desiccant or stored in dry nitrogen. ESD rated trays for JEDEC standard body sizes are readily available and are optionally bakeable to 180 °C.

Test and Analysis

Figure 3 shows a dense electronics assembly typical of ones used for product reliability testing. Over 100 plastic ball grid array packages

(~30,000 solder joints) are mounted back to back on both sides of the 10" x 16" assembly. Unique monitoring circuitry featured on this assembly includes a latch circuit for each BGA pair (front and back) and a dedicated LED for each BGA. The fault circuitry was designed with sub microsecond response time to detect opens in the solder joints during thermal cycling and vibration testing, and provided visual identification of failure sites. Surface mount capacitors and resistors make up the remainder of the components.

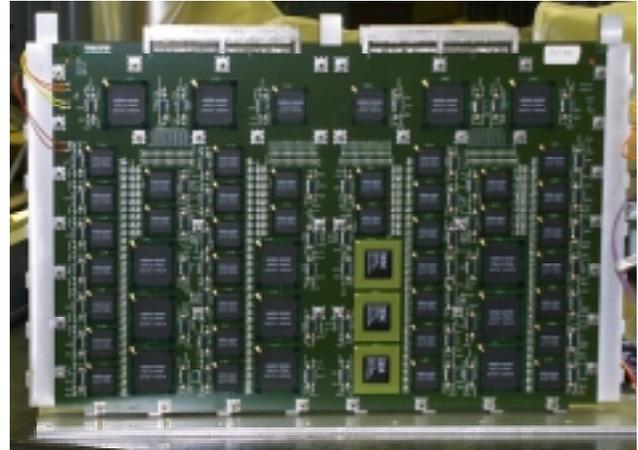


Figure 3. HDI Board; 108 Back-to-Back PBGAs

PWB Design and Manufacturing – To support a BGA solution to the increasing demand for reliable, cost effective, high-density interconnect (HDI) solutions, a high density printed wiring board must meet conflicting requirements in design, assembly, and environmental compatibility while remaining producible. In design, the board must meet the required routing density, provide breakout within the pitch of the area array package, meet signal quality requirements, and provide a reliable interconnect structure. In assembly, the board must meet size constraints, automated pick and place, solder reflow constraints, and flatness. For environmental compatibility the board must provide adequate stiffness for vibration and dissipate the heat through adequate thermal conduction. A design solution for such a printed wiring board has been demonstrated.

The selected construction is polyimide-glass and the board is dual sequentially laminated (DSL) symmetrical about the midplane and utilizes blind vias from both sides of the board. Four separate designs were evaluated to assess producibility aspects of large panel HDI structures as well as subsequent assembly and environmental differences. Multiple via structures have been studied ranging from offset blind vias in a “dogbone” configuration (Figure 4)

through microvia “via-in-pad”. All designs incorporate DSL construction and featured fault detection circuitry. Considerable research has been done to optimize the geometry of the surface conductor pattern. IBM has been a leader in testing almost all of the possible geometrical structures and established that a non-solder-mask-defined (NSMD) pad, also called “pad defined”, at the PWB level is more reliable [5] than a “solder mask defined” (SMD) pad. Figure 5 graphically depicts one design. The details of the board are considered proprietary but design features have included considerations of, pad geometry, via diameter, aspect ratio, plane clearance, plating thickness, surface condition, construction balance, plane thickness, impedance control, surface clarity, flatness, soldermask coverage, fiducials, surface finish, dynamic deflection, coefficient of thermal expansion, outgassing, and marking.

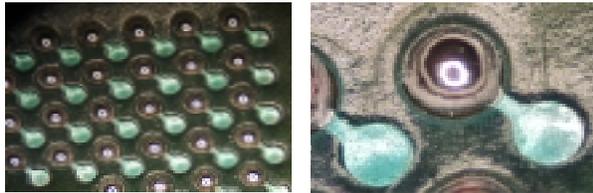


Figure 4. Dogbone Mini Vias

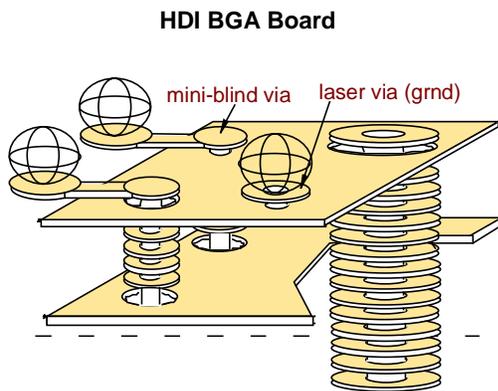


Figure 5. Design with Dogbone Construction

Part Handling and PWB Assembly – PBGAs should be stored in clean, dry nitrogen boxes. A bakeout for 4 hours at 125°C prior to assembly is required which provides a floor life of two days when held at an ambient condition not exceeding 30°C and 60%RH. This step ensures that the components will not “popcorn” in response to the rapid heating that occurs during mass reflow operations. Boards should be baked for 6 hours at 121°C and also stored in dry nitrogen prior to assembly.

Automated board assembly is essential to establish repeatable processes and achieve the control required to eliminate 100% inspection of solder joints. Placement accuracy is important for large, extremely dense PWB assemblies, even with the “self-aligning” feature during reflow that is characteristic of PBGAs. Solder joints must not open in response to anticipated mission or test thermal cycles or vibrations, and joints must not bridge (short) during placement or reflow. Figure 6 shows a cross sectional view of an assembly with a via in pad construction.

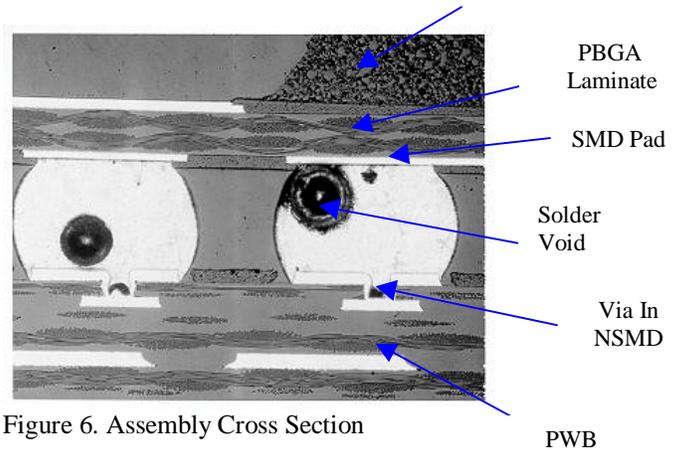


Figure 6. Assembly Cross Section

Inspection methods that verify process control and identify anomalous solder joints (eg. shorts, opens, or irregular/weak joints), need to be established. Solder joint inspection is difficult once the parts have been mounted to their host circuit board. Several commercially available systems address this problem of a blind joint. Ninety-degree prism assisted optical inspection systems utilizing fiber optic lighting make direct observation of the periphery of the first row of solder joints feasible. Though tedious, this approach can identify cold solder joints, external cracks, bridges, and flux contamination. X-ray techniques can rapidly locate solder-joint bridges. X-ray laminography permits overall assessment of solder-joint quality by providing layer-by-layer images of the solder joints. The scans gathered from each layer can be assembled into a three-dimensional image of the PBGA-board interconnections.

Rework operations must lead to solder joints as reliable as those produced during the normal process flow. A localized rework procedure has been established and a 3x single site rework capability has been demonstrated

The following sections summarize the analytical work performed on PBGA board assemblies to predict the performance of this

hardware and induce failures to characterize long-term reliability.

Board Assembly Thermal Analysis - Board assembly thermal analysis couples chassis-level boundary conditions with PBGA-level power dissipation to predict temperature rise from chassis-to-part, including the part itself. The thermal designs were modeled to predict the PBGA junction temperature and assure that it would not exceed the specified maximum allowable operating temperature.

Thermal Cycling - Continuous temperature cycling was performed on plug-in assemblies consisting of two board assemblies mounted on either side of an aluminum frame support structure. Thermal cycling tests to failure were conducted from -40°C to $+100^{\circ}\text{C}$ with a 30-minute dwell time and transfer time. Continuous monitoring was performed with quick visual indicators of failures via the LED circuitry. Two groups of PBGA board assemblies were tested. The assemblies in the first group were thermal cycled to failure. The second group of board assemblies were first exposed to acceptance test thermal cycling (10-cycles, -40°C to $+100^{\circ}\text{C}$), and were then vibration tested. Fifteen hundred cycles were monitored in the first group before concluding the test. Initial solder fatigue failures did not occur until well over 1100 cycles. As expected, the large 35mm body size PBGAs exhibited a higher failure rate than the smaller parts, which were still not showing significant failures at 1500 cycles. Significant variability in thermal cycle induced failures from vendor to vendor was observed. This result is attributed to the individual PBGA design and construction. Figure 7, a Weibull distribution plot of our thermal cycle data, shows PBGA package reliability consistent with industry data for similar systems [6].

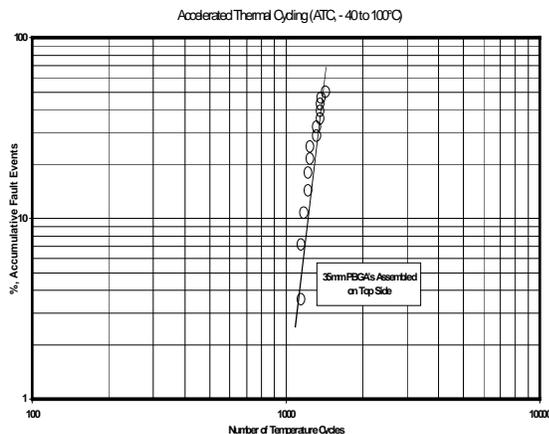


Figure 7. Weibull Distribution of Failures

Board Assembly Structural Analysis - The structural design of the board assembly is such that the dynamic deflection criterion for part mounting is not exceeded. Board assembly structural analysis translates environmental conditions into design loads for hardware design. For instance, the board assembly is designed to meet typical overall random vibration levels of approximately 23 Grms.

Vibration Testing - Our expectations that *this* hardware qualification test would be the one most likely to produce catastrophic failures was *not* in fact fulfilled. One early observation, was that while we did experience early vibration induced solder joint failures from one PBGA supplier, we were unable to test to destruction PBGAs provided by a second supplier. This result reinforced the proposition that controlled package design, materials, and construction, coupled with a prudent overall approach to the electronic equipment design can yield qualifiable space hardware.

Over 20 random vibration tests have been performed on flight like hardware. Figure 8 shows a BGA assembly in its vibration fixture and the test setup used during testing.

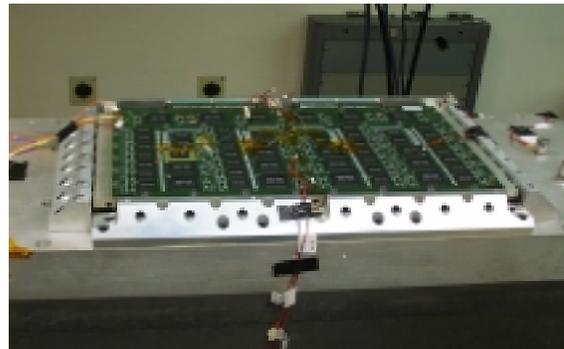


Figure 8. Vibration Test Fixture for BGA Board

During all the trials, the LED/latch circuitry visible from the top of the assembly was used to monitor BGAs on both sides of the assembly. Failures identified by a lit LED were recorded. Once lit, the LED remained lit and BGA locations were recorded as failures even if the joint ultimately recovered electrical continuity. Initial vibration trials reinforced the thermal cycle result that one package supplier's design, materials, and construction outperformed the other supplier. Two board assemblies were tested during initial vibration trials. The initial vibrate tests was conducted as a four phase step test as follows: 5Grms (0.5 min), 10Grms (2 min), 14Grms (3 min), 22Grms (6 min). Three 35 mm BGAs failed during the low-level test set-up runs and one failed during the final 22 Grms run. All the failed parts were from one supplier. The second

board was vibration tested to 15 Grms for 3 minutes without any failures. The results of these early trials were very encouraging and served as a catalyst to launch the next design effort. Here, eight assemblies, each having over one hundred PBGAs, were subjected to various vibration tests, with some assemblies exposed to multiple vibration profiles. During initial 3-minute duration trials on all eight boards, 0.0017 in/in and 0.0019 in/in slope parameters were produced from 16 Grms and 23 Grms vibration levels respectively. First failures on four of the assemblies were noted, all from one package vendor in the 35mm body size. None of the smaller packages failed and none of the 35 mm PBGAs from the second source failed.

The assemblies had an overall board thickness of >0.125 in., and a fastener span of roughly 4.5 in. making it difficult to induce board deflections greater than .002 in/in. Additional trials were conducted, this time removing rows of fasteners to produce greater board deflection. Four of the original eight assemblies were re-tested to a maximum of 30 Grms producing a .003 in/in slope. The test was for six minutes at full level instead of a three-minute duration characteristic of a qualification test. No new electrical failures were observed. Allowing for a fatigue factor of two, slope parameters for all out trials ranged to 0.0015 in/in. While there was early evidence of failures from one package supplier, there was no evidence of any solder joint failures from a second supplier. All of the PBGAs from the second supplier maintained electrical continuity throughout the test. These results validate our ability to successfully design and manufacture high density, space flight hardware using controlled PBGAs as the packaging technology of choice for large high I/O integrated circuits.

Conclusions

Research conducted at TRW concludes that reliable space flight hardware, using plastic ball grid array (PBGA) IC packaging technology, can be produced through explicit control of design and manufacturing processes. Test results to date are extremely encouraging, and additional testing to fully characterize the limitations of this IC packaging technology is planned. A new test vehicle has been produced to increase the product qualification envelope to a 45 mm (816 I/O) package housing a silicon die over 17 mm square. Through additional testing of the new assemblies, we plan to further characterize the performance of PBGA solder joints. Random vibration testing is planned which will increase board deflection and test to destruct levels. These results will be used to provide design feedback to enhance current digital product designs.

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