

Reliability Evaluation of MIT/LL FDSOI 0.25 μm Process for Space Applications. (Part II)

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1.0 Introduction

The previous report titled, “Reliability Evaluation of Fully Depleted SOI (FDSOI) Technology for Space Applications,” posted on the NEPP web site, provided a general overview of SOI technology including materials, process, reliability issues, and MIT/LL FDSOI processes and associated reliability test structures. The hot carrier degradation effects in the MIL/LL FDSOI FETs at $V_g = V_d/2$ conditions, which are known to maximize the interface trap generation have been investigated at JPL [1].

This report (Part II) of the continuing evaluation, addresses characterization of the N- and P-channel transistors, including scaling effects and estimation of the reproducibility of the front- and back-channel parameters was performed. The transistor measurements included threshold voltage, subthreshold slope, mobility of charge carriers, gate leakage currents, and investigation of the edge effects.

2.0 FDSOI Process Monitor Transistors

A detailed description of the test structures used in MIT/LL to control manufacturing process and, in particular, FDSOI FETs was provided in the previous report [2]. For this evaluation, four process monitor dice were received, containing NMOS/PMOS transistors of various sizes. There were 40 FETs in each dice with $L = 0.2 \mu\text{m}$ to $0.8 \mu\text{m}$ and $W = 0.5 \mu\text{m}$ to $100 \mu\text{m}$.

The transistor structures were mesa-isolated and fabricated in SIMOX (separation by implantation of oxygen) wafers with silicon thickness 47 nm. The thickness of buried and thermal oxides was 170 nm and 7.3 nm. Polysilicon gates (200 nm of thickness) and active areas of the transistors were silicided after spacer formation. Parameters of the process used for wafer manufacturing are shown in Table 1.

The calculated maximum depletion width for a silicon with a doping level of $4 \times 10^{17} \text{ cm}^{-3}$, $W_T = 54.1 \text{ nm}$ which exceeds the t_{si} value of 47 nm , thus confirming that the device operates in a fully depleted mode.

Table 1. Process Parameters

| Characteristic | value | unit |
|---------------------|----------|-------------------|
| Handle wafer, Ptype | 2.00E+15 | 1/cm ³ |
| doping, $N_A = N_D$ | 4.00E+17 | 1/cm ³ |
| t_{ox} | 7.30E-07 | cm |
| t_{box} | 1.70E-05 | cm |
| t_{si} | 4.70E-06 | cm |
| Poly gate for NMOS | N+ type | |
| Poly gate for PMOS | P+ type | |

Values of the gate oxide capacitance (C_{ox}), buried oxide capacitance (C_{box}), and silicon capacitance, C_{Si} are shown in Table 2.

Table 2. Capacitance of the Layers

| Element | C, F/cm ² |
|--------------|----------------------|
| Gate oxide | 4.73E-07 |
| Buried oxide | 2.03E-08 |
| SOI | 2.22E-07 |

This allows for calculation of the coupling coefficients, α_1 and α_2 , and theoretical minimums for the subthreshold slopes, S_{11} and S_{22} . In a general case, the subthreshold slope and the coupling coefficients can be calculated as follows [3]:

$$S_{11} = 2.3 \frac{kT}{q} \left(1 + \frac{C_{it1}}{C_{ox}} + \alpha_1 \frac{C_{Si}}{C_{ox}} \right), \quad \dots(1)$$

$$\alpha_1 = \frac{C_{box} + C_{it2}}{C_{Si} + C_{box} + C_{it2}}, \quad \dots(2)$$

where the $C_{it1,2}$ are the capacitances due to front and back interface state densities $N_{it1,2}$. The equations for α_2 and S_{22} can be obtained by replacing C_{ox} with C_{box} and C_{it1} with C_{it2} .

The $S_{11/22}$ values are minimal when the interface capacitance can be neglected. This is true when the concentration of fast interface traps, which could exchange charges with

the Si during electrical measurements is below approximately $10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$. In this case, the calculations using data in Table 2 gives $S_{11\text{min}} = 62 \text{ mV/decade}$ and $S_{22\text{min}} = 503 \text{ mV/decade}$.

3.0 Experimental Measurement of Transistor Characteristics

Characteristics of the transistors were measured under probes using a Hewlett Packard Precision Semiconductor Analyzer, Model 4156A.

Typical output curves of the transistors are shown in Figure 1. Due to a strong coupling effect, characteristics of one of the channels of a transistor (front or back) strongly depend on the voltage applied to the opposite gate. This results in significant variation of the front-channel threshold voltage with the back gate bias.

To characterize gate oxide-SOI and buried oxide - SOI interfaces separately, the measurements were performed at “decoupling conditions” by biasing the opposite gate to create accumulation in the corresponding channel. The front gate characteristics were measured at +10 V on the back gate for N-channel transistors and -10V for the P-channel transistors. The back gate characteristics were measured at +1 V correspondingly for N- and P-channel transistors.

The threshold voltage, V_{th} , was measured using two methods: (1) constant current level ($I_d = I_{th} = W/L * 0.1 \mu\text{A}$ at $V_d = 50 \text{ mV}$), and (2) ohmic region by $I_d/\text{SQRT}(g_m)$ extrapolation (where g_m is the transconductance) to the intercept with the horizontal axis. In all cases, a very good correlation between the two methods was observed (see Figure 2).

The subthreshold slope, S , typically was measured at the drain current range from 10^{-11} A to 10^{-8} A . The mobility of the carriers, μ , was calculated by measurements of the slope, K , of the $I_d/\text{SQRT}(g_m)$ function in the ohmic region [4]:

$$\frac{I_d}{\sqrt{g_m}} = K(V_G - V_{th}), \quad \dots(3)$$

$$\text{where } K = \sqrt{\frac{\mu V_d C_{ox} W}{L}} \quad \dots (4)$$

Out of four dice obtained from MIT/LL, one dice had more than 90% of failed transistors (in most cases the front channel did not open up to $V_{g1}=2\text{V}$). It is possible that this die was from another lot/wafer and was not considered in the statistics shown below.

3.1 Threshold Voltage

Threshold voltage was measured for 15 to 20 transistors of N- and P-type from three dice. Average and standard deviations of the V_{th} values for transistors with the same gate width and length were calculated. Mean values of these characteristics are shown in Table 3 below.

It is seen that variation of the V_{th} within one wafer did not exceed 5% for the P-channel devices. However, characteristics of the front gate channels in the N-channel transistors are less reproducible and the variation reached 12%.

The front-gate threshold voltage in P-channel transistors significantly increased with decreasing the channel length from approximately -850 mV at $L = 8$ μm to 0 V at $L = 0.2$ μm (see Figure 3). N-channel transistors manifested similar trend; however, the decrease was much smaller (on the average, from 550 to 420 mV) and scattering of the data was larger.

Table 3. Threshold Voltages of the FD FETs.

| Gate | Mean V_{th} | Std. Dev. | Std. dev/avr, % |
|------------|---------------|-----------|-----------------|
| N-ch front | 560.2 mV | 65.8 | 11.7 |
| N-ch back | 8.3 V | 0.5 | 5.7 |
| P-ch front | -609.6 mV | 23.2 | 4.4 |
| P-ch back | -9.4 V | 0.2 | 2.2 |

The gate length effect (or short channel effect) is well known [4] and is due to a portion of the source and drain depletion regions expanded under the gate.

The gate width had a similar effect on V_{th} as the gate length (see Figure 4). A decrease in the gate width from 100 μm to 0.5 μm increased V_{th} values for P-channel transistors from approximately -500 mV to -350 mV and decreased V_{th} for N-channel transistors from 600 mV to 250 mV. The back-channel transistors behaved similarly (see Figure 5).

This behavior is different compared to what is known for the bulk-Si transistors [5], where the absolute value of the threshold voltage had a trend to increase with decreasing channel width. For SOI devices, the trench isolation does not allow spreading the depletion layer outside the silicon island. Besides, the parasitic conduction if the side wall transistor may play an important role in the short-width devices. For these devices the depletion layer at the mesa isolation oxide plays a similar role as the source and drain depletion layers in the short-length-gate transistors.

3.2 Subthreshold Slope

Average subthreshold slope values, their standard deviations, and variations from the calculated minimal values for basic-technology, 0.25 μm transistors are shown in Table 4. It is seen that the reproducibility of the S values is below $\sim 10\%$ except for the back channel in the NMOS transistors, where it reached $\sim 20\%$.

Table 4. Subthreshold Slope, mV/decade.

| Gate | Average | Std.dev. | (S-Smin)/Smin, % |
|------------|---------|----------|------------------|
| N-ch front | 80 | 9 | 29 |
| N-ch back | 960 | 210 | 91 |
| P-ch front | 99 | 5 | 60 |
| P-ch back | 1110 | 98 | 120 |

The measured values for the front-gate channels are 30-60% larger and for the back-gate channel 90 – 120% larger than the corresponding theoretical minimal values. Formal calculations in accordance to the Eq. 1 and 2 show that similar increase in S could be due to the presence of interfacial traps with a density of 8×10^{11} to $1.7 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ for the front gate, and of 1.1×10^{12} to $1.5 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ for the back gate. The calculated interface density for the front channels transistors are 1-2 order of magnitude larger than the typical values for comparable technology. A relatively high density of interface states at the buried oxide-SOI is usually expected; however, several sources of errors, which might have affected these calculations, should be considered.

First, the values in Table 4 were measured at accumulation at the opposite interface ($V_{g2} = -10\text{V}$ for the front gate measurements and $V_{g1} = -1 \text{ V}$ for the back gate measurements). However, it is known that the minimal values of S could be obtained at less severe accumulation conditions, or at the onset of formation of a depletion layer. This might decrease the S values at the front gate to the level, where application of this D_{it} extraction technique is not accurate any more (the level below $0.5 \cdot 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ [6]). Experiments showed (see Figure 6) that for both, the front and the back gates, the minimal level of the S could be approximately 10% less, than those shown in Table 4. Even at less severe accumulation conditions at the opposite interface, the subthreshold slope still remains larger than the theoretical minimum.

Another, and probably more significant source of errors in calculations using average S values, is due to the size effect. Figures 7 and 8 show that both, the front and the back gates exhibited a strong gate length effect. The minimal values, which are very close to the theoretical minimum were observed at $L = 2 \mu\text{m}$ in the P-type transistors and at approximately $0.5 \mu\text{m}$ in N-type transistors. A decrease in the gate length below these values, resulted in an increase by a factor of more than two times, the subthreshold slope. Similar behavior in the submicron FD SOI devices was observed in [7], where the S increased approximately 50%, when the drawn gate length decreased from $1 \mu\text{m}$ to $0.18 \mu\text{m}$ in both N- and P-channel devices.

Variations of S with the gate length for the front channels in N- and P-type transistors are not that dramatic. However, the trend is similar and the minimum values (which are still approximately 15% larger than the theoretical minimum) are obtained in transistors with the gate length of $0.4\text{-}0.5 \mu\text{m}$.

The subthreshold slope variations with the gate width were much less significant; however, a trend of monotonically decreasing S with the gate width decrease was

observed (see Figure 9). In the P-channel transistors, S decreased approximately 10% and in the N-channel transistors by approximately 25% over the range from 100 μm to 0.5 μm .

3.3 Mobility of the Charge Carriers

The average values of mobility of the charge carriers in N- and P-type transistors calculated for the gate length of 0.25 μm are displayed in Table 5. Also, the values of mobility in the bulk silicon doped to a $4 \times 10^{17} \text{ cm}^{-3}$ level are shown for reference purposes.

The front gate mobilities in transistors of both types were approximately 20-30% less than the volume values, which is usually explained by additional scattering at the Si/SiO₂ interface. The back channel mobility was significantly larger than the front gate mobility, contrary to what was expected. One of the possible explanations is that due to silicon inclusions in the SIMOX, the effective capacitance of the buried oxide is less than the one calculated for 170 nm thick oxide. Another possible reason is a decrease in the doping level at the buried oxide-SOI interface.

Table 5. Mobility, cm^2/Vs , for gate length $L = 0.25 \mu\text{m}$

| Gate | μ average | Std.dev. | μ_0 (bulk Si) |
|------------|---------------|----------|-------------------|
| N-ch front | 268 | 67 | 400 |
| N-ch back | 487 | 117 | 400 |
| P-ch front | 158 | 217 | 200 |
| P-ch back | 466 | 36 | 200 |

The gate length did not change any significantly, the mobility of carriers for the front gate in N-channel transistors, and approximately increased by two times, the μ values in the P-channel transistors when the gate length decreased from 8 μm to 0.2 μm (see Figures 10). The back gate mobility in the submicrometer region increased dramatically (approximately 3 times for PMOS and 2 times for NMOS transistors) when the gate length decreased below 0.5 μm .

A strong gate size effect on the degradation of the electrical characteristics of SOI MOSFETs with STI structures was reported in [8]. The degradation was due to a decreased mobility in N/P MOSFETs, which is believed to be caused by the interface roughness (or damage) at the STI gate edge location. This degradation becomes significant with a decrease in channel width and increase in channel length. These results qualitatively agree with the experimental data obtained. However, the edge effect appears to be much stronger than for the reported STI structures.

3.4 Effective Dimensions

Calculations of the transconductance parameter K (see Eq.4) for transistors with different drawn gate width (W_{mask}), and length (L_{mask}) allow estimations of the effective channel length and width, which might deviate from the drawn values:

$$W = W_{\text{mask}} - \Delta W, \text{ and } L = L_{\text{mask}} - \Delta L,$$

where ΔW and ΔL are the channel width and length reduction due to possible lateral diffusion and/or overetching during the gate definition process.

Substituting W and L in Eq. (4) gives the following equations [6]:

$$\frac{K^2}{V_d} = \frac{\mu C_{\text{ox}}}{L} (W_{\text{mask}} - \Delta W)$$

$$\frac{V_d}{K^2} = \frac{1}{\mu W C_{\text{ox}}} (L_{\text{mask}} - \Delta L)$$

When the K^2 value is plotted against the drawn gate length or K^{-2} value is plotted against the drawn gate width, the intercept with the X axis gives ΔW and ΔL values. In the measurements obtained, the mobility of carriers also varied with the gate size, so the corresponding corrections were made when performing these calculations. Typical plots are shown in Figure 11 and the results of calculations are summarized in Table 6.

Table 6. Deviation of the Drawn Gate Size.

| Gate | $\Delta L, \mu\text{m}$ | $\Delta W, \mu\text{m}$ |
|------------|-------------------------|-------------------------|
| N-ch front | 0.004 | 0.019 |
| N-ch back | 0.001 | -0.11 |
| P-ch front | 0.06 | 0.02 |
| P-ch back | -0.005 | -0.13 |

The data show that the gate size deviation from the drawn values in most cases is negligible. For a basic transistor size of $L = 0.25 \mu\text{m}$, $W = 1 \mu\text{m}$, the front gate deviation did not exceed 2%, in all cases, except for the gate length in P-channel transistors where the deviation was approximately 25%.

3.5 Gate Leakage Current

Attempts to measure gate leakage currents directly, showed that they were below the limit of HP4156 sensitivity ($< 10^{-13}$ A in the used set up). For this reason, the gate lifting technique was used. The drain current was monitored after applying corresponding bias to contact pads of a transistor following a mechanical disconnection (lifting) of the gate probe. The drain current decreased with time; thus, indicating a decrease in the gate

voltage caused by the oxide leakage current. The drain current declined exponentially with the characteristic time of the decay being $\tau = RC$, where R is the effective resistance of the oxide and C is the capacitance, allowed for calculation of the resistance.

Typical results of these experiments are shown in Figure 12. The calculations showed that the gate oxide resistance was approximately 2×10^{18} Ohm, which corresponds to negligible leakage currents in the range below femto-amperes and to the specific resistivity of the gate oxide 10^{15} Ohm*m. It should be noted that the surface conductivity is most likely, the predominant component at these levels of the leakage currents.

3.6 Edge Effect

A decrease in the gate width, significantly increases the possibility that the parasitic conduction path between the drain and source at the lateral edges in SOI MOS FETs would provide a major contribution to the leakage current in the OFF condition of transistors. The side-wall transistor, which is always formed in mesa-isolated structures, operates in parallel with the main transistor and may cause failures of SOI devices.

Analysis of more than 100 different transistors performed in this work, did not reveal any excessive leakage currents, which might be related to the edge effect, (except for one case, where the current was approximately 10^{-11} A).

A small hump in the transconductance versus front gate voltage appeared in N-channel transistors at $0.3\text{V} < V_{g1} < 0.7\text{V}$ and $V_{g2} = -10$ to -20 V, as the gate width decreased below 2 μm (see Figure 13). This hump was most likely caused by parasitic leakage along the mesa oxide at the edge of the transistors.

A difference in the behavior of transistors with different gate widths should be noted. A decrease in the transconductance (G_m) with increasing inversion bias is typical for MOS FETs and is due to a mobility degradation at high electric fields. In the measurements obtained, the transconductance at $V_{g1} > 1$ V and accumulation conditions at the back channel ($V_{g2} < 0$) decreased much more significantly in transistors with large W compared to the micrometer-range-width transistors (the decrease was approximately 10 times for $W = 100 \mu\text{m}$ and 3 times for $W = 0.5 \mu\text{m}$). Besides, a decrease in the $G_{m_{\text{max}}}$ at $V_{g2} > 0$, which is due to the minority carriers building up deeper into the SOI film (the volume inversion effect) [3], is also much more pronounced for the wide-gate transistors.

For PMOS FETs neither transconductance humps in small-width-gate transistors, nor the volume inversion effect were observed (see Figure 14). However, a decrease in G_m due to the field effect was also much larger for the wide-gate transistors.

The back channel variations of transconductance with front and back gate voltages appeared to be more complicated than the one for the front channels. Figure 15 shows example of the $G_m(V_{g2}, V_{g1})$ dependencies for transistors with the gate length of 0.25 μm and width of 0.5 μm (Figure 15a) and 100 μm (Figure 15b). Transconductance peaks at $V_{g2} < -15$ V are due to the front channel activation at strong accumulation at the back gate and depleting/inversion conditions at the front gate. Transconductance behavior at $V_{g2} > 0$ was similar to what was observed for the front channels and is due to the electric field effect and the volume inversion effect. The origin of the wide peaks in the range -5

$< V_{g2} < 2 \text{ V}$ is possibly related to the volume inversion effect, but additional analysis of the curves is required. However, no anomalies in the back channel transconductance, which would be directly related to the edge effect, were observed.

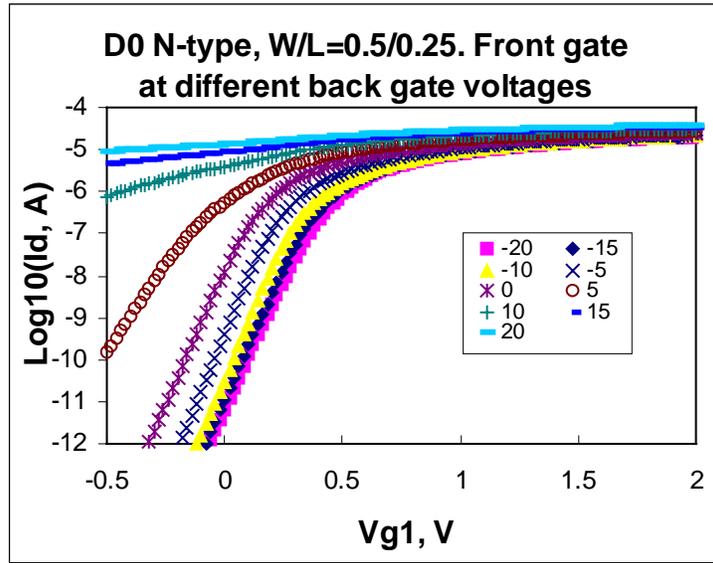
4.0 Conclusions

The front- and back-channel N- and P-type transistors manufactured in MIT/LL 0.25 μm SOIFD technology were fully characterized using three process monitor dice with 40 transistors in each die (the gate length varied from 0.2 μm to 8 μm and the gate width varied from 0.5 μm to 100 μm). The test results are summarized below.

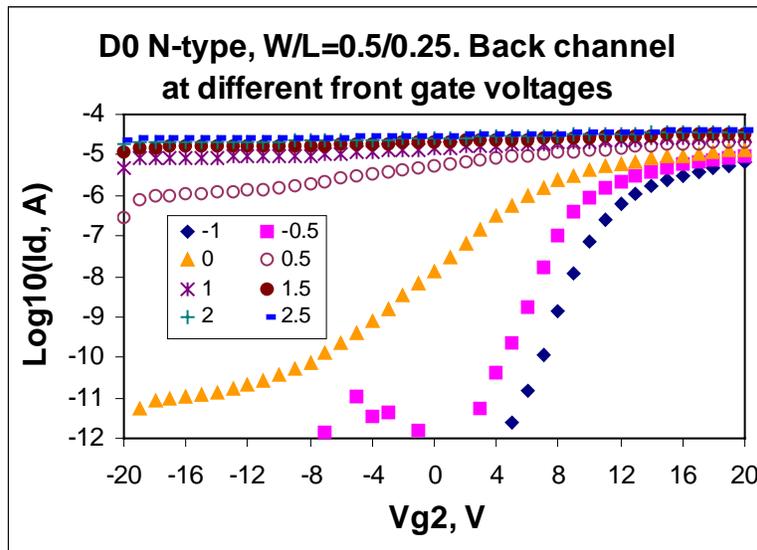
- The variations in the threshold voltage and the subthreshold slope did not exceed 12% and 20% (respectively for V_{th} and S). Characteristics of the front channels in NMOS FETs were much less reproducible than for the PMOS transistors.
- Both N- and P-channel transistors exhibited the short channel effect. The absolute values of the threshold voltage decreased significantly below 0.5 μm . The effect was most pronounced for PMOS transistors. A decrease in the gate width, also resulted in a decrease of the absolute value of the threshold voltage.
- The subthreshold slope also showed a strong gate-length dependence, significantly increasing in the submicrometer region (more than twice for the back channel, and approximately 15% - 25% for the front channel transistors).
- The mobility of the charge carriers virtually did not change with the gate length for the front-channel NMOS transistors and increased for the PMOS transistors when the gate length decreased below 0.5 μm .
- Electrical measurements showed that the gate length deviations did not exceed 2% of their drawn value.
- The specific resistance of the gate oxide was approximately $10^{15} \text{ Ohm}\cdot\text{m}$ and the gate leakage current was in the femto-ampere range.
- The parasitic side-wall transistor at the gate edge resulted in some deviations of the transconductance characteristics for the NMOS transistors with the gate width below 2 μm . However, no excessive leakage currents in the OFF condition of the transistors, or any other significant anomalies were observed.

References

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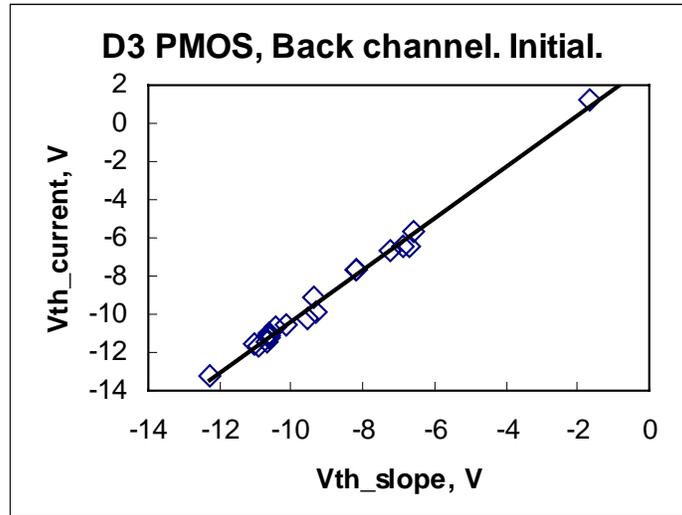


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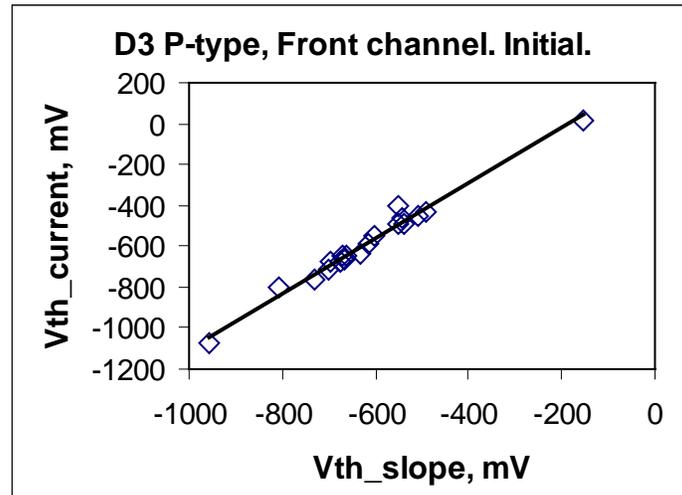


b)

Figure 1. Typical transfer characteristics of the transistors showing strong coupling effect.

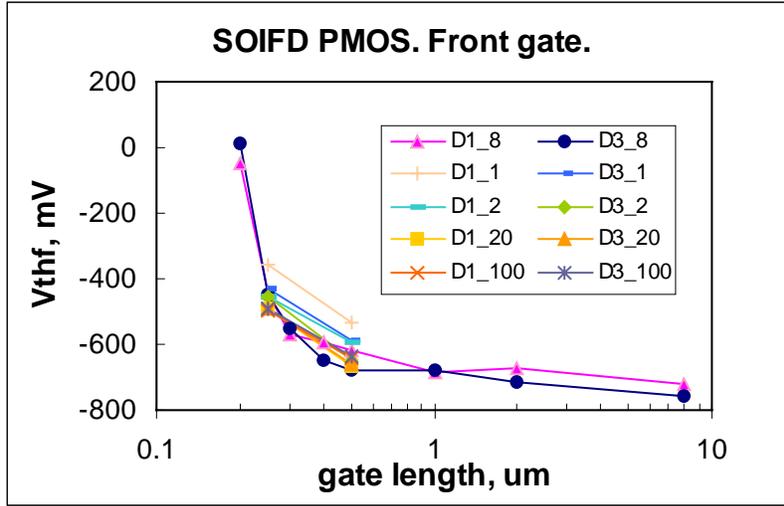


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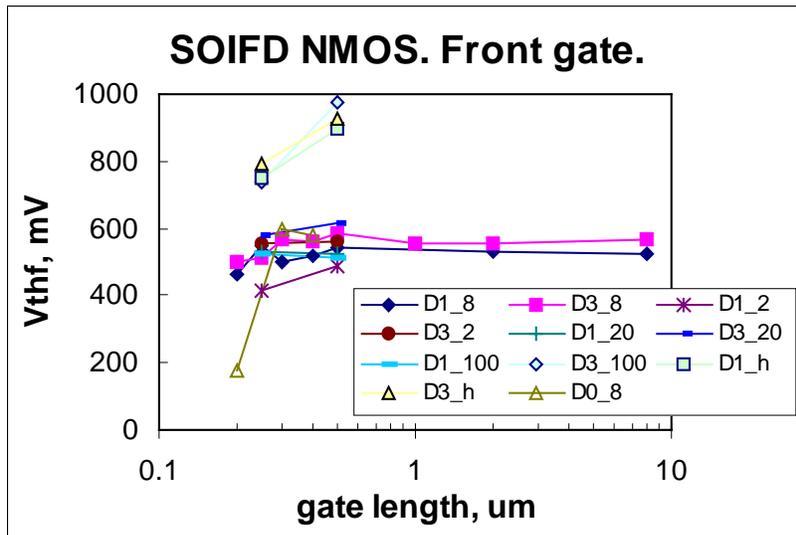


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Figure 2. Typical results of the threshold voltage measurements showing correlation between the two methods.

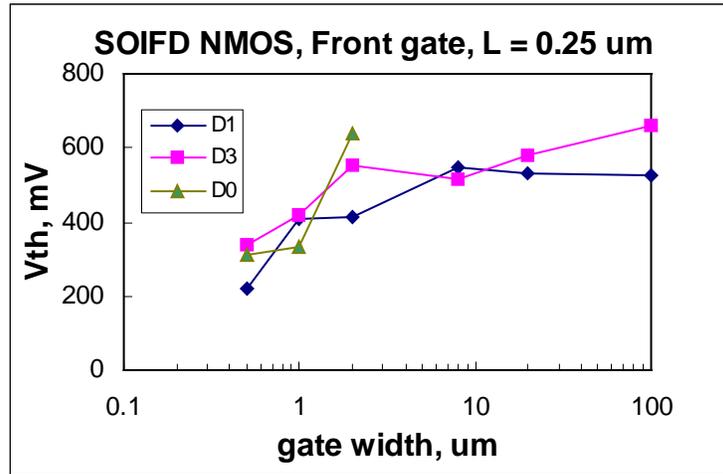


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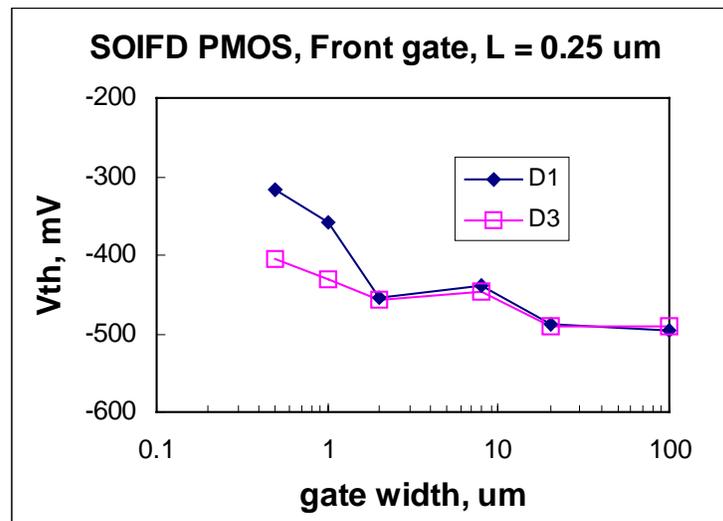


b)

Figure 3. Short channel effect in the PMOS (a) and NMOS (b) SOIFD transistors.

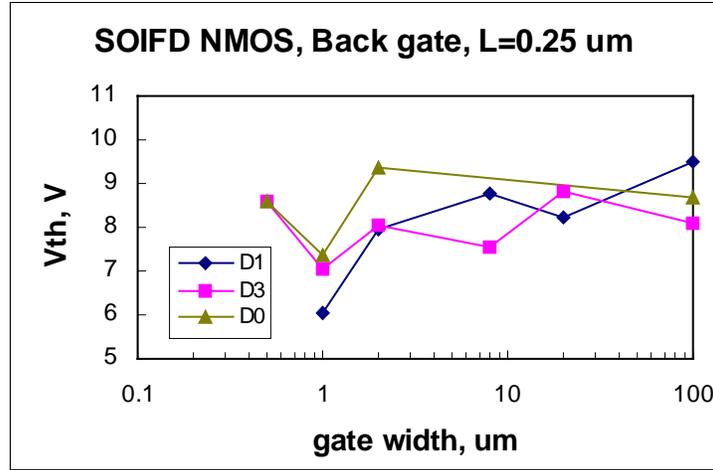


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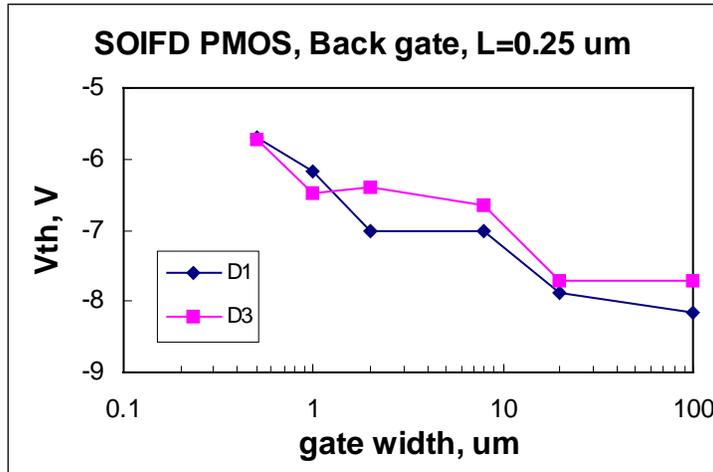


b)

Figure 4. Gate width effect on the threshold voltage.

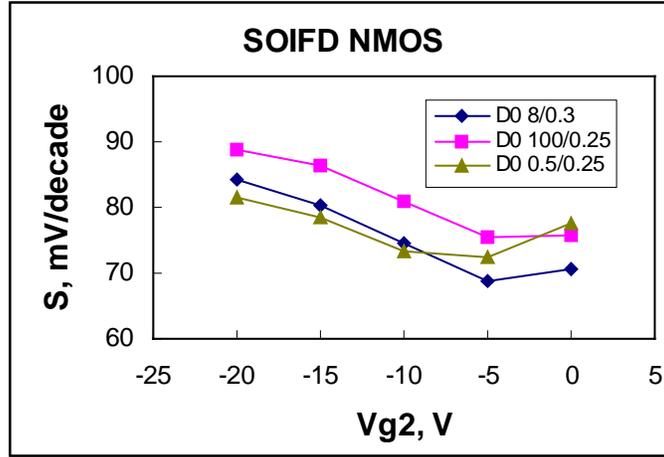


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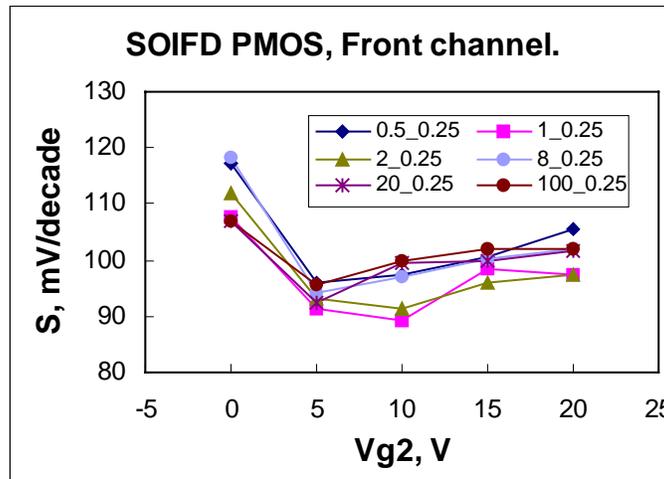


b)

Figure 5. Gate width effect in the back-channel transistors.

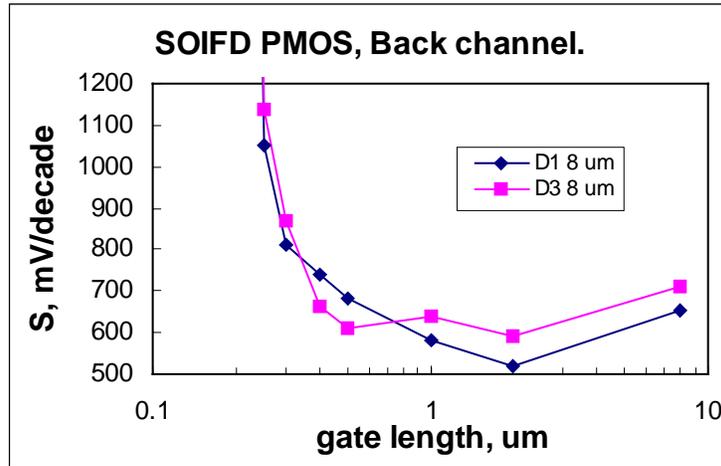


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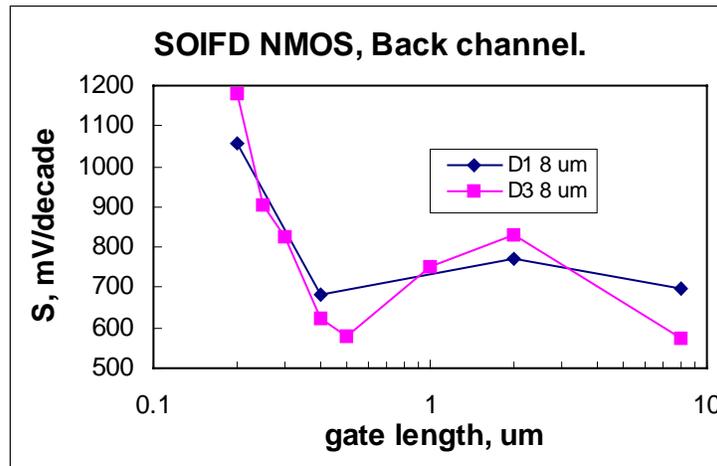


b)

Figure 6. Back gate effect on the subthreshold slope in front-channel transistors.

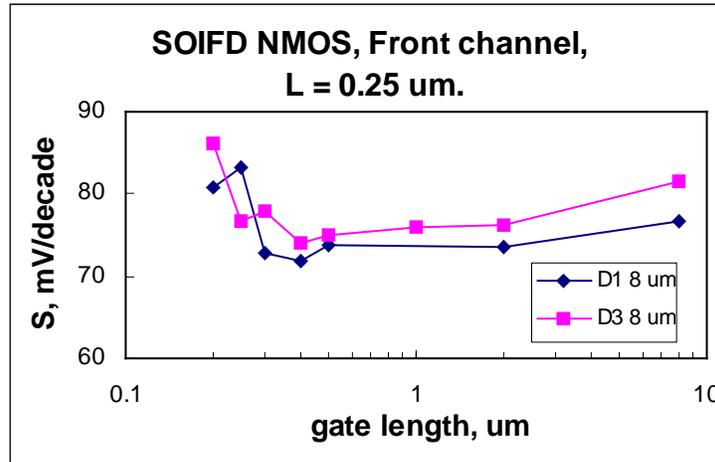


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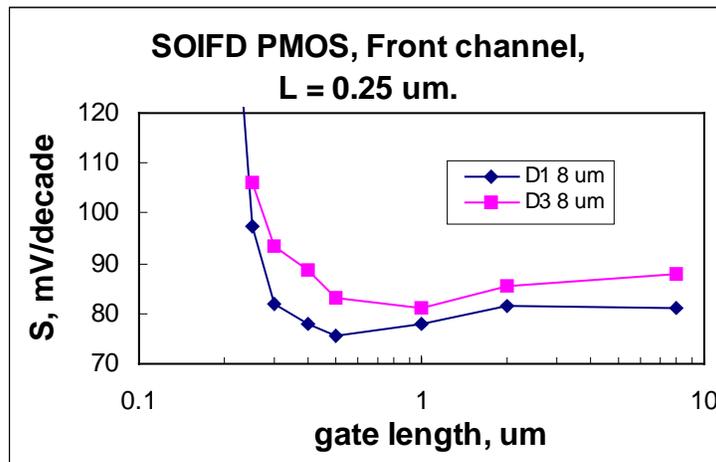


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Figure 7. Gate length effect on the subthreshold slope in back-channel transistors.

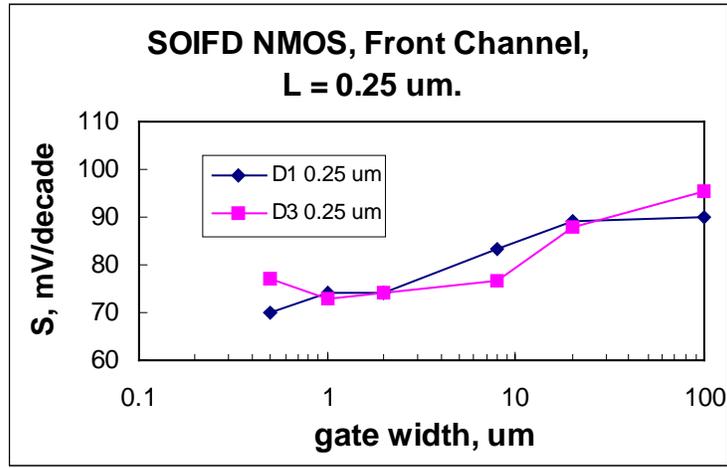


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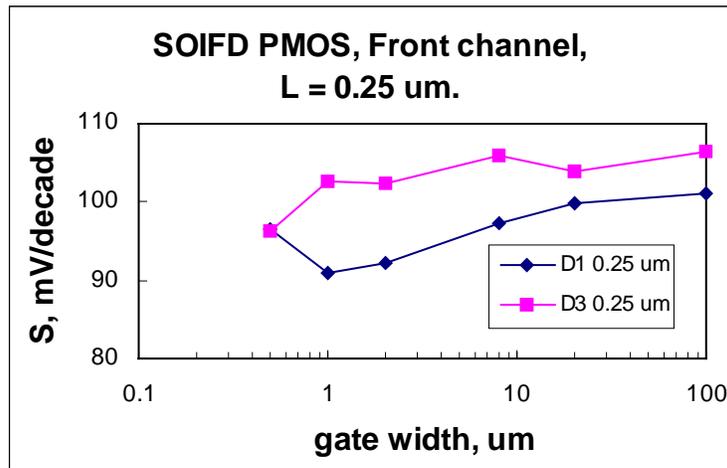


b)

Figure 8. Gate length effect on the subthreshold slope in front-channel transistors.

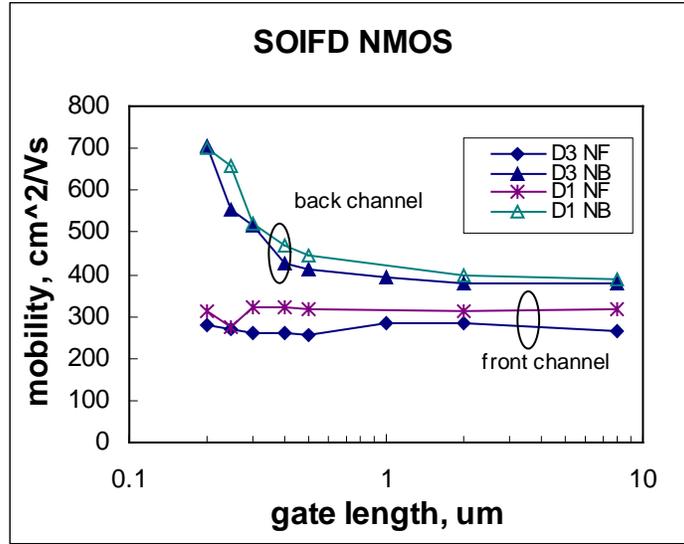


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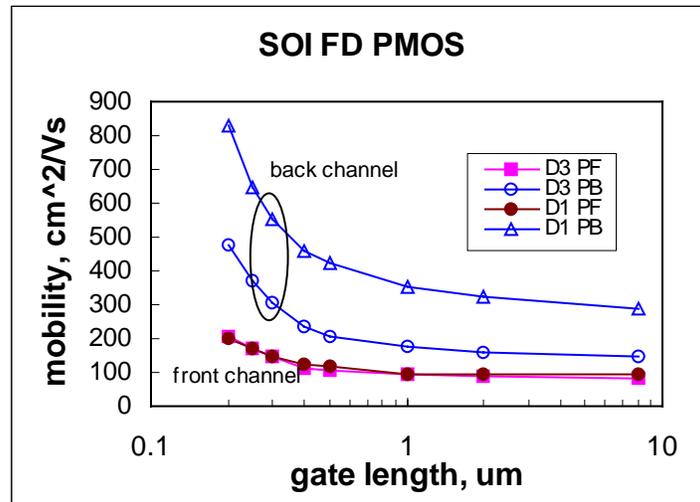


b)

Figure 9. Gate width effect on the subthreshold slope in front-channel NMOS (a) and PMOS (b) transistors.

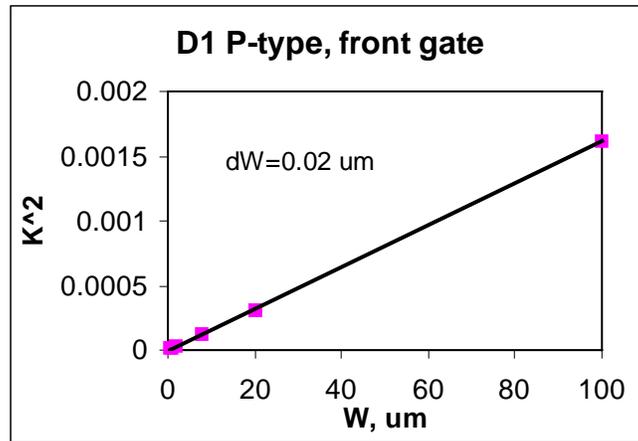


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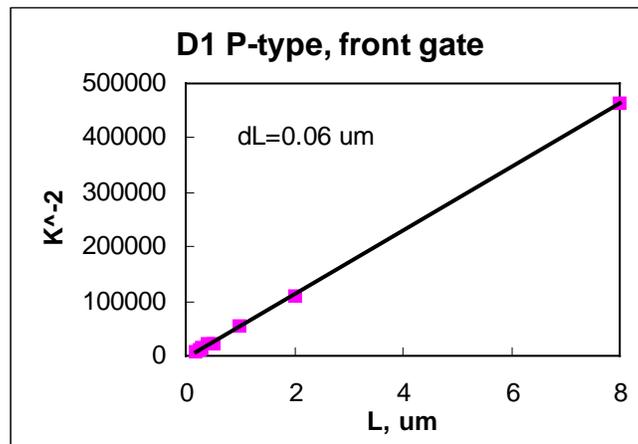


b)

Figure 10. Gate length effect on the mobility of the carriers in NMOS (a) and PMOS 9b) transistors.

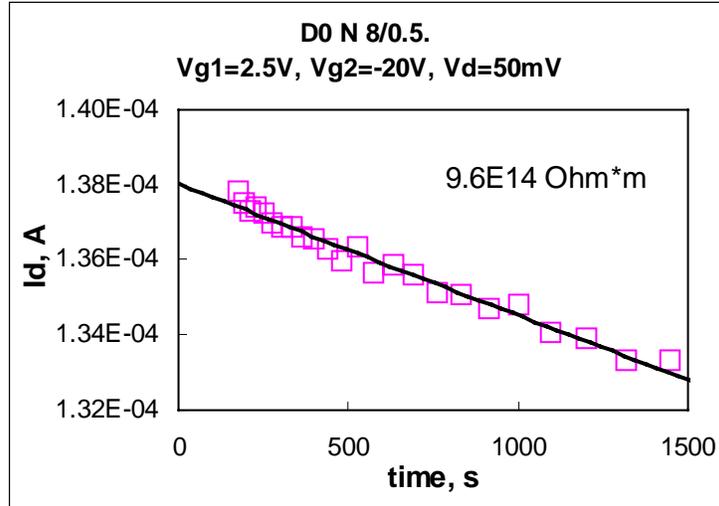


a)

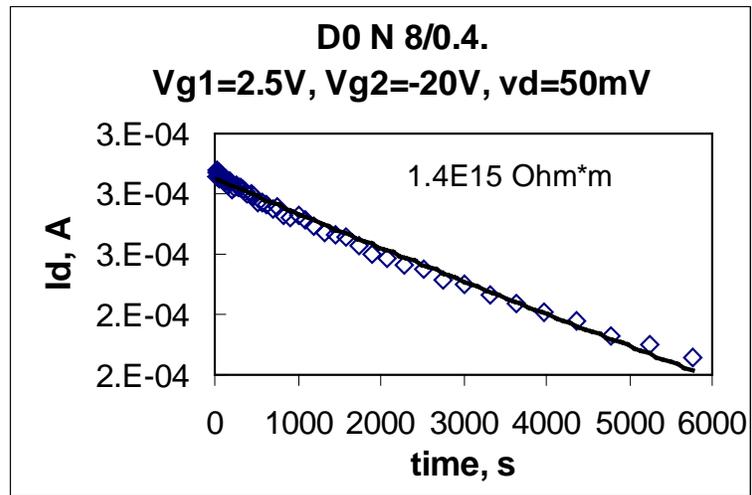


b)

Figure 11. Functions of the K-factor, K^2 in (a) and K^{-2} in (b), versus the drawn gate width (a) and length (b) allow for estimation of the gate size deviations.



a)



b)

Figure 12. Gate probe lifting experiment results.

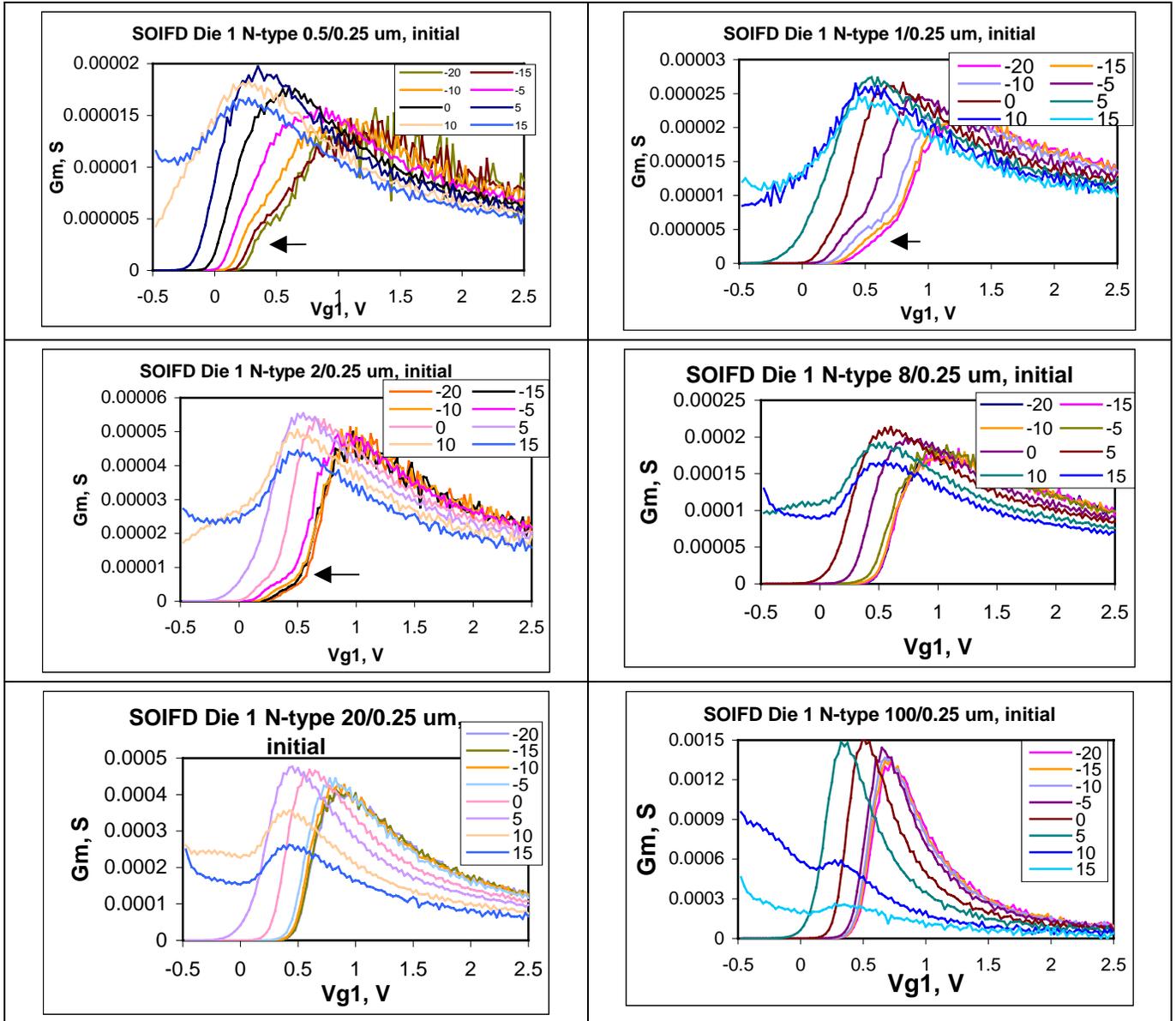


Figure 13. Transconductance in SOIFD NMOS with the gate length of $0.25 \mu\text{m}$. The back gate voltage varied from -20V to $+15\text{V}$ in 5V step. Different charts correspond to different gate width indicating edge effect in transistors with the gate width below $2 \mu\text{m}$ (at arrows).

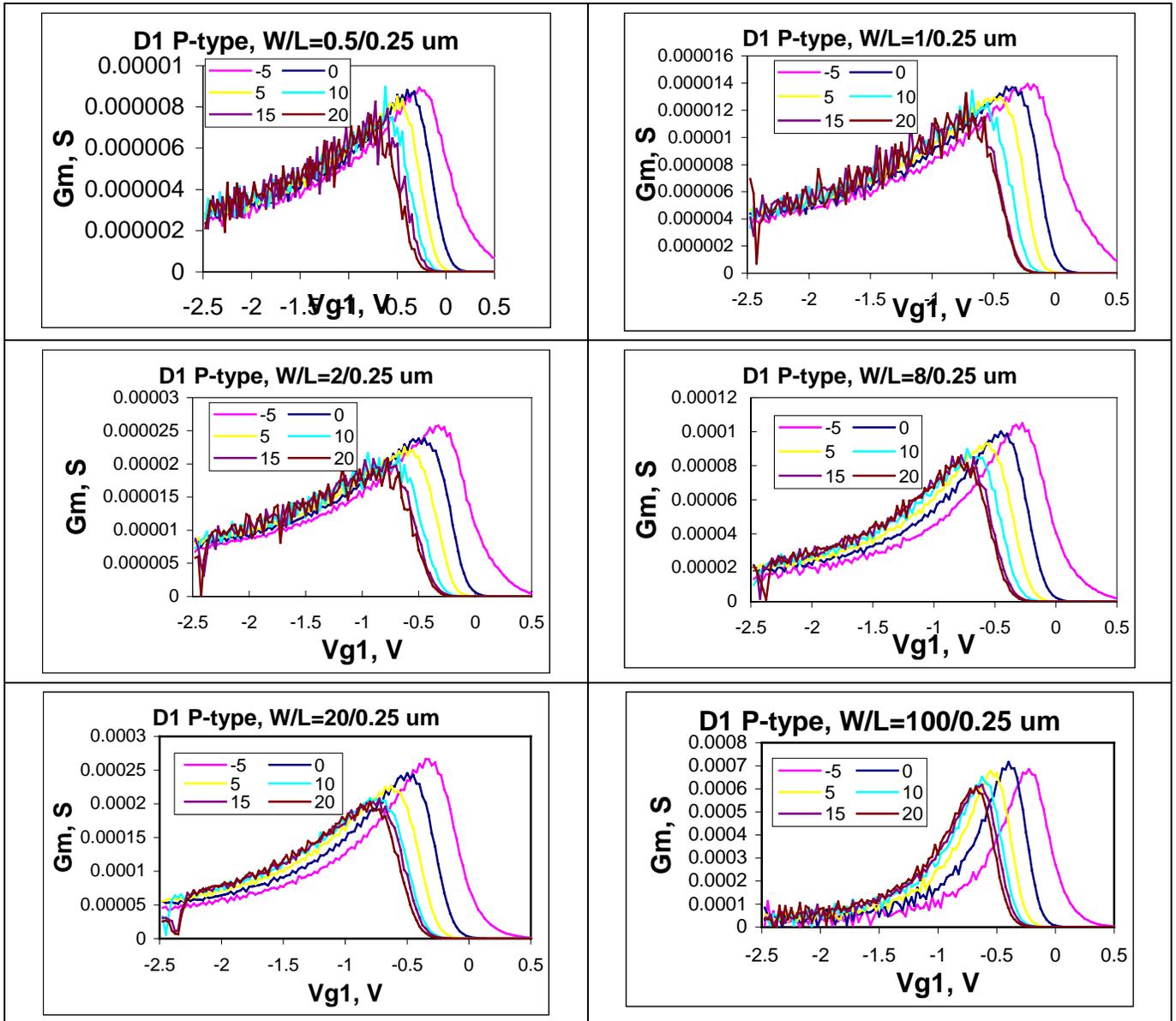
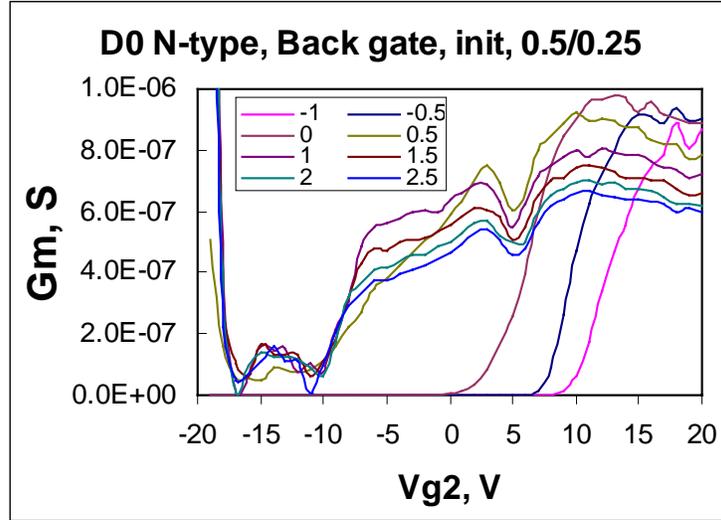
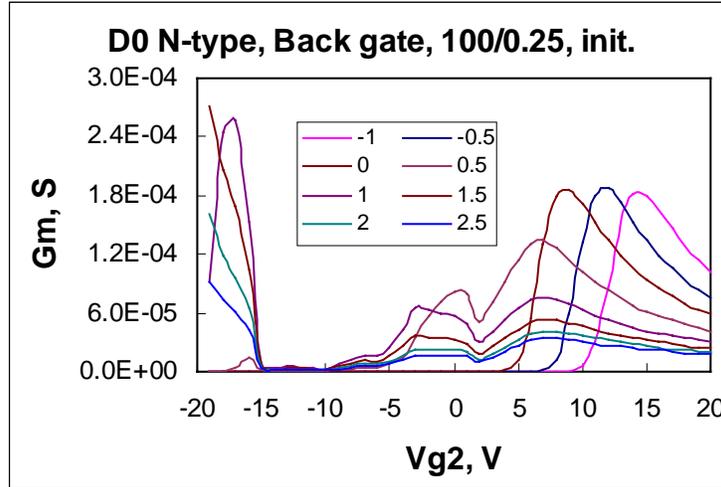


Figure 14. Transconductance in SOIFD PMOS with the gate length of $0.25 \mu\text{m}$ at back gate voltages varying from +20V to -5 V in 5 V step. Different charts correspond to different gate width. No edge effect in transistors was observed.



a)



b)

Figure 15. Back gate transconductance for two NMOS FETs with gate length 0.25 μm and width of 0.5 μm (a) and 100 μm (b).