C02-03 Embedded Passive Reliability and Tradeoff Analysis

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Objectives:

I. Evaluate the reliability of embedded (integral) resistors and capacitors through environmental testing of layer pairs and multilayer boards containing embedded components.
II. Extend and verify application-specific size/cost tradeoff analysis models developed in the C01-11 project.

Background:

The use of discrete passive components (resistors, capacitors and inductors) in electronic systems has continued to increase even as the degree of system integration has increased. This trend not only requires more passives to be and assembled to the system, but also suggests that discrete passives will consume increasing amounts of board area and assembly time. Passives that are fabricated within printed circuit boards (integral passives) are one approach that is being explored to address these trends. While integral passives will never replace all passive components, they provide a potential advantage for many applications including: increased circuit density through savings in board real-estate, decreased product size and weight, improved electrical properties through additional termination and filtering opportunities and shortening electrical connections, cost reduction through increasing manufacturing automation, increased product quality through the elimination of incorrectly attached devices, and improved reliability through eliminating solder joints.

In the CALCE C01-11 project, embedded passive technologies were reviewed and a technology tradeoff analysis capability (size and cost estimation) for assessing the use of embedded passives on an application specific basis was developed and implemented within a web-based analysis tool. Using this analysis capability, several applications were assessed and general conclusions about embedding bypass capacitors were drawn. Besides maintaining this tradeoff capability (updating the technologies modeled), additional tradeoffs remain to be addressed in order to build a complete picture of the applicability of embedded passives to a particular system. The additional effects include reliability, assessing the amount of bypass capacitance needed when discrete capacitors are converted to embedded, and supporting various technology mixing scenarios (for example, using both Ohmega Ply for large value embedded resistors and screen printing for small value resistors in the same board) that are likely to occur in real applications.

Approach:

This project will collaborate with the NIST Advanced Embedded Passive Technology (AEPT) program to obtain test vehicle designs. Layer pairs and multilayer boards for reliability testing of embedded resistors (and possibly capacitors) will be fabricated. CALCE in-turn will share the environmental testing results with the AEPT program, CALCE members. All reliability testing results will be delivered within the Embedded Passives Webbook developed in C01-11.

Updates to the tradeoff analysis methodology will include laser trimming models, generalization of board costing results, additional case studies, and extension of the tool to accommodate integrated passive tradeoffs. All updates to the tradeoff analysis methodology will be delivered as upgrades to the web-based analysis tool developed within C01-11.

Deliverables:

- Tradeoff analysis methodology upgrades delivered within the existing web-based analysis tool.
- Embedded resistor (and possibly capacitor) reliability assessment results.
- Technology and materials updates to the technology review web-book developed in C01-11.

ID	Task Name
1	**Tradeoff Tool Extensions**
2	Laser trimming models
3	Generalization of board costing
4	Cadence integration
5	More case studies
6	Integrated passive tradeoffs
7	**Board Reliability Analysis**
8	Resistor board fabrication
9	Resistor board testing
10	Webbook Updates