TOTAL IONIZING DOSE EFFECTS ON 64Mb 3.3V DRAMs*

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Abstract

64Mb 3.3V CMOS DRAMs from two different manufacturers were tested for total dose. Retention time, power supply current, and functionality were used to characterize device response. Burned-in devices failed functionally at lower total dose levels. Results showed that these scaled DRAMs are about twice as hard as older generation 16Mb commercial DRAMs.

I. INTRODUCTION

Next generation space systems will require high data rate and large memory capacity for high resolution and accuracy of data information. The never-ending drive for higher density DRAMs continues to pack more transistors on a single chip, increasing operating speed and reducing power consumption. Therefore, DRAMs, microprocessors, and multi-mega-gate logic chips must achieve high speed, fast clock access, and consume just a few milliwatts. As the memory density increases, smaller cell size and lower standby current for low cost and low power are major requirements for DRAM developments and applications, particularly in solid-state recorders, which are key systems for many new space programs. High density DRAMs require scaling of the capacitor, line widths, and spacing, thinner oxides, and lower operating voltage. Experimental DRAMs with 1Gb have been developed [1]. Although 64Mb DRAMs were available in 1993, they are just entering mass production.

In this paper, 64Mbit DRAMs from two leading manufacturers, Samsung and Mitsubishi, are tested for total dose and characterized for burned-in effects. These are extended data out (EDO) mode and fast page mode CMOS 3.3V DRAMs for high-speed and low-power applications. Both device types were in plastic packages, typical of commercial DRAMs. Some of the devices were subjected to burn-in before irradiation to determine the effects of burn-in on total dose response for these devices. Previous work has shown that total dose effects in CMOS devices can be affected by burn-in. [2]

II. EXPERIMENTAL APPROACH

Five devices were irradiated with a cobalt-60 room type irradiator at room temperature and dynamically biased with a 10 MHz clock during irradiation. An Advantest VLSI test system (T3342) was used for electrical characterization and dynamic bias. This Advantest test system has two test heads; one (shielded) inside the radiation cell area and the other one with the main frame. Devices were irradiated at 10 rad(Si)/s with in-situ dynamic bias using a 10 ft cable from the test head inside the radiation cell. After irradiation, the device was taken out of radiation room and electrical measurements were made at another test head for better measurement with precision and full clock speed. A test program was designed to characterize data retention time. A separate test program was used to measure supply currents while providing dynamic bias to devices. Retention time was measured by writing ones to all memory cell locations, waiting for a specified time before refreshing, and then finally reading ones from all cell locations to determine the number of cells that had already changed state. Standby and dynamic power supply current were also measured until functional failure.

Five different devices were burned-in at 125 °C for 168 hours to study burn-in effects. Devices were dynamically biased with continuous writing marching 1's and 0's to memory cell locations and verifying them to ensure that the high temperature is not causing any degradation to the devices. After devices were burned-in, they were characterized using the same procedure as that for the non burned-in devices prior to irradiation. A few parameters were slightly higher for the burned-in parts that for the parts that were not subjected to burn-in.

III. TEST RESULTS

A. Samsung 64Mb DRAM: KM48V8004A

This is a 8Mx8 bit 3.3V CMOS DRAM with extended data out (EDO). EDO mode DRAMs offer high speed random access of memory cells within the same row. Devices are fabricated with Samsung's advanced CMOS process to achieve high bandwidth and low power consumption.

Standby current during total dose irradiation is shown in Figure 1. The initial standby current was about 40 μA and increased only slightly to a total dose level of 20 krad(Si). At 30 krad(Si), the standby current increased rapidly to about 1.9 mA, but did not increase further at the final total dose level of 70 krad(Si) where the device failed functionally. This is not a typical response of CMOS device which usually show more gradual increase in power supply current, with saturation at much higher currents.

* The work described in this paper was carried out by the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration Code Q. Work funded by the NASA Microelectronics Space Radiation Effects Program (MSREP).

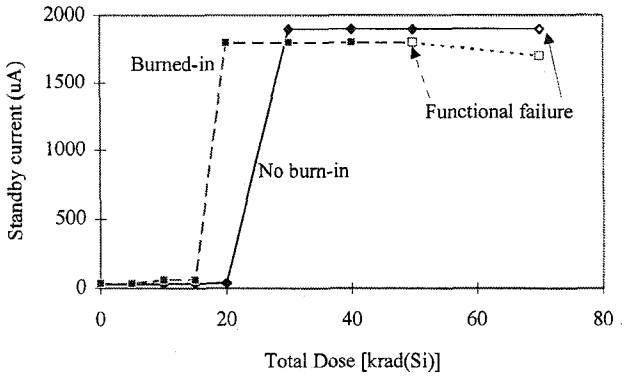

Figure 1. Samsung 64Mb DRAM standby current degradation.

The standby current of burned-in devices started out at about 28 μA and increased only slightly to levels below 15 krad(Si). It is shown as a dashed line in Figure 1. The current increased rapidly above 15 krad(Si), a lower level than that of the non-burned-in devices, and remained at 1.8 mA, a slightly lower value until the functional failure at 50 krad(Si). The overall current degradation curve was very similar for both burned-in and standard devices. However, the non-burned-in devices stayed slightly higher at after 20 krad(Si) than burned-in devices. After burned-in devices failed functionally at 50 krad(Si), devices were further irradiated to observe any increase in current. The standby current decreased a very small amount (0.1 mA) at 70 krad(Si).

Dynamic power supply current was also measured for burned-in Samsung devices and it is compared with Mitsubishi devices in Figure 2. The dynamic current was about 37 mA initially and remained unchanged to 30 krad(Si). It then started to increased rapidly after 30 krad(Si) and almost doubled in value at 70 krad(Si). The Mitsubishi devices showed only a small increase in dynamic current until functional failure at 50 krad(Si) and it increased only slightly at 70 krad(Si). It is interesting to note that dynamic current behaved quite differently even though the process technologies are almost identical. This will be further discussed in later section.

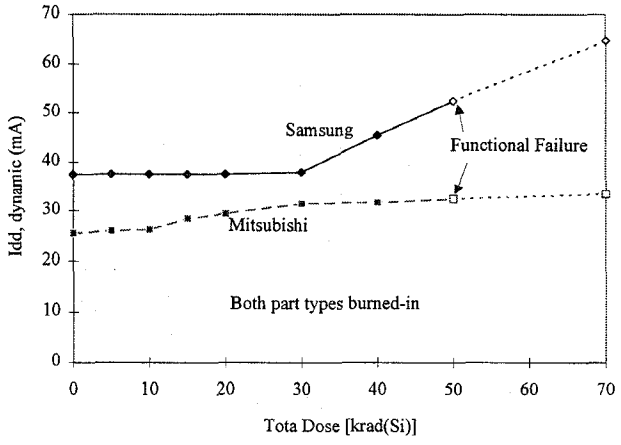

Figure 2. Comparision of dynamic power supply current degradation of burned-in devices. [Functional failure was observed at 50 krad(Si).]

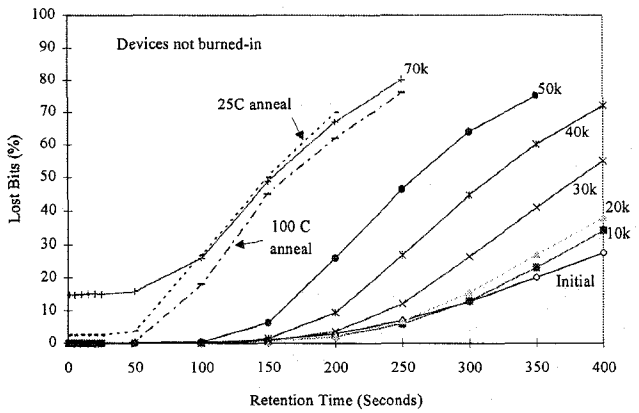

Figure 3. Samsung 64Mb DRAM retention time degradation. [Functional failure was observed at 70 krad(Si).]

Data retention time was measured on Samsung's non-burned-in devices. Percentage of lost bits among 64Mb vs. retention time (which is the actual time in seconds since the last refresh cycle) is plotted in Figure 3. The retention time decreased as the radiation level increased. Note that the slope of the retention curve increased as well. At 70 krad(Si), the device failed functionally and almost 15 % of bits were missing at zero retention time. The device was annealed for 24 hours at room temperature and showed some recovery during room temperature annealing. However, the device functioned erratically after room temperature annealing. The device was fully recovered after high temperature (100 °C) anneal for 24 hours and the slope of the retention time curve returned to almost the same value as the post 70 krad(Si) curve, but did not have any missing bits between zero to 50 seconds.

Burned-in devices failed functionally after 50 krad(Si), a significantly lower level compared to 70 krad(Si) with non-burned-in devices as shown in Figure 4. The gradual degradation of retention time up to 50 krad(Si) is very similar with and without burn-in devices (compare Figure 3 and 4). The sudden functional failure at 70 krad(Si) with burned-in devices is definitely due to the burn-in effect. Devices recovered function-

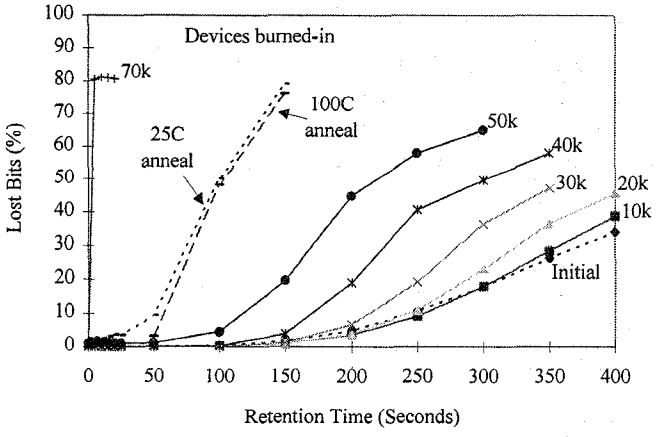

Figure 4. Burned-in Samsung 64Mb DRAM retention time degradation. [Functional failure was observed after 50 krad(Si).]

ally after 72 hours at room temperature anneal. However, the retention time did not anneal much at all. The slope of the retention time increased slightly more in non-burned-in devices as the radiation level increased to 50 krad(Si) and the functional failure occurred after 50 krad(Si). The sharp increase in retention time curve at 70 krad(Si) shows that about 80 % of the 64M cells had lost their data and remained the same after 200 seconds which indicates that leakage current from access transistors and storage capacitors reached a saturation point. Devices annealed functionally after 72 hours at 25 °C and retention time annealing further after 24 hours of 100 °C, but they did not recover fully to the initial values.

B. Mitsubishi 64Mb DRAM: M5M467800AJ-6

This is a fast page mode DRAM and is functionally identical to the Samsung device. It is fabricated with double-layer aluminum process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell. It can be used at very low power dissipation and high speed applications. This DRAM uses a single 3.3 V power supply and the maximum specified standby power dissipation is only 1.08 mW.

The standby current degraded differently compared to non burned-in Samsung devices and it is shown as a solid line in Figure 5. It gradually increased from an extremely small initial value to about 1 mA after 10 krad(Si), then it gradually increased to about 3.8 mA at the final total dose level of 70 krad(Si).

The standby current of burned-in devices started out slightly higher initially than the non burned-in devices, about 28 μA. And it is plotted as a dashed line in Figure 5. The standby current increased much rapidly at 15 and 20 krad(Si) compared to the non burned-in devices. It continued to increase slightly after 20 krad(Si) until the functional failure at 50 krad(Si), and then it further increased to 6.5 mA at 70 krad(Si). The abrupt increase in current of burned-in devices at 15-20 krad(Si) is very similar to the Samsung devices. However, the standby current of Mitsubishi devices increased much larger amount after the functional failure at 50 krad(Si) where as the Samsung devices had a slight decrease in current after their functional failures.

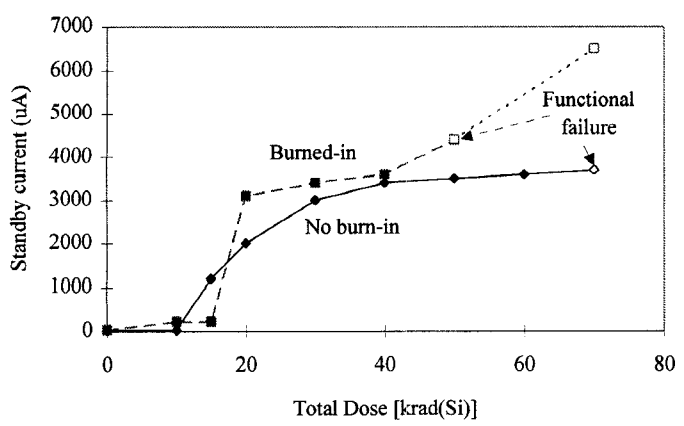

Figure 5. Mitsubishi 64Mb DRAM standby current degradation.

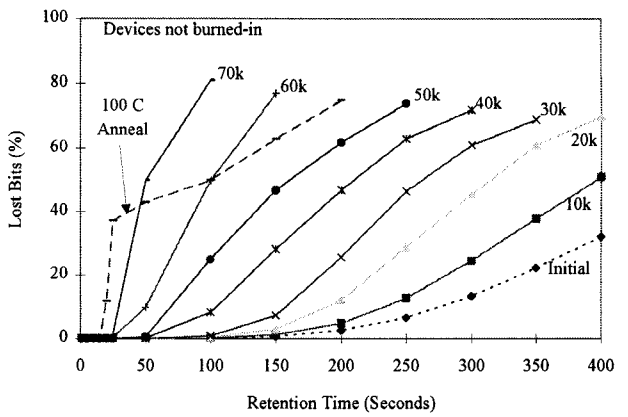

Figure 6. Mitsubishi 64Mb DRAM retention time degradation.

Dynamic power supply current of burned-in devices increased from 25.5 mA to 33.4 mA at 70 krad(Si). It degraded much less than for the Samsung devices (see Figure 2 in the previous section). The standby current showed totally opposite behaviors where the Mitsubishi devices showed almost three time higher degradation at the final total dose level of 70 krad(Si).

Retention time curves of non-burned-in devices showed slightly more gradual degradation as the radiation level increased compared to the Samsung device. As shown in Figure 6, the slope of the retention time curve is almost linear. This device failed functionally at 70 krad(Si). It did not recover after 24 hour room temperature annealing. The slope of the retention time curve remained the same after room temperature anneal. However, after 24 hours of 100 °C annealing, the device showed sudden loss of data when the refresh time interval reached 25 seconds.

Burned-in devices in Figure 7 showed slightly more degradation in retention time compared to the Samsung devices and functionally failed after 50 krad(Si). Initially, retention time measurements looks almost identical with burn-in or without burn-in. Burned-in devices showed more classical annealing responses. Devices showed some recovery after 72 hours at 25

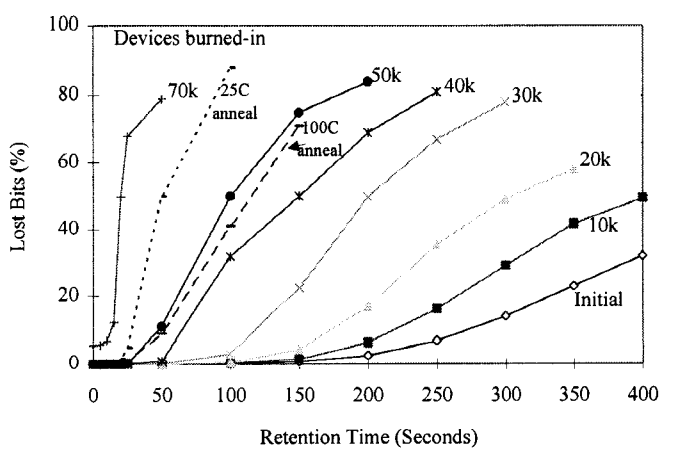

Figure 7. Burned-in Mitsubishi 64Mb DRAMs retention time degradation.

°C annealing and further annealed at 100 °C after 24 hours back to the 50 krad(Si) retention time measurements.

IV. Discussion & Summary

Both of these DRAMs are much harder than an advanced 64Mb DRAM from Micron which was previously tested in 1995. [3] Burned-in devices showed slightly lower total dose failure levels than non-burned in devices for both manufacturers. The standby current showed more degradation with burned-in devices. It is consistent with results from the previous work done on similar CMOS devices in the reference 2.

The slope of the retention time curve for both Samsung and Mitsubishi DRAMs increases as the level of radiation increases. This change in slope is mainly due to subthreshold leakage current from the access transistors.

The effective threshold voltage can be extracted from mean values of normalized retention times as discussed in Reference 2. For the Samsung DRAM as shown in Figure 8, the slope is nearly constant, which implies that oxide traps dominate the threshold voltage response. The Mitsubishi device has a similar slope and corresponds to about 20 % hole trapping for oxide thickness of 10 nm, which is the approximate thickness of 64 Mb DRAM technologies [4]. However, the magnitude of the change is greater than for the Samsung device. The previously tested Micron device showed a smooth change in retention time, but again, the magnitude of the change is much larger than both Samsung and Mitsubishi devices. These differences may be due to differences in hole trapping efficiency (note that the DRAM gate is biased negatively during most of the operation cycle).

These results show that scaled DRAMs can operate at total dose levels that are about twice as great as typical 16 Mb commercial DRAMs [5]. A similar trend has been seen in commercial SRAM technologies [6], with longer integration density, but much larger currents were observed for SRAMs than for the DRAMs in this study. Although some improvement may be anticipated because of oxide scaling, the complex architecture, boosted wordline, and lower internal voltage margins make it difficult to predict scaling effects in real DRAM circuits. [7-9]

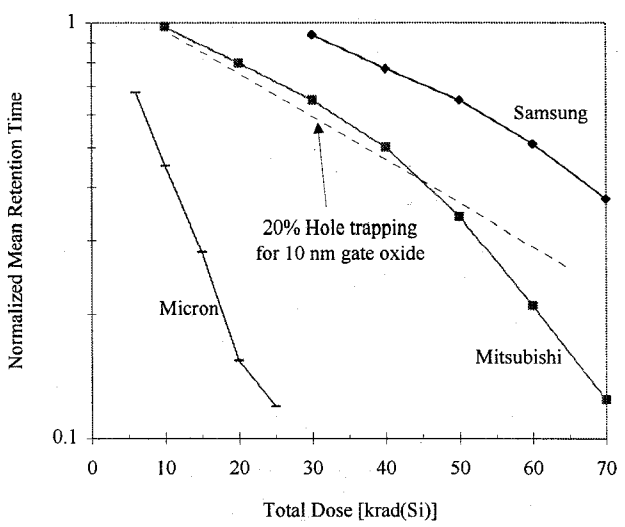

Figure 8. Median normaized retention time vs. total dose for 64 Mb DRAMs.

In addition to the improved hardness, the retention time measurements show that there are negligible cells with abnormal response, indicating that degradation is quite uniform between different cells within the device. This is very important for solid-state recorders and similar data storage applications in space systems, which can only tolerate a small number of failed bits.

Finally, burn-in caused some differences in the total dose response. Burned-in devices may fail functionally at lower total dose levels than non-burned-in devices. Even though the sample size was too small to establish any statistical confidence, all five devices showed consistent results. This latest effect on burned-in devices must be considered also for hardness assurance testing for space systems.

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