

**TITLE:** Evaluation of Silicon on Insulator (SOI) Processes for Mixed Signal ASICs, #19

**PROGRAM GROUP:** Electronic Parts Project

**PROPOSING CENTER:** JPL

**PARTICIPATING CENTER:** GSFC

**POINTS OF CONTACT:**

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**OBJECTIVES:**

Perform a comprehensive technology characterization of SOI processes in partnership with industry, academia, and government-sponsored laboratories. Provide critical information for design engineers and circuit designers relating to the characteristics and limitations of this technology for high reliability applications in an extended temperature range down to -150°C.

**BACKGROUND:**

Silicon-On-Insulator (SOI) technology is emerging as a major contender for digital and mixed signal device and circuit applications. The technology features small device dimensions (0.35 to 0.25-um gate length), high packing density, low power dissipation, high speed, and the potential for high radiation tolerance; and is of great interest to system designers, specifically for space applications. As with any new technology, there is very limited information on the characteristics of this technology over the operational temperature range, the dominant failure mechanisms, operational and reliability limitations and other environmental variables. Of particular interest are the characteristics of these devices at low temperatures (-100 °C) for applications on the Martian surface and at cryogenic temperatures for applications in instruments and sensors [Space Interferometry Mission (SIM), Space Infra Red Facility (SIR-F)]. In addition, application of mixed signal functions such as analog-to-digital converters (ADCs) is of great interest for near future applications of this technology.

**APPROACH:**

We will design test structures and simple circuits suitable for the evaluation of device and reliability parameters. Device parameters will include dc and ac transistor parameters with special attention to effects caused by the floating gates and to effects at low currents. Simple circuits such as inverters and ring oscillators will also be evaluated for extraction of switching parameters, including noise margins as function of temperature. Devices and circuits will be characterized down to -150 °C. The temperature range below -55°C is usually not addressed by commercial vendors. Reliability tests will focus on transistor-related effects, such as dielectric breakdown and hot carrier effects of gate and buried oxide, and will be performed in the appropriate temperature intervals. The thermal performance of SOI-CMOS will be evaluated and compared to that of bulk CMOS. Reliability tests focussing on (on-chip) interconnect-related effects, such as metal electromigration and stress voiding, are being addressed in a separate proposal.

The test structures will be developed, fabricated, and tested in partnership with MIT/Lincoln Lab (LL), Honeywell Solid State Electronics Center (SSEC), the JPL/System-On-A-Chip (SOAC) program, and the University of Maryland/ Microelectronics Reliability. The Lincoln Lab process features presently a fully depleted silicon layer (< 50 nm) and a 0.25-um gate length, the

Honeywell process SOI-V, scheduled for production release early in 1999, features a partially depleted silicon layer and a 0.35-um gate length. Part of Lincoln Lab's 0.25-um technology may be licensed to Honeywell for their next generation SOI process.

Honeywell plans to begin their own evaluation of the SOI-V (0.35 micron) process for mixed signal in late 1999. QML certification should be sought by mid-2000. GSFC will support DSCC qualification activity for this process by reviewing Honeywell standard evaluation circuits (SECs), test structures, technology characterization vehicle (TCV), and the qualification data.

The results of this evaluation will be disseminated via the NASA Electronic Parts and Packaging (NEPP) web site, EEE Links and technical presentations and publications.

**BENEFITS:**

The results of this task will enable design improvements and extend the range of operation to low temperatures by providing technical evaluation not otherwise available. The collaboration with the System-on-a-chip program at JPL provides a direct infusion path of SOI technology into space applications. This joint proposal with GSFC will benefit the NASA community in the areas of Codes S, Y, and M.

**DELIVERABLES:**

1. Design of process evaluation test structures for fabrication by Honeywell and LL
2. Design of device/circuit test structures for fabrication by Honeywell and LL
3. Design of transistor reliability test structures for fabrication by Honeywell and LL
4. Test results of fabricated structures at appropriate temperatures down to -150°C
5. Evaluation of test results
6. Process qualification reports (2) [GSFC]
7. Interim and final report [JPL]

**PARTNERSHIPS:**

MIT/Lincoln Lab (Fabrication),  
Honeywell SSEC (Test Structures & Fabrication)  
JPL/CISM/SOAC (Process & Device Test Structures & Test),  
NIST/University of Maryland at College Park (Reliability Test Structures & Test),  
GSFC (Process Qualification Review)

Leveraging: Test samples will be acquired through collaboration with CISM. Most of the JPL test structures will be dual use: process and device characterization [CISM project] and SOI reliability [NEPP project].

**ENDORSEMENTS:**

Mars Exploration Program (Code S & M).....see letter by Frank Jordan/JPL  
New Millennium (Code S).....see letter by Chuck Minning/JPL  
X2000 (Code S).....see letter by Dwight Geer/JPL  
CISM/SOAC (Code S).....see letter by Brent Blaes/JPL

The following projects at GSFC were identified by A. Sharma to have interest in the proposed work with priority "important":

EO1, MAP, GLAS  
GOES  
DISCOVERY Missions

**SCHEDULE:**

Q1/00	Process, reliability and circuit test structure design of Honeywell chip [JPL]
Q2/00	Fabrication and characterization test of Honeywell chip [JPL]
Q3/00	Process, reliability and circuit test structure design of MIT/LL chip[JPL]
Q4/00	Fabrication and characterization test of MIT/LL, Interim Report [JPL] Process Qualification Interim Report [GSFC]
Q1/01	Set-up of low-temperature and reliability tests [JPL]
Q2/01	Low-temperature and reliability tests [JPL] Process Qualification Final Report [GSFC]
Q3/01	Final Data Analysis [JPL]
Q4/01	Final Report [JPL]