NASA Electronic Parts and Packaging Program

EEE LINKS

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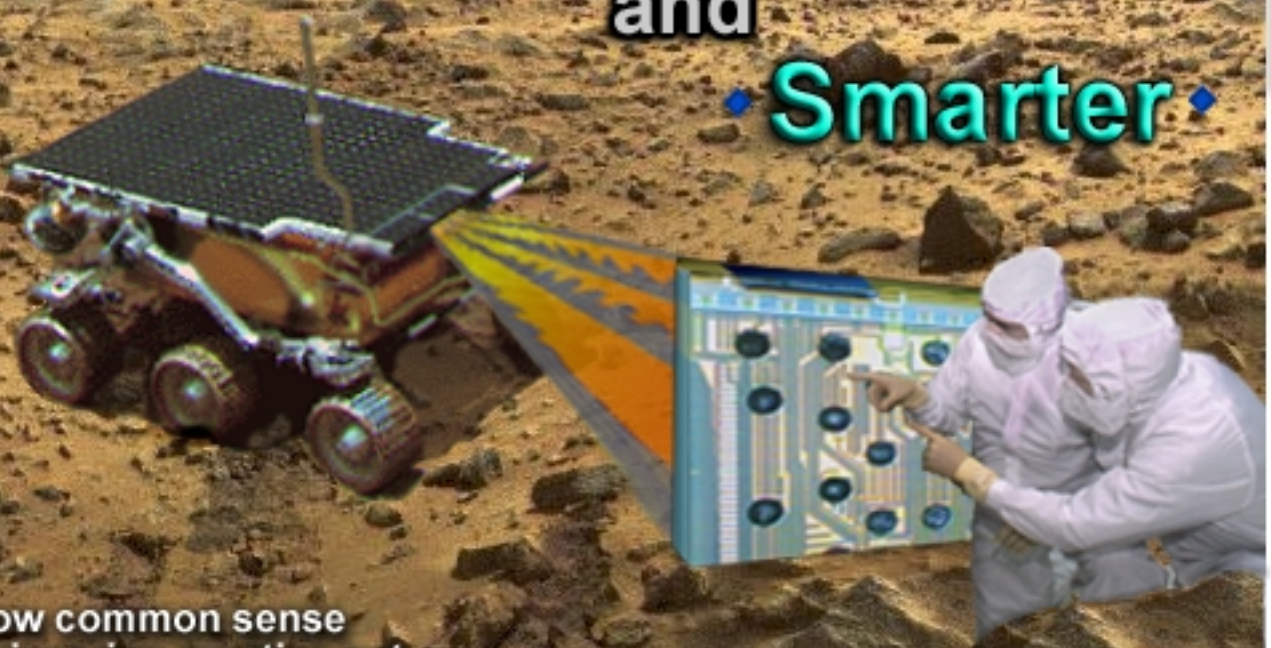
Faster • Better • Cheaper • and • Smarter •



"We cannot throw common sense and sound engineering practice out the window. We cannot blame poor planning on faster, better, cheaper."
Brian Keegan

Up Close with Brian Keegan
NASA's Chief Engineer

NASA Electronic Parts Assurance Group (NEPAG)
David Peters, Jet Propulsion Laboratory

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Accelerated Thermal and Mechanical Testing of CSP Assemblies
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Technology Validation of Optical Fiber Cables for Space Flight Environments
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Advanced Adhesion and Bonding
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Acoustic Microscopy, a Tool for Evaluating Quality of Microelectronics
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Preliminary Reliability Evaluation of Copper-Interconnect Metallization Technology
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Letter from the Editors

Welcome to the January 2001 issue of EEE Links.

The EEE Links Newsletter is a great way to share practical experiences and discoveries with your colleagues.

The NASA Electronic Parts and Packaging (NEPP) Program says goodbye to Mr. Tom Gindorf and best of luck in his retirement. We welcome Mr. Chuck Barnes, JPL, as the new NEPP Program Manager. Mr. Choon Lee, JPL, has been named the Electronic Parts (EPAR) Program Manager.

In our interview with Brian Keegan, NASA's Chief Engineer, he stressed the importance of the NEPP Program in performing technical assessments, characterizations, and evaluations of newly available and advanced (emerging) electronic parts and packaging, to enable their rapid infusion into NASA's hardware projects, thereby reducing the cost of mission success.

By doing this, the NEPP Program enables NASA's projects and missions to be "faster, better, cheaper". Please keep us informed with your questions and needs so we can continue to improve the upcoming issues to meet your needs.

You may also submit articles for upcoming issues anytime. Check out the focus for future EEE Links at http://nepp.nasa.gov/imd/eee_links.

To learn more about the NEPP Program visit our web site, http://nepp.nasa.gov.

The EEE Links Newsletter is published under the NASA Electronic Parts and Packaging (NEPP) Program. This is the first issue published by QSS Group, Inc., the new EEE Links Editor.

Thank you,

Shelly DiPaula and Sandy Aitken
Editors, EEE Links
QSS Group, Inc.

Up Close with Brian Keegan, NASA's Chief Engineer

EEE Links - The faster, better, cheaper philosophy has generated interest in greater use of COTS. How do you see NEPP playing a role in this?

Keegan - I think NEPP is a key aspect in enabling the infusion of technology. There has been a lot of effort in trying to grasp how we can better manage programs and projects in general. Driven by the Mars failure, there have been many evaluations of the faster, better, cheaper philosophy and how we apply it. I think one important message that came out of the evaluations was the heightened realization of our dependency on technology. We need to infuse technologies in our programs not only to improve performance but also to improve reliability and reduce weight, power, volume and related resource needs.

As far as technology products are concerned, EEE parts are associated with the lower levels of assembly, and are extremely important elements of technology products. It is important for us to understand that the Agency's engineers need to determine how to apply new EEE parts to meet their requirements. NEPP plays a key role in providing the Agency the performance and reliability that we seek as we infuse emerging technology into our programs.

NEPP provides an understanding that will improve our ability to use parts technology in applications that enhance performance and reliability. We talk a lot about faster, better, cheaper relying on the products of a separate technology program. I personally see NEPP as a key element of that.

EEE Links - Do you see the NASA community trying to leverage off other industries?

Keegan - Yes, I think there is a need to leverage off of like things. I think it is important to understand our needs. Then we can identify other customers of

the EEE Parts community that have similar needs and work with them. It is important to maintain close ties with others in the EEE parts community as a way of helping to get our needs met. This approach will minimize the cost burden that we incur while still meeting our goals.

EEE Links - What are your expectations of the NEPP engineers and scientists?

Keegan - I expect the NEPP engineers and scientists to continue to understand parts applications in order to reduce undue failures and rework and to increase performance, reliability and safety. The NEPP engineers and scientists are an important part of mission success by characterizing technology in emerging areas. This provides greater confidence that parts have been tried and the probability of failure reduced. It becomes more expensive if problems are not uncovered until later in the development cycle. An important part of cost and schedule success is to minimize failures during systems test.

Another expectation is that the NEPP engineers will communicate their results to the Agency's projects and missions teams. These findings become key elements in our risk management

processes. Risk management embraces the whole team. It has to be a project-wide/ team-wide activity. It is very important that the Agency continues to develop our people in the areas of risk management and effective communication.

EEE Links - Explain what you mean by development of people.

Keegan - People need technical skills to get their job done but they also need interpersonal skills. The Agency's management needs to be proactive in helping the individuals become aware of the need for such development and in helping them obtain it.

EEE Links - How can NEPP improve NASA's parts assurance?

Keegan - It is very important to keep NEPP focused on the future and the emerging technologies. We need to keep near-term and future separate. The primary thrust areas for future NASA missions are higher performance, lower weight, and reduced power dissipation. NEPP needs to intensify its effort in technology assessment and characterization for emerging technologies. This effort needs to be congruent with the Agency's technology roadmaps. Also, NEPP needs to clearly define paths for infusion of these advanced technologies in ways that produce reliable results.

I am worried that tying NEPP too closely to parts assurance will be limiting on NEPP's ability to focus on the future. Parts assurance and NEPP are not one and the same. NEPP needs to be viewed distinctly. NEPP's emphasis is on the future.

EEE Links - How do you see the relationship between the NASA EEE Parts Assurance Group (NEPAG) and NEPP?

Keegan - A continued dialog between NEPAG and NEPP is critical. A joint program is not appropriate. We need to devote appropriate funding levels to both programs. NEPAG serves the projects of today and can draw funding from today's projects. NEPP focuses on the projects of tomorrow.

EEE Links - How would you measure the success?

Keegan – By whether or not customers are using the NEPP products to help them meet their project goals in ways that are faster, better, and cheaper.

EEE Links - How do you keep the vision of faster, better, cheaper working through the Agency?

Keegan - Management must believe in it. Faster, better, cheaper does work if the fundamental tenets are applied. If you save money but increase failure then nothing is accomplished. We need to apply faster, better, cheaper as a 3-dimensional paradigm. The Agency's managers need to make well-informed decisions by believing in the faster, better, cheaper philosophy for their projects. We can move towards improving all three simultaneously. The secret lies in properly using technology to enhance the way we do things. Originality and aptness of thought must apply. We cannot throw common sense and sound engineering practice out the window. We cannot blame poor planning on faster, better, cheaper. We must be willing to use new methods and new products but not without some reasonable understanding of the risk we are accepting as we do so. NEPP is a fundamental building block for being prudent in the risk we take as we apply new technology in pursuing faster, better, cheaper.

Mr. Keegan participated with Dan Goldin, the NASA Administrator, in the NASA Integrated Action Team (NIAT) Web Cast. The web cast can be viewed at http://www.nasa.gov and select NIAT web cast.

Brian Keegan's Biography

Mr. W. Brian Keegan was named NASA Chief Engineer in February 2000. The Chief Engineer reports directly to the Administrator and is responsible for overall review of the technical readiness and execution of all NASA programs. The Chief Engineer also provides an integrated focus for Agency-wide engineering policies, standards and practices.

Since 1997, Mr. Keegan has been the Goddard Space Flight Center's Director of Applied Engineering and Technology. He was responsible for providing engineering support to a wide array of science instrument and spacecraft development projects.

In August 1994, Mr. Keegan was appointed the Deputy Director of Engineering. In this position, he directed a broad spectrum of activity, ranging from technology development to the design, development and test of components, instruments, subsystems, and spacecraft for various flight projects such as the Roentgen X-Ray Timing Explorer (XTE), the Tropical Rainfall Measurement Mission (TRMM), the Hubble Space Telescope (HST) Servicing Missions, and the Small Explorer (SMEX) series of Space Science missions. In April 1997, he was appointed the Acting Director of Engineering. In September 1986, he was selected as the Deputy Director of Flight Assurance at Goddard, providing direction and leadership in formulating and implementing policy for design reviews, environmental testing, reliability, quality, and flight systems safety in conjunction with the significant revamping of these activities that followed the Challenger accident. In recognition of his accomplishments, Mr. Keegan was awarded the NASA Outstanding Leadership Medal in May 1994. Mr. Keegan joined NASA's Goddard Space Flight Center in 1966 as a structural engineer involved with test program planning and the derivation of environmental test requirements. Mr. Keegan received his Bachelor of Science in Physics from Loyola College in Baltimore in 1962. Mr. Keegan currently resides in Ellicott City, Maryland, with Charlotte, his spouse of 37 years.

Coming Events

February 12 - 15, 2001
Commercialization of Military & Space Electronics Conference & Exhibition
http://www.cti-us.com, 256-536-1304

May 15 - 16, 2001
The Second Annual NEPP Conference
Electronic Parts, Packaging, and Radiation Characterization for Space Applications
http://nepp.nasa.gov/pubs/socal01/index.htm

October 22–25, 2001
Reliability, Testing, and Characterization MEMS (mfO2)
Part of SPIE's International Symposium on Micromachining and Microfabrication
membership@spie.org or call 360-676-3290; http://www.spie.org/info/mf/

NEPP and CALCE Working Together

Dr. Michael Osterman
University of Maryland, College Park, Maryland
http://www.calce.umd.edu

The National Aeronautics and Space Administration (NASA) Electronic Parts and Packaging (NEPP) Program and the Computer Aided Life Cycle Engineering (CALCE) Electronic Products and Systems Center partnership will provide research and development strategies and methodologies for selecting and evaluating electronic parts and packaging technologies on future NASA projects and missions.

Selected NASA engineers will be trained at CALCE on the use and application of CALCE tools and on strategies for improving the quality of parts selection and qualification processes and procedures.

The CALCE Center, based at the University of Maryland, was established in 1986 under a National Science Foundation (NSF) program and operates through industry sponsored research. The center and its original six industry sponsors formed the CALCE Consortium with a mission to create a knowledge and resource base for the development of competitive electronic components, products, and systems.

Today the CALCE Consortium consists of over forty companies and agencies from all over the world, and represents the full breadth of the electronics industry including automotive, avionics, consumer, semiconductor, telecommunications as well as government agencies.

The CALCE research program has also expanded and is committed to developing a comprehensive methodology for achieving quality and sustainability of electronic systems. This research effort is organized by three primary thrusts:

- Failure Identification and Reliability Modeling
- Environment and Operational Assessment of Products
- Risk-Informed Technology Insertion Methodologies

Current research efforts are focused on the use of lead-free solder, parts management, the effect of impact on portable electronics and simulation techniques to virtually qualify electronics.

With over 15 years of research, CALCE has compiled resources on such issues as the use of plastic parts in high reliability applications, durability of ball grid arrays (BGAs) and chip scale packages (CSPs) and guidelines for developing high temperature electronics.

In conducting research, CALCE has always emphasized the examination of the fundamental physical principles that cause failure, for which the group coined the phrase “physics of failure”. In striving to provide the best possible service to CALCE sponsors, the Center underwent the process of becoming ISO certified and received the Certificate of Registration for ISO 9001 in December of 1999.

The collaboration between NASA and CALCE will afford NASA engineers the opportunity to interact with CALCE and gain access to CALCE web resources.

The CALCE web site, www.calce.umd.edu, contains some of the world’s most advanced reliability assessment and virtual qualification software: calcePWA and CADMP II. It provides the guidelines for a silicon-to-system accelerated product qualification, and a wide collection of resources such as journal articles,

technical reports, web-based textbooks that cover areas of critical importance in electronic product and system development. Also guidelines for solder joint fatigue analysis, cost analysis and supply chain management are available through the web site.

The CALCE research and software is available to NASA GSFC engineers and contractors through the NEPP web site at http://nepp.nasa.gov. CALCE is in the process of forming additional partnerships with the other NASA centers. An online account request form is available at http://www.calce.umd.edu/account_request.html.

For more information on the program, contact Dr. Michael Osterman, osterman@calce.umd.edu, or Ashok Sharma, asharma@pop300.gsfc.nasa.gov

NASA EEE Parts Assurance Group (NEPAG)

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An Agency level organization has been formed by NASA/HQ Code Q/AE to support the Centers by providing sound EEE Parts Assurance guidance in today's world of supplier mergers, acquisitions, COTS, and FBC.

The considerable expertise of three Governmental Agencies, NASA, USAF/SMC, and the USN/NSWC, seven NASA Centers, ARC, GRC, GSFC, JSC, KSC, LaRC, MSFC, NASA Headquarters, JPL, and an International Partner, European Space Agency, are combining experiences on space flight EEE Parts.

Our Charter is to exchange EEE Parts information of mutual interest on the subjects of quality, reliability, availability, and technology used in space flight. We will also, through consensus, control the necessary industry specifications, coordinate Military Specifications, create tools for estimating microelectronic part risk, mitigate vendor issues, resolve on-going problems, and support DLA audits to assure reliable hardware.

Please feel free to visit our web site, http://eee.larc.nasa.gov/forum.

Don't be surprised when you hear our name: NASA EEE Parts Assurance Group (NEPAG).

PACKAGING

Accelerated Thermal and Mechanical Testing of CSP Assemblies

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Abstract

Chip Scale Packages (CSP) are now widely used for many electronic applications including portable and telecommunication products. The CSP definition has evolved as the technology has matured and refers to those packages with a pitch of 0.8 mm and lower. Packages with fine pitches, especially those with less than 0.8 mm, and high I/Os may require the use of a microvia printed wiring board (PWB) which is costly and they may perform poorly when they are assembled onto boards. A test vehicle (TV-1) with eleven package types and pitches was built and tested by the JPL Microtype BGA Consortium during 1997 to 1999. Lessons learned by the team were published as a guideline document for industry use[1].

The finer pitch CSP packages, which recently became available, were included in the next test vehicle of the JPL CSP Consortium [2]. The Consortium team jointly concentrated their efforts on building the second test vehicle (TV-2) with fifteen (15) packages of low to high I/O counts (48 to 784) and pitches of 0.5 mm to 1.27 mm. In addition to the TV-2 test vehicle, other test vehicles were designed and built by individual team members to meet their needs. At least one common package was included as control in each of these test vehicles in order to be able to compare the environmental test results and understand the effects of PWB build and manufacturing variables.

One test vehicle was designed and assembled by Hughes Network Systems using their internal resources and is identified as TV-H. This paper presents the most recent thermal cycling test results to 900 cycles which are currently being performed under -55 to 125°C conditions for packages with various die sizes. Mechanical fatigue test results for the 280 I/O count packages under various deflections with and without local heating are also presented.

CSP Test Matrix

Test Vehicle Package I/O /PWB

The TV-H had eight packages ranging from 48 to 280 I/Os with pitches of 0.8 mm as shown in Figure 1. The PWB had four layers with the two resin coated copper (RCC) layers and an FR-4 core (1+2+1) having a total thickness of 0.43 mm. Microvia technology was used. The pad had a 0.1-mm (4-mil) microvia hole at the center of pad. A non-solder-mask-design (NSMD) pad with a diameter of 0.3 mm and 0.05-mm clearance was used. The surface finish of the PWB was Ni/Au immersion with about 2-8 micro inch of gold over 100-200 micro inch Ni. No clean solder paste for assembly was applied with a 5-mm thickness laser cut stencil. The test vehicle was 11.9 cm by 4.6 cm (4.75″ by 1.85″) with one connector attached for continuous thermal cycling monitoring. The width of test vehicle was cut into 1” for the three point bend fatigue testing.

280 I/O Package/Test Vehicle Features

Figure 1 shows a full populated test vehicle (TV-H) with two sites for the 280 I/O fine pitch ball grid array (U4 and U2 sites). All packages were daisy-chained, and they were divided into several internal chain patterns. The daisy chain pattern on the PWB completes the chain loop into the package through solder joints. Several probing pads connected

to daisy chain loops were added for failure site diagnostic testing. The package and PWB daisy chains for the 280 I/O package is shown in Figure 2. All locations including U4 and U2 sites were populated for the thermal cycling assembly testing. Only the U4 location was populated for mechanical cycling testing. All packages were pre-baked at 125°C for 2 ½ hours prior to assembly.

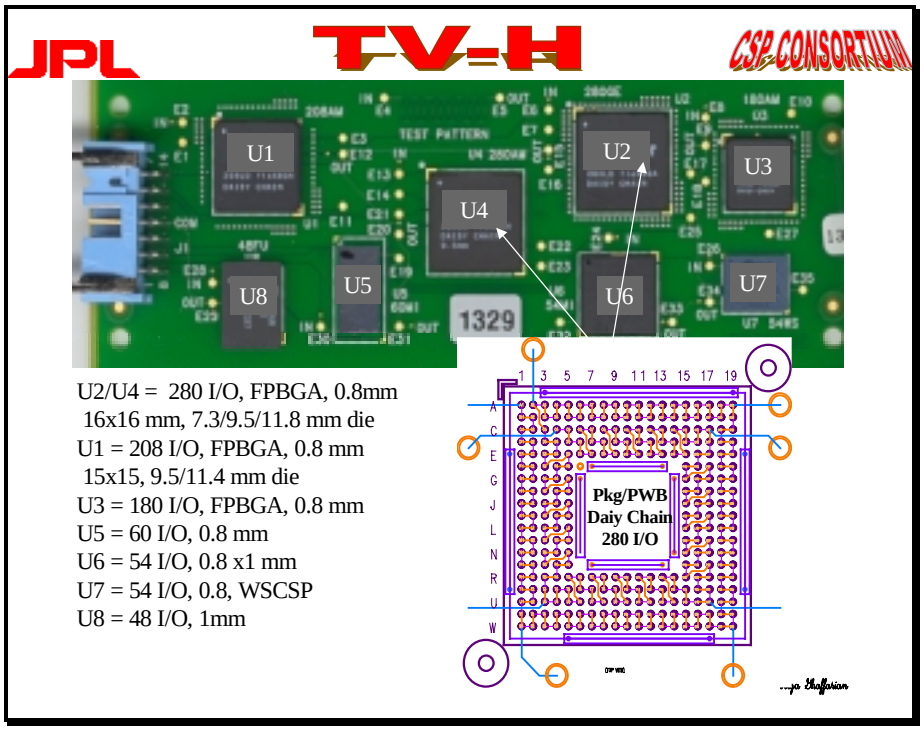

Figure 1 - The assembled TV-H with numerous CSP and Fine pitch BGA packages. The package/PWB daisy chain for the 280 I/O FPBGA is shown on the bottom right.

Test Conditions

Thermal Cycling Test

Thermal cycling was performed in the range of –55°C to 125°C. The heating and cooling rates were 2° to 5°C/min with a dwell at maximum temperature of more than 10 minutes and a shorter dwell time duration at the minimum temperature. Each cycle lasted 159 minutes. The test vehicles were monitored continuously during the thermal cycles for electrical interruptions and opens.

Mechanical Cycling Test

Mechanical cycling test was performed using a three point bending test set up as shown schematically in Figure 1. This test vehicle coupon had one package at its center. The center of the package along the PWB was set on a stationary ram with 3.13-mm (1/8″) radius. The coupon was in contact along its edges with two moving bars, spaced at 80 mm apart each having a 3.13-mm (1/8″) radius. These two bars pushed the coupons down onto the stationary ram with specified maximum deflections for mechanical cycling. To determine the maximum deflection of assembly under static condition, a test coupon was tested to failure by continuously increasing deflection. Failure was automatically detected by application of current to the daisy chain with 3.2-ohm resistance to achieve a four (4) volt output. Monitoring was accomplished by interfacing a PC into the output signal

from the mechanical testing system and recording data. When the daisy chain become open, the output voltage from the system increased to 4.16 volts. Voltage output and deflection levels were continuously recorded in a database for retrieval and data analysis.

The first three test results were inconsistent and they failed unexpectedly at very low values. Two observations were made: (1) the test coupon was slightly moved during cycling form its zero deflection state, and (2) the application of high current into the daisy chain introduced heat into the package. The first observation was corrected by using a double-sided tape to secure the coupon to the bars in order to minimize the movement of the coupon. The second observation was corrected by using current as variable. A set of test coupons were tested under current condition thereby further accelerating cycles-to-failure relative to a no-current condition. To know the effects of current on package temperature, the package surface temperature was monitored by thermocouple before the start and during mechanical cycling. The temperature rises were in the range of 95°C-105°C. When no current was applied, the daisy chain resistance was monitored using a multimeter. The first increase in resistance (considered initiation of failure) was reported. Test was continued until complete daisy chain open condition and this value was also recorded.

Test Results

Thermal Cycling Results

Only a limited number of test vehicles were subjected to accelerated thermal cycling condition (-55 to 125°C). The most recent thermal cycle test results to 500 cycles for these are presented in a recent publication [2]. Cycles-to-failure (CTF) for other packages and under other thermal conditions are being gathered and will be analyzed and presented in the future. Figure 4 shows cycles to first failures for the 280 I/O FPBGA with 3 die sizes. The 280 I/O package with an 11.8-mm die in 16 mm packages failed in the range of 303 to 824 cycles. For packages with 9.5-mm die, only two out of the 10 assemblies failed at 690 and 836 cycles when they are subjected to a total of 900 thermal cycles.

Mechanical Cycling Results

Twenty test coupons were used for accelerated mechanical cycling testing under deflection levels from 0.125 mm to 1.875 mm (0.005” to 0.075”). The maximum cycling deflection value represents approximately 30% of maximum deflection under static test. MCTF for assemblies with various die sizes for single and combination of two to three deflection levels to 300,000 cycles are listed in Table 1.

Table 1 - Static and mechanical cycles-to-failure for the 280 I/O fine pitch BGA with three die sizes under various cycling conditions

ID	Voltage (Ohm)	Die Size (mm)	0.025" (0.625 mm) Deflection	0.050" (0.125 mm) Deflection	0.075" (1.875 mm) Deflection	Comments
1A	N/A	11.8	N/A	N/A	N/A	Static, max. deflection 5.65 mm (0.226")
3C	N/A	9.5	300,000	86,887	N/A	Low deflection, high cycles
3A	N/A	11.8	N/A	10.000	6,470	6,470-7,691 cycles
4B	N/A	9.5	10,000	10.000	6,384	6,384-8,595 cycles
5B	N/A	7.3	N/A	10,000	8,450	8,450-10,204 cycles
2C	N/A	11.8	N/A	10,000	900	900-1,490 cycles, Age at 150°C, 20 min.
2D	N/A	11.8	N/A	10,000	2,984	2,984-3,109, Age at 150°C, 20 min.
3B	4 (3.2)	11.8	104,361	N/A	N/A	One deflection only
1D	4 (3.2)	11.8	10,000	2,764	N/A	2,764-2,764 cycles
4A	4 (3.2)	9.5	10,000	1,460	N/A	1,460-1,865 cycles, 10,000 @ .005"
5A	4 (3.3)	7.3	10,000	2,846	N/A	2,846-3,175 cycles

Conditions listed are failure under static deflection and failure under mechanical cycling with and without application of 4 volts to the package/PWB daisy (chain resistance 3.2 Ohms). The load deflection under static condition was determined and found to have a linear relationship, i.e. as load increased the deflection increased. The maximum deflection prior to failure was 5.65 mm (0.226") under 4-volt condition. This value is expected to be higher if no current is applied to the daisy chain during testing.

To achieve accelerated failure to less than a day under 5 Hz cycling frequency (10,000 cycles for every 33 minutes), damage levels were accumulated under increasing level of deflection. Deflection levels were increased when assemblies survived 10,000 cycles under one level of deflection. Further acceleration was achieved by application of current to the daisy chain resistance of package/PWB. Data presented in Table 1 clearly indicates that assemblies failed under maximum combined deflection of 1.25 mm (0.050") for a 4-volt condition. The maximum deflection increased to 1.875 mm (0.075") when no current was applied. If no damage accumulation technique is used then assemblies under deflection of 0.625 mm (0.025") with and without current failed at 104,000 and more than 400,000 cycles (300,000 cycles plus 87,000 at 0.050"), respectively. Note the MCTF reduction when assemblies were subjected to 150°C for only 20 minutes. This temperature and time represent cure of a reworkable underfill.

Failure Mechanisms

Assemblies are currently being subjected to scanning electron microscopy, cross sectioning, and pull test to determine failure mechanisms due to various accelerated mechanical cycling schemes. However, several observations were made during mechanical cycling when assemblies started to show signs of failure. One aspect was included in Table 1 by listing the MCTF range from the start of daisy chain voltage/resistance increase to complete daisy chain open. In general, increase in resistance or voltage was

slow and sometimes it required thousands of additional cycles before a complete daisy chain open occurred under loading (deflection). Failure under load was not permanent for most cases, especially for no voltage condition. Daisy chains showed increase in resistance after removal of load, but did not show a complete open. Under current application conditions, sometimes complete failure occurred under both load and no load conditions.

Discussion

New applications of advanced electronic packaging, including chip scale package in consumer portable products, brought about new environmental requirements not seen in their previous generation of relatively benign office applications. The on/off cycles introduce failure of solder joints due to thermal mismatch of package and PWB. Solder joint integrity is critical since the joints carry both mechanical and electrical load. Failure of solder joints due to CTE mismatch is commonly characterized using a dummy package daisy chained through solder joints and the PWB by monitoring their failure under temperature cycling. Use of power cycling, i.e. heating solder locally by imbedding resistance inside of the package, is now being considered as an alternative since it provides higher reliability results much needed for miniature packages.

In addition to on/off cycles, electronics in portable products are also required to be robust under mechanical conditions, e.g. robustness to repeated mechanical cycling due to key punching and to shock due to dropping or bending due to sitting on product. The mechanical requirements are not new for high reliability application environments including automotive, military, and aerospace. Conventional leaded SMT packages have been shown to be robust. Unfortunately, both the use of rigid balls instead of flexible lead and reduction of the interconnect area for most CSPs due to reduction in package size have negative effects on their environmental robustness. Accelerated thermal and mechanical testing are required to screen for different designs and also to determine robustness of CSPs in order to meet the increasing demand for time to market shrinkage for consumer products and effective use of these products for high reliability applications.

Mechanical cycling tests, if they provide the same trends as thermal cycling, could be a very effective acceleration technique. The investigation performed here was aimed at characterizing behavior of CSPs under mechanical cycling conditions. Also to determine if techniques can be developed to determine trends that are being established under thermal cycling conditions. One key parameter that affects thermal cycles to failure is the die size in a CSP. Thermal cycling of packages with various die sizes clearly indicated the criticality of die size and its effects on solder joint reliability. With limited tests performed, it appears that there is a possibility that such a trend can be established by mechanical cycling.

Mechanical tests with no local package heating will significantly overestimate the life of solder joints. Local heating will accelerate life testing and provide a better application representative. Very promising accelerated test results under mechanical cycling were found for those assemblies exposed to isothermal aging at 150°C for 20 minutes. These assemblies clearly showed much lower mechanical cycles to failure and the trend was apparent. Further work is required to determine if this accelerated technique could be used to screen for a variety of manufacturing defects and possibly, in conjunction with limited thermal testing, to project life for intended applications.

Conclusions

These conclusions are based on results limited to assembly failure to 900 thermal cycles in the range of -55°C to

125°C and a limited number of mechanical cycling tests to failure.

Cycles-to-failures for the fine pitch ball grid array (FPBGA) with 0.8-mm pitch were in the range of 300 to 800 cycles. These are significantly lower than their BGA counterparts with 1.27 mm which they failed higher than 1,000 cycles[3].

The FPBGA failed at 5.7-mm maximum deflection under static bending load. It survived more than 400,000 mechanical cycles to maximum deflection of 0.625 mm (0.025"). This value decreased to about 100,000 cycles when packages were locally heated.

The trend on the effects of die size, when sizes were far apart, could be possibly detected by the use of accelerated mechanical cycling and local heating of the package possibly due to heating and rigidity differences in loading. Accelerated mechanical testing detected the degradation effect of assemblies subjected to isothermal aging at 150°C for 20 minutes. Thus, such tests may be effective in screening for manufacturing defects, severe degradation due to environmental exposure, and mechanical robustness for application.

Acknowledgements

The portion of research described in this publication is being carried out by the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

The JPL author would like to acknowledge the in-kind contributions and cooperative efforts of the JPL CSP Consortium. Special thanks to A. Arreola, T. Hills, JPL; M., Lam, D., Strudler, S., Umdekar, Hughes Network Systems (HNS), and package suppliers and other team members who have made contributions to the progress of this program.

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3. Ghaffarian, R., "*Ball Grid Array Guidelines*" distributed by Interconnection Technology Research Institute, http://www.ITIR.org, (512) 833-9930

NEPP Web Site Overhaul

The NEPP web site, http://nepp.nasa.gov, is getting a makeover. If you have any suggestions or comments please forward them to Sandy Aitken, saitken@qssmeds.com. We are in the process of talking with users to make sure that the site is useful and provides the information needed to perform their jobs.

Technology Validation of Optical Fiber Cables for Space Flight Environments

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The following article contains excerpts from a paper that was published and presented at the International Society of Optical Engineers Photonics East conference Optical Devices for Fiber Communication II, November 8, 2000, in Boston, MA. Melaine Ott and Patricia Friedberg (NASA Goddard Code 562) performed this work. The entire paper is available through SPIE proceedings Vol. 4216 or at the web site location:

http://misspiggy.gsfc.nasa.gov/tva/authored/fo_photonics.htm

Abstract

Periodically, commercially available (Commercial off the Shelf, COTS) optical fiber cable assemblies are characterized for space flight usage under the NASA Electronic Parts and Packaging Program (NEPP). The purpose of this is to provide a family of optical fiber cable options to a variety of different harsh environments typical to space flight missions. The optical fiber cables under test are evaluated to bring out known failure mechanisms that are expected to occur during a typical mission. The tests used to characterize COTS cables include: vacuum exposure, thermal cycling and radiation exposure. Presented here are the results of the testing conducted at NASA Goddard Space Flight Center on COTS optical fiber cables over this past year. Several optical fiber cables were characterized for their thermal stability both during and after thermal cycling. The results show how much preconditioning is necessary for a variety of available cables to remain thermally stable in a space flight environment. Several optical fibers of dimensions 100/140/172 microns were characterized for their radiation effects at -125°C using the dose rate requirements of International Space Station. One optical fiber cable in particular was tested for outgassing to verify whether an acrylate coated fiber could be used in a space flight optical cable configuration.

Introduction

This is the fifth paper in a series of publications on the subject of characterization of commercial optical fiber and optical cables for space flight. The objective of these publications is to provide information on the correct environmental usage of commercial cables for space flight through characterization testing to typical space flight environmental parameters. Several tests are used as a technology validation method to determine if an optical cable is suitable for a typical space flight environment. Included in this validation testing are outgassing testing, thermal testing and radiation testing. Vibration testing is also used as a technology validation test but data from this type of testing is not included in this paper.

In most cases, all materials used on space flight hardware are evaluated for outgassing characteristics in a vacuum environment to ASTM 595 (% Total Mass Loss, %TML must be less than 1%).5 If a material passes the ASTM 595 test then the material is considered acceptable for usage in a vacuum environment. A comprehensive database is available via a NASA GSFC web site. In some cases when a material is known to outgas in a vacuum environment, the potential for usage still exists if the outgassing occurs in an area of the unmanned portion of a space craft such that these materials could not degrade the performance of any existing systems. Acrylate coatings used as protection on

optical fiber are well known as "outgassers" and therefore are usually prohibited from space flight missions. However, acrylate coating used inside of a cable configuration was evaluated by Lockheed Martin to verify whether the acrylate coating added to the collected materials or mass loss. The testing showed that this configuration was acceptable by ASTM-595. The result of this testing was never verified at GSFC until now.

Thermal stability of optical cables is examined in two ways. The first is to examine the optical stability of fiber optic cable configuration given a changing thermal environment or during thermal cycling. The second is to examine the total amount of cable component shrinkage after exposure to a changing thermal environment or after thermal cycling. Both tests are used to determine if a cable is suitable for space flight. Presented here are results from testing using a generic thermal environment of -55°C to +125°C.

Lastly, of the subjects presented here, total ionizing dose radiation testing is used as a technology validation method of determining which fiber cable is suitable for space flight environment usage. The data presented is from testing using the International Space Station environment at two different dose rate exposures while at a temperature of -121°C. In most cases, low temperature during radiation exposure, represents the worst case for radiation induced attenuation for cable configurations containing typical germanium doped 100/140 micron optical fiber. At colder temperatures optical fiber is less likely to anneal and recover from the color centers generated as a result of radiation exposure. The test results from cold temperature radiation exposure of three optical fibers are discussed here.

Conclusion

Examined here were several optical fiber cables and optical fiber for their suitability in typical space flight environments. The W.L. Gore FON1008 cable was tested with acrylate fiber inside for its suitability in a thermal vacuum environment. The W.L. Gore FON1004, the Brand Rex OC1614 and OC1008 and the Northern Lights H06 and HL1 made for RIFOCS were examined for thermal stability for the parameters of length shrinkage and optical stability. Lastly three 100/140/172 polyimide, carbon coated optical fibers made by Lucent SFT were tested for their suitability of use in the ISS space radiation environment at -125 °C.

Advanced Adhesion and Bonding

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Introduction

The following article provides an overview of JPL Publications D-17926: Advanced Adhesion & Bonding.

Executive Summary

Structural integrity of an adhesive bond that holds together two dissimilar materials is determined by a discouragingly large set of factors. The primary objective of this work is to provide an engineer practicing in the field of aerospace/aircraft industry with a concise overview of the basic principles, design recommendations and other characteristic parameters needed for a complete description of the quality of the adhesive bond. This review incorporates essential elements of Chemistry, Physics, Mechanics, Mathematics and technological requirements that are pertinent to the subject matter.

One may then describe the collection of four chapters that follow as a compendium that summarizes our state-of-the-art know-how relating to the chemical, thermal, mechanical properties as well as the strength and range of applications (and their limitations) of the commercially available adhesives. Also certain design procedures are discussed and shown how they can be used to plan for manufacturing of a new product with pre-determined properties.

The report consists of four chapters, but the substance of the entire text may be readily divided into two major groups: fundamental and applied. Chapter 1 belongs in its entirety to the first group. This chapter summarizes our present knowledge and provides an information of fundamental nature about the intermolecular forces and about the reversible (elastic) and irreversible (viscous and plastic flow type) deformation processes, which precede the final act of bond fracture.

To understand the nature of state of stress induced in the immediate vicinity of fracture front and that existing within the bulk of deformable bodies participating in transmission of loads through the bonded contact area, it is necessary to consider five sub-elements, all of which take part in the global deformation and fracture processes. These sub-components are:

1. Adherend No. 1,
2. Interface between the adhesive and adherend No. 1,
3. Adhesive layer,
4. Interface between the adhesive and adherend No. 2,
5. Adherend No. 2.

If fracture propagates along one of the interfaces, it is referred to as the **adhesive fracture** characterized by the specific energy of adhesion, G_a. If, on the other hand, the chemical bond within the interfaces is stronger than the molecular attraction of either one of the adherends, then the cohesive fracture propagates through one of the joined elastic substrates, and it is characterized by the **cohesive fracture energy**, G_c. Since almost every adhesive is a composite material, and at the same time we have to deal with interfaces and adherends, which frequently possess dissimilar elastic moduli, it becomes apparent that the complexity of required

mathematical modeling requires a profound knowledge of the pertinent principles of Materials Science, Chemistry and Physics. Chapter 1 explains some of the first principles involved in the Mechanics of bond performance (such as the concept of energy balance at the onset of fracture, for instance), while certain rules of Thermodynamics of the bonding process are discussed in Chapter 4. Both chapters provide a useful insight into the complex phenomena of the bonding process. A reader who wishes to gain a somewhat deeper understanding of "how" and "why" things work as they do, will find reading of these two chapters useful.

Those interested in the technological aspects of adhesion will find a wealth of information in Chapter 2 and Chapter 3. Let us briefly mention the important topics belonging to this category such as adhesives used in Micro-Electro-Mechanical (MEMS) devices, package sealing and encapsulation, hermetic packaging, sealing by soldering, brazing, welding, laser welding and other methods used in aerospace and aircraft industries. Quality assurance and product evaluation techniques are discussed in the context of their appropriate applications. Special attention is paid to the non-destructive methods of evaluations, including X-ray radiography, acoustic microscopy and particle impact noise detection. Modes of failure are discussed along with a brief description of fatigue failure and time-dependent fracture caused by chemically aggressive environments, often referred to as "stress corrosion", a process which accounts for the synergistic effects of stress and chemical weakening of the intermolecular bond.

Finally, the response of adhesives subjected to extreme temperatures, either low or high, is reviewed in the context of space applications.

Chapter 3 is devoted to the thin film technologies, including growth and deposition of the film particles by thermal evaporation, resistive heating, electron-beam method, RF induction technique and sputtering. An important method of deposition of poly-silicon structural material is also discussed, and a mention of stiction and supercritical cleaning is made. These latter techniques are essential for the space applications promoted by NASA.

Chapter 4 reviews the approaches used in the selection of specific types of adhesives for a designated application. First, it emphasizes the advantages of adhesive bonding over other technologies intended for joining two materials. Then, it describes the various kinds of adhesives available for the job. Matching an adhesive to an adherend is discussed in the context of their chemical compatibility. Two characteristic entities are defined, critical surface energy and solubility parameter; and then shown how they can be used to define the proper selection of an adhesive for a given adherend, or vice versa. Guidelines are provided for designing a compatible pair of adhesive/adherend. A number of criteria to determine quantitatively the quality of the bond are described. In this class you will find such determining parameters as threshold strength, pressure sensitivity, rate and temperature effects, autohesion, interdiffusion and influence of molecular weight on the bond quality.

B A list of relatively simple testing procedures intended to determine specific energy of adhesion is carefully composed. Each technique is illustrated by an example, and the essential equations that relate the applied load to the characteristic energy of adhesion, G_a, are provided. This list incorporates the test configurations such as tensile detachment, contoured double-cantilever beam designed for steady-state fracture investigation, peel resistance test, pull-off test and the so-called "blister" (or bubble) test. Each of these techniques offers its unique advantages; some are suitable for soft adhesives with high degree of

compliance, and others serve well to examine the mechanical response of the structural adhesives.

Interestingly, the Griffith concept of the energy criterion for fracture is used throughout most of the sections in Chapter 4, thus providing a conceptual continuity and demonstrating the usefulness of the theoretical foundation laid down in some detail in the introductory chapter, Chapter 1. Some references to Nonlinear Fracture Mechanics are also made, but these fall beyond the scope of this compendium intended for engineers rather than advanced research personnel.

Support: NASA NEPP RTOP through Advanced Technology Program Office (JPL).

Acoustic Microscopy, a Tool for Evaluating Quality of Microelectronics

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JPL Quality Assurance has acquired a Sonix™ SAM (Scanning Acoustic Microscope) and is applying it to the NDE (Non Destructive Evaluation) of microelectronics, both components and encapsulated assemblies. The acoustic microscope is often used in conjunction with a x-ray microscope located in the same facility. The two provide information that is complimentary.

The SAM functions by sending pulses of extremely high frequency sound waves (10-210 megahertz) into a sample that is submerged in a fluid. Where discontinuities exist in the sample, the sound is reflected back to the transducer which functions both as the sound source and the detector. Reflections at a point are referred to as an A-scan. They are displayed as an oscilloscope trace as shown in Figure 1.

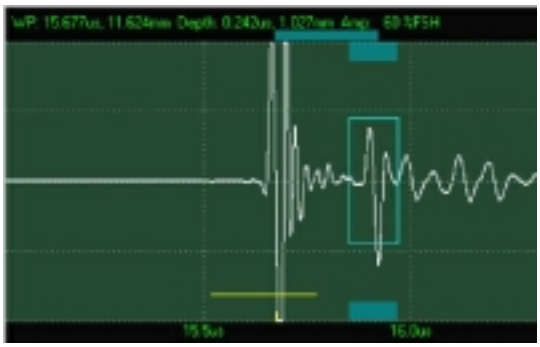

Figure 1 - A Scan

A line of these reflections taken across a sample results in a cross sectional display where large reflection intensity produces a lighter shading and weak reflections result in dark areas. Layers in the sample are clearly displayed in Figure 2.

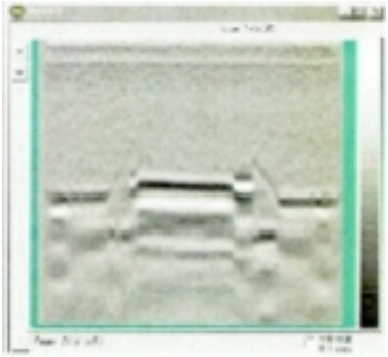

Figure 2 - B Scan

The data from multiple lines of reflections when taken together produces a planar view of the interior of a sample. Figures 3, 4 and 5 show the top surface and two interior layers of a Ball grid array package. These three pictures were produced in a single scan using a technique known as TAMI (tomagraphic acoustic microscopy inspection).

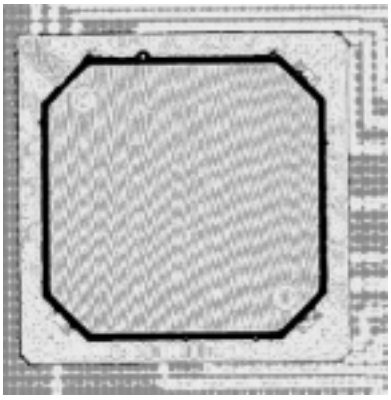

Figure 3 - Top Surface BGA.

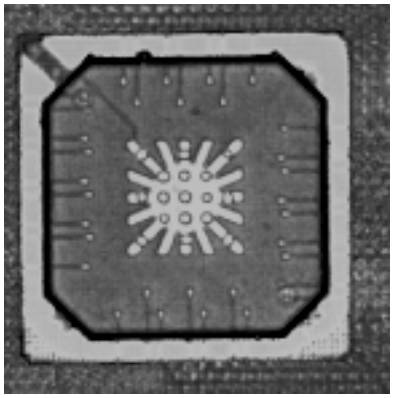

Figure 4 - Inner Layer BGA.

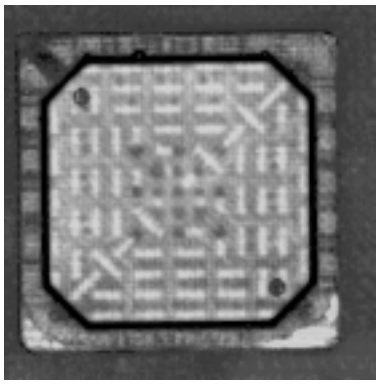

Figure 5 - Second Inner Layer BGA.

Acoustic microscopy displays delaminations as light areas against a darker background. Interpretation of areas lying below delaminations must be carefully undertaken, as most of the acoustic energy will be reflected back by the delamination so that the underlying area will appear unnaturally dark. In general, upper layers have the effect of casting a sonic shadow onto patterns contained in deeper layers.

In addition to delaminations many other defects can be revealed using SAM. These include die tilt; voids in underfill and die attach material and cracks in dies and substrates.

An example of using the acoustic microscope in conjunction with the x-ray microscope is shown in Figures 8 and 9. Both figure 8 (the x-ray image) and figure 9 (the acoustic image) show two wafers of silicon which were to be bonded together by reflowing indium squares that were deposited on facing surfaces of the wafers. The x-ray image clearly shows that the indium has not remained in place but has melted and agglomerated. The amount of actual bonding of the two wafers is somewhat in doubt. The acoustic image of the same area shows that most of the bonding occurs in the upper right quadrant which appears almost uniformly dark as a result of the acoustic energy passing freely through the indium bond.

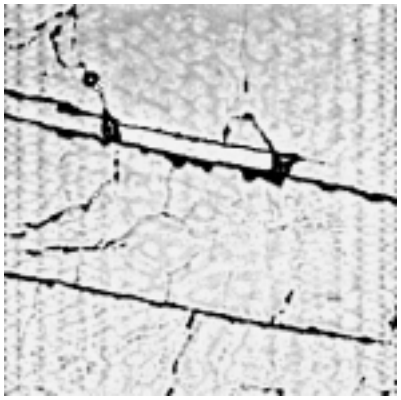

Figure 6. Rock Surface

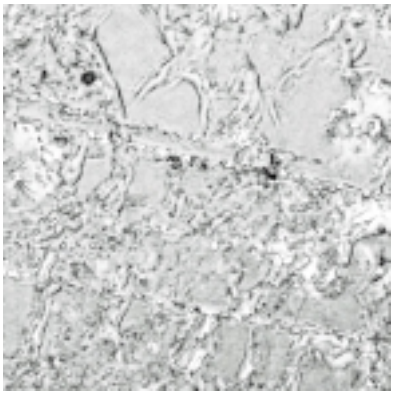

Figure 7. Rock Inner Structure.

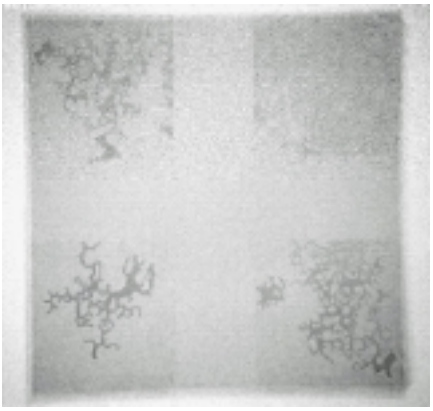

Figure 8. In bonded Si X-ray.

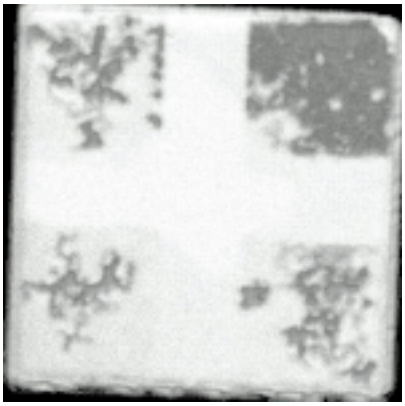

Figure 9. In bonded Si Acoustic

PARTS

Hot-Carrier Reliability of Transistors Fabricated by a 0.25-µm Fully-Depleted SOI CMOS Process

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Abstract

Fully Depleted (FD) Silicon-On-Insulator (SOI) transistors are particularly susceptible to hot carrier effects because the thin silicon body has two closely spaced, interacting oxide interfaces. In the present work, the hot-carrier degradation of transistors fabricated by a 0.25-µm FD SOI CMOS process was investigated. The degradation of key transistor parameters under drain voltage stress and worst-case gate bias was observed as a function of time. The shift of the front and back threshold voltages was analyzed with different back biases in order to separate front and back (buried) oxide degradation. A lifetime defined by a front threshold voltage shift equal to one sigma of the original distribution was extracted as function of the drain voltage. Whereas the first batch of transistors showed a large sigma but a reasonable lifetime at 2 Volt, the other had a reasonable sigma but a lifetime of only 1-day at that voltage. Even when comparing equal absolute degradation, the lifetime of the second batch was much inferior. It is shown that in the second case the short lifetime is caused by poor properties of the buried oxide (here created by a SIMOX process). Therefore, SOI wafers must be characterized for their hot-carrier susceptibility.

The paper was presented at the 2000 IEEE Microelectronics Reliability Qualification Workshop in Glendale, CA on October 31, 2000. Proceedings were distributed at the meeting. The work is being continued including low-temperature tests under the NASA Electronic Parts & Packaging Program (NEPP).

In Upcoming Issues

EEE Links is a quarterly publication with the following publication dates and focus

- April 2001 - Space Station
- July 2001 - Deep Space, Extreme Environments
- October 2001 - System on Chip Technologies

The EEE Links Newsletter is a great way to share practical experiences and discoveries with your colleagues. To submit an article go to http://nepp.nasa.gov/imd/eee_links/article_submission.htm for the guidelines and checklists.

Let your peers know what you are doing. Submit your work to saitken@qssmeds.com.

EOS Simulation and Failure Analysis of Metallurgically Bonded Silicon Diodes.

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Metallurgically bonded double plug non-cavity silicon diodes encapsulated in glass (type DO-35) are widely used in military and aerospace applications. In spite of a relatively simple design, these diodes have a large proportion of failures during destructive physical analysis (DPA) compared to microcircuits. Analysis of DPA jobs performed at the GSFC Parts Analysis Laboratory in 1999 shows a failure rate of 15% for diode jobs, compared to 11.5% for microcircuits. Similar results were reported by T. Devaney at Hi-Rel Laboratories, where the DPA failure rate for diodes was 44% compared to 33.1% for microcircuits. In typical military and aerospace applications, diode failures occur approximately three times more often (relative to the population of the system) than microcircuit failures. In many cases, failure is due to electrical overstress and the failure analyst is challenged to find the damage site and determine the conditions causing the failure.

Extensive analysis has been performed on secondary breakdown in diodes and transistors and the physical mechanism of this phenomenon is well-understood. Heat flow analysis is widely used to estimate failure conditions for devices damaged during EOS/ESD events. However, in most diode failures described in technical literature, failure analysis was not performed, and the relationship between overstress conditions and the location and appearance of damage has not been adequately investigated.

In this study, short pulses of forward and reverse current were applied to typical power rectifier 1N5811 diodes in order to simulate overstress conditions. Forward current pulses varied from 0.1 to 3 ms with current amplitudes varying from 200 to 1000 A were applied to one group of diodes. Reverse bias current pulses in the microsecond range with amplitudes from 2 to 400 mA (above breakdown voltage) were applied to another group. A small-step cross sectioning in combination with electrical probing, light emission microscopy, liquid crystal technique, and chemical staining were used to reveal and compare damage in three groups of diodes: two overstressed groups and the third group which had failed during burn-in electrical testing.

Failure mechanisms and peculiarities of damage created in these diodes and several case histories related to different types of diodes are discussed.

Analysis showed the following:

1. Small-step cross-sectioning technique in combination with electrical probing, light emission microscopy, liquid crystal technique, and chemical staining was successfully used to reveal damage in the failed metallurgically bonded diodes.

2. In all cases damage to the diodes was caused by local overheating above the melting temperature of silicon. Depending on the dissipated power and the pulse duration the overstress caused changes in the characteristics of the diodes varying from a hard short circuit with a resistance of less than 1 Ohm, to a subtle increase in the leakage current and/or decrease in the breakdown voltage that might not exceed the specification limits.

3. Hard shorts in the diodes with a resistance of less than 1 Ohm were caused by a three-dimensional web

of silver alloy with a thickness of approximately 0.1 µm which was formed across re-crystallized silicon, shorting the terminals of the diode. Shorts with a resistance from several Ω to KΩ were caused by the re-solidification of melted silicon/silver/nickel alloy within the P-N junction area. Softening of the reverse I-V curves was due to damage a few micrometers in size with only minor disruptions in the P-N junction area.

4. Relatively large forward current pulses of more than 1 ms and less than 400 A resulted in smooth, sphere-like damage with a size of 100 to 250 µm, located mostly in the central area of the die. Shorter, but higher amplitude pulses caused damage of 25 to 100 µm located at the mesa-slug interface. Heat transfer simulations showed that failures caused by forward current pulses in the millisecond range are due to fundamental thermal properties of silicon. These are not related to possible minor irregularities in the junction and/or metallization contacts. The Wunsch-Bell model can be used to estimate conditions of the forward bias EOS events.

5. The appearance of damage in TVS diodes overstressed by reverse voltage pulses in the millisecond range, is similar to diodes overstressed with forward current. This suggests a similarity in the heat transfer mechanisms in these diodes during forward and reverse voltage EOS events.

6. Short reverse voltage spikes of 1 to 3 µs duration above the breakdown level, and with a current of 10 to 200 mA in amplitude, resulted in surface breakdown and exhibited damage at the mesa-glass interface. The damage consisted of melted silicon with dimension of 5 to 20 microns and caused a softening of the reverse I-V curves and a decrease in the breakdown voltage.

The diodes that failed during burn-in testing had relatively high short circuit resistance measured in KΩ, caused by a small volume of melted and re-crystallized silicon/silver/nickel alloy measuring 5 to 10 µm in the bulk of the diodes. The small amount of damage initially caused in diodes by a short, microsecond range reverse voltage spike can be significantly enlarged providing a sufficient current follows through the weakened site once the initial failure has occurred.

The full version of the paper is published in the "Proceedings from the 26th International Symposium for testing and Failure Analysis", ISTFA 2000, 12-16 November, 2000, pp.425 - 434.

Evaluation of Thermo-Mechanical Stability of COTS Dual-Axis MEMS Accelerometers for Space Applications

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Introduction

Micro Electro-Mechanical Systems (MEMS) is one of the fastest growing technologies in microelectronics, and is of great interest for military and aerospace applications. Accelerometers are the earliest and most developed representatives of MEMS. First demonstrated in 1979, micromachined accelerometers were used in automobile industry for air bag crash-sensing applications since 1990. In 1999, MEMS accelerometers were used in NASA-JPL Mars Microprobe [1].

The most developed accelerometers for airbag crash-sensing are rated for a full range of ±50 G. The range of sensitivity for accelerometers required for military or aerospace applications is much larger, varying from 20,000 G (to measure acceleration during gun and ballistic munition launches), and to 10^{-6} G, when used as guidance sensors (to measure attitude and position of a spacecraft). The presence of moving parts on the surface of chip is specific to MEMS, and particularly, to accelerometers. This characteristic brings new reliability issues to micromachined accelerometers, including cyclic fatigue cracking of polysilicon cantilevers and springs, mechanical stresses that are caused by packaging and contamination in the internal cavity of the package. Studies of fatigue cracks initiation and growth in polysilicon [2, 3] showed that the fatigue damage may influence MEMS device performance, and the presence of water vapor significantly enhances crack initiation and growth.

Environmentally induced failures, particularly, failures due to thermal cycling and mechanical shock are considered as one of major reliability concerns in MEMS [1]. These environmental conditions are also critical for space applications of the parts. For example, the Mars pathfinder mission had experienced 80 mechanical shock events during the pyrotechnic separation processes [4].

In general, most of the analyses of the failure mechanisms in MEMS have been performed, using test structures. However, a comprehensive qualification of MEMS, requires experimental data obtained using real parts. In this respect, endurance characteristics of the accelerometers with respect to temperature cycling and mechanical shock is of great interest in their evaluation for space applications.

In the present study, thermo-mechanical stability of commercially available mass production accelerometers (ADXL250) available from Analog Devices was evaluated, by subjecting them to multiple temperature cycles in the range from –65 °C to +150 °C and mechanical shocks of 2000 G in the X and Z directions.

Part Description

Analog Devices ADXL250 is a dual-axis, surface micromachined accelerometer rated for ± 50 G and packaged in a hermetic 14-lead surface mount cerpack. The operating temperature range of the part is from –55 °C to +125 °C and the storage temperature range is

from –65 °C to +150 °C. The part can withstand acceleration up to 2000 G.

The device is fabricated using a proprietary surface micromachined process that has been in high volume production at Analog Devices, since 1993. The two sensitive axes of the ADXL250 are orthogonal (90°) to each other and in the same plane as the silicon chip. The differential capacitor sensor consists of fixed plates (stationary polysilicon fingers) and moving plates attached to the beam (inertial mass) that shifts in response to the acceleration. Movement of the beam changes the differential capacitance, which is measured by the on-chip circuitry (the clock frequency of the capacitance meter is 1 MHz).

Figures 1 and 2 show overall views of the chip and the capacitive sensor. Figure 3 shows a close up view of the polysilicon finger attachment.

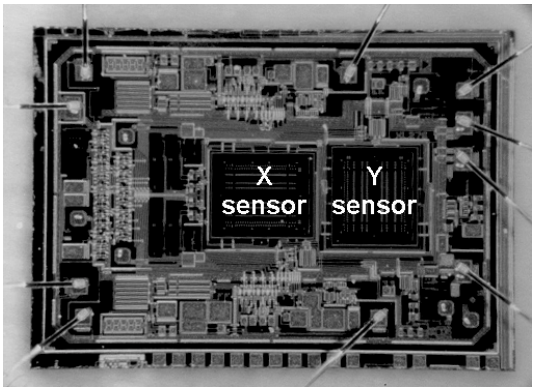

Figure 1. Overall view of the ADXL250 chip.

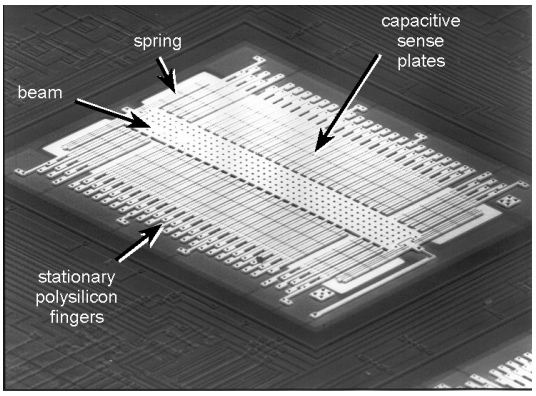

Figure 2. Overall view of the capacitive sensor.

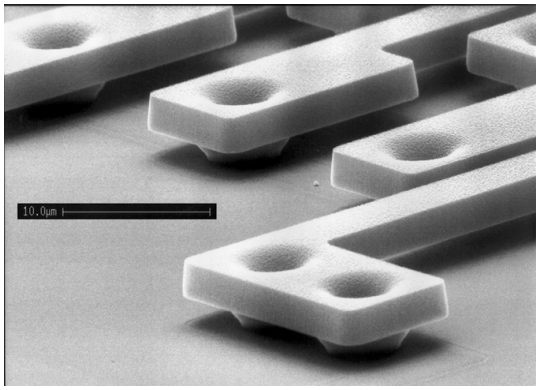

Figure 3. Close up of the stationary polysilicon finger attachment.

The sensor has 12-unit capacitance cells for electrostatically forcing the beam during a self-test. During a logic high on the self-test input pin, an electrostatic force acts on the beam equivalent to approximately 20% of the full-scale acceleration input, activating both the entire mechanical structure and the electrical circuitry. The polysilicon electrodes have a thickness of 2 µm and are suspended approximately 1 µm over the surface by means of two long and folded polysilicon beams, acting as suspension springs.

The overall capacitance of the sensor is small, typically in the order of 0.1 pF and during acceleration, the capacitance variation, which is measured by the on-chip electronics, ranges from 0.001 to 0.01 pF [5].

Temperature Cycling Test Results

Temperature cycling was performed on 10 parts in the range from – 65 °C to +150 °C, with 15 minutes dwell time at each temperature. Measurements were taken after 100, 200, 400, 700, and 1000 cycles. Figure 4 shows results of this test. No failures or any significant changes in parameters of the parts were observed.

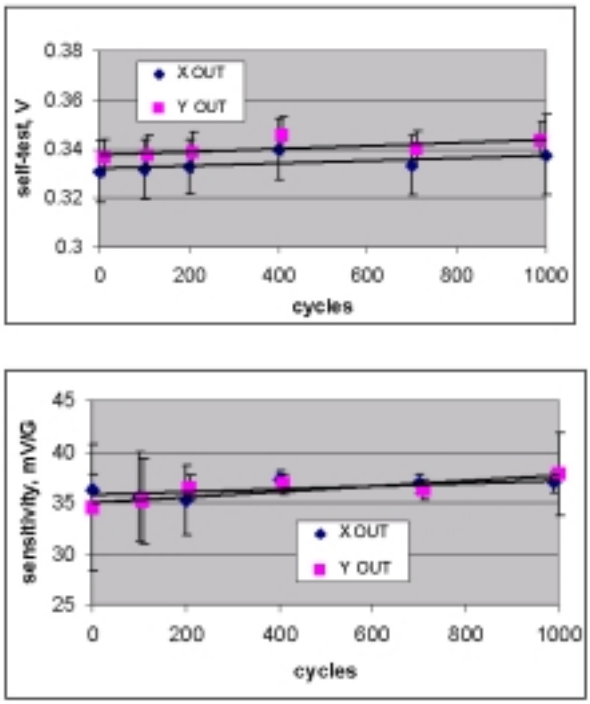

Figure 4. Temperature cycling effect on parameters of the accelerometer.

Mechanical Shock Test Results
Mechanical shock testing was performed on two groups of devices with ten samples in each group. The first group was subjected to 2000 G shocks in X-direction and the second group to 2000 G shocks in Z direction.

Measurements were taken after 100, 300, 1000, 3,000, 10,000, and 30,000 shocks.

All parts in the second group withstood 30,000 shocks with only minor changes in their parameters (see Figure 5). One sample in the first group failed after 10,000 shocks with output Y stuck high (4.9 V). Parameters of samples in the first group also, did not show any significant changes during this testing (see Figure 6).

All samples in both groups except for the failed one, passed PIND testing. The failed part exhibited permanent noise bursts indicating presence of free particles inside the cavity.

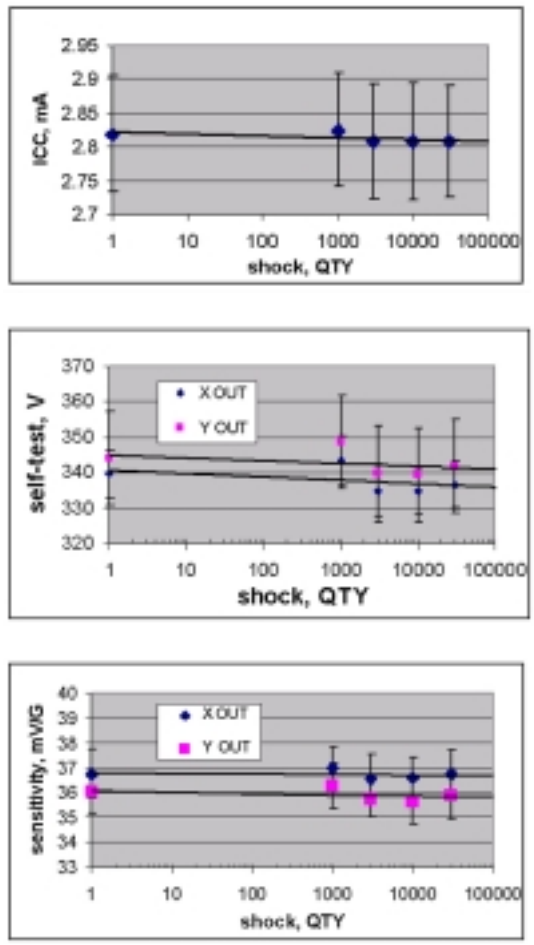

Figure 5. Z-direction mechanical shock effect on parameters of the accelerometer.

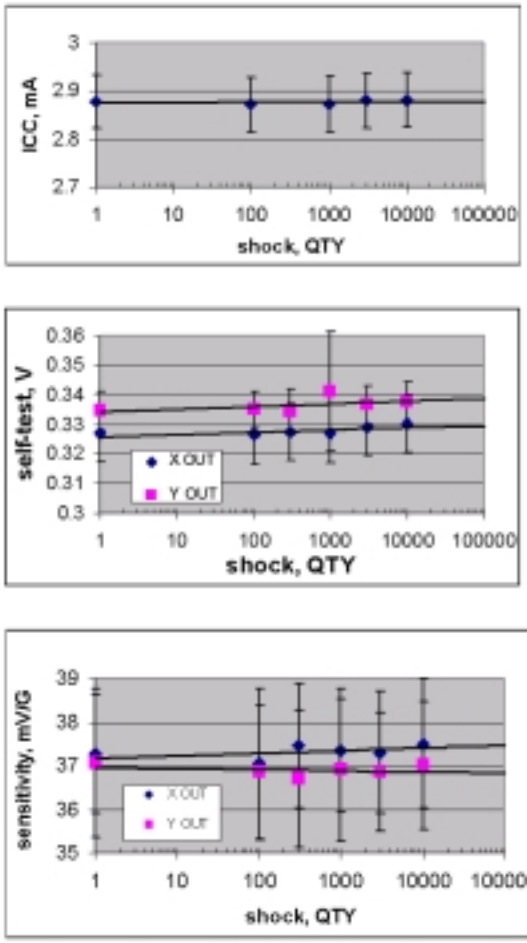

Figure 6. X-direction mechanical shock effect on parameters of the accelerometer.

Internal Examination and Failure Analysis

The failed part and several good parts from different groups were decapsulated after testing and examined using optical and SEM microscopes. No microcracks or other defects, which would indicate fatigue-related damage in the sensors, were observed in any of the parts. Figure 7 shows typical close-up views of the polysilicon spring ends after temperature cycling and mechanical shock testing.

A site with a structural anomaly was found in the sealing glass of the failed device. This site had excessive voiding and porosity, which most likely was due to a contaminant embedded in the glass (see Figure 8).

Electron beam induced current technique (EBIC) was used in attempt to find any anomaly in the failed Y-channel electronic circuit as compared to the X-channel. EBIC images of the two channels were similar, suggesting that no damage to electronics has occurred.

A small particle with a size of approximately 1 µm, which most likely chipped out from the package, was found jammed between the comb fingers in the Y-channel sensor in the failed part (see Figure 9). This particle appears to have wedged electrodes of the capacitor sensor, causing the Y output to be stuck high.

Discussion

The process of decapsulation of ceramic packages, usually generates glass and/or ceramic particles, making it harder to identify the original particle, which was expected in the failed part. However, the following observations suggest that the failure was due to the packaging problem:

1. Only the failed part had loose particles inside the cavity, detected during PIND testing.

2. Sealing glass in the failed part had a site with excessive porosity and local mechanical stresses caused by the embedded foreign material (contaminant). This facilitated glass cracking during the mechanical shocks and resulted in chip-outs and generation of loose particles.

3. A particle jammed between the electrodes was found in the capacitor sensor of the stuck Y channel of the failed part.

No indication on possible damage to the polysilicon fingers and/or springs, or to the electronics was found.

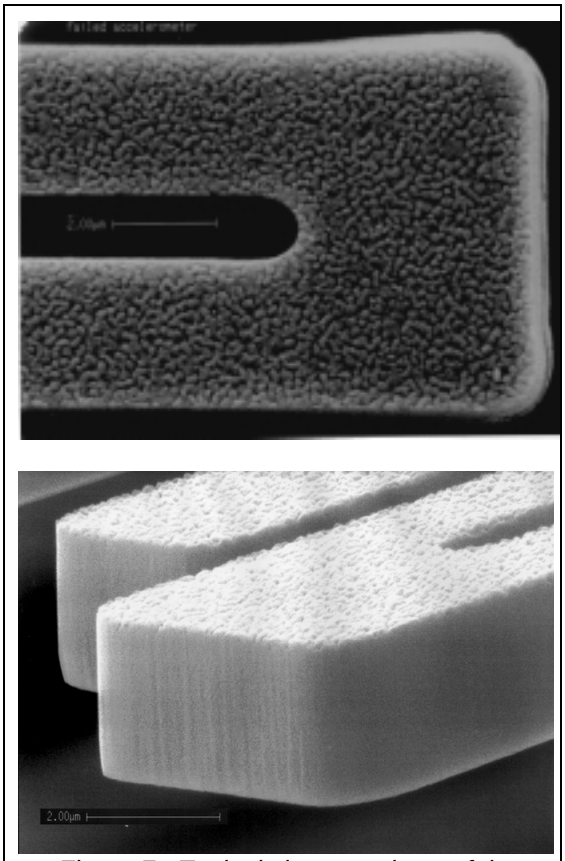

Figure 7. Typical close up views of the polysilicon spring ends after temperature cycling and mechanical shock testing.

The observed failure, stresses the need for thorough control of packaging materials and process for MEMS and for accelerometers, in particular. For example, the adaptation of new packaging solutions for MEMS, such as the use of cap-on-chip technology [6], would probably eliminate problems associated with loose particles in the package.

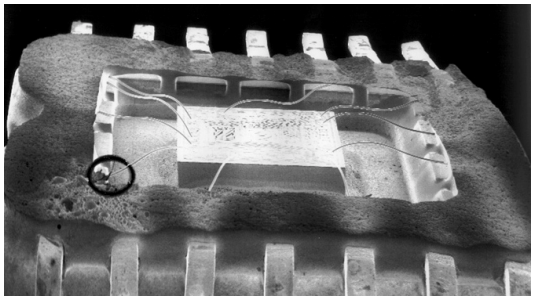

Figure 8. Structural anomaly in the sealing glass of the failed part (bug-in-the-glass).

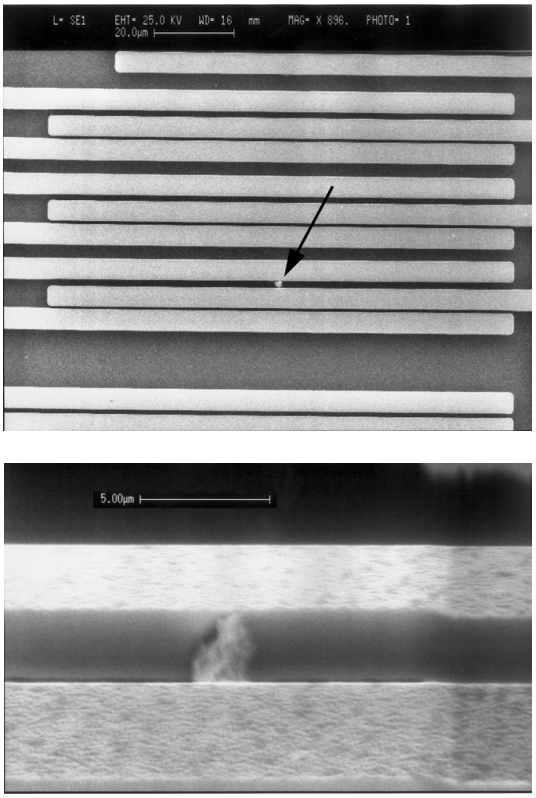

Figure 9. Overall and close up views of a particle jammed between the plates of the capacitive sensor in the failed part, channel Y.

Conclusions

Analog devices ADXL250 dual-axis accelerometers successfully withstood 1000 temperature cycles in the range from –65 °C to +150 °C, as well as 30,000 mechanical shocks of 2000 G in

Z direction and 10,000 shocks in X-direction, with only minor parametric changes. No evidence of fatigue-related defects or microcracks in the stationary polysilicon fingers and/or springs were observed.

One part failed, with output Y stuck high after 10,000 shocks in the X-direction. The failure most likely was caused by a structural defect in a sealing glass (contaminant), which enhanced glass cracking and formation of loose particles. During the mechanical shocks, a small particle of submicrometer range size, appeared to have broken loose and lodged in space between the capacitive sense plates, wedging the electrodes and causing failure of the device.

The results demonstrated that mechanical robustness of the micromachined accelerometers is adequate for most aerospace applications, provided a proper control and qualification of the packaging materials and processes is performed.

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Preliminary Reliability Evaluation of Copper-Interconnect Metallization Technology

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Background

The advantages of using copper for interconnection in microcircuits are mostly due to its lower resistance compared to the aluminum metallization. Copper-based metallization has specific resistance of less than 2 μΩ-cm compared to more than 3 μΩ-cm for aluminum metallization. In combination with a reduced susceptibility to electromigration failures, this enables designing of highly scaled devices with significantly reduced time delays. These features are mostly beneficial for high-performance microprocessors and fast static RAMs (FSRAM).

In addition, copper interconnect process uses the dual damascene technology for deposition of copper, which can potentially reduce the manufacturing cost by eliminating some labor intensive steps of aluminum etching. This makes copper interconnect use quite attractive for semiconductor industry, and positions this technology as a standard interconnect process for the most high performance microcircuits in the future.

Major problems with copper metallization are due to some specific physical/electrochemical properties. Copper does not create a passive oxide film (as aluminum does), has poor adhesion and high rate of diffusion through silicon and dielectric layers (organic and inorganic). This introduces new failure mechanisms such as poisoning of the P-N junctions, charge instability and formation of resistive shorts caused by copper electrochemical migration.

The first on the market, copper-based FSRAM was manufactured by Motorola (the part is available since 1999). This part was used to gain experience with the copper-based interconnect design and technology, to analyze problems related to their evaluation and to obtain preliminary results of destructive physical analysis (DPA) of the parts.

Due to constraints caused by relocation of the GSFC Parts Analysis Lab, cross-sectional analysis of the part was performed by the Chipworks, Inc., Ottawa, ON, Canada [1].

Part Description

The XCM63R836RS3.3 is an 8M–bit synchronous, late write, fast static RAM designed to provide high performance in secondary cache and ATM switches, telecommunications, and other high speed memory applications. The part is organized as 256K words by 36 bits, and is fabricated in Motorola's high performance silicon gate CMOS technology (0.15 μm process). The technology employs copper interconnect metallization based on the damascene and dual- damascene processes.

The part features low cycle time of 3.3 ns, low power supply voltage of 3.9 V maximum for the core supply voltage and 2.5 V maximum for the output supply voltage. Operating temperature range of the part is specified as 0 °C to

70 °C, temperature under bias is –10 °C to 85 °C, and storage temperature is –55 °C to 125 °C.

The part is designed as a Flipped Chip Ceramic Ball Grid Array (CBGA). Figure 1 shows external views of the part. It should be noted that no underfill compound was used in this design. The chip is mounted directly on a ceramic board using the flip-chip solder bump technology. Bottom side of the board has 119 solder bumps, which are organized in a 17×7 array with a 50 mil (1.27 mm) pitch.

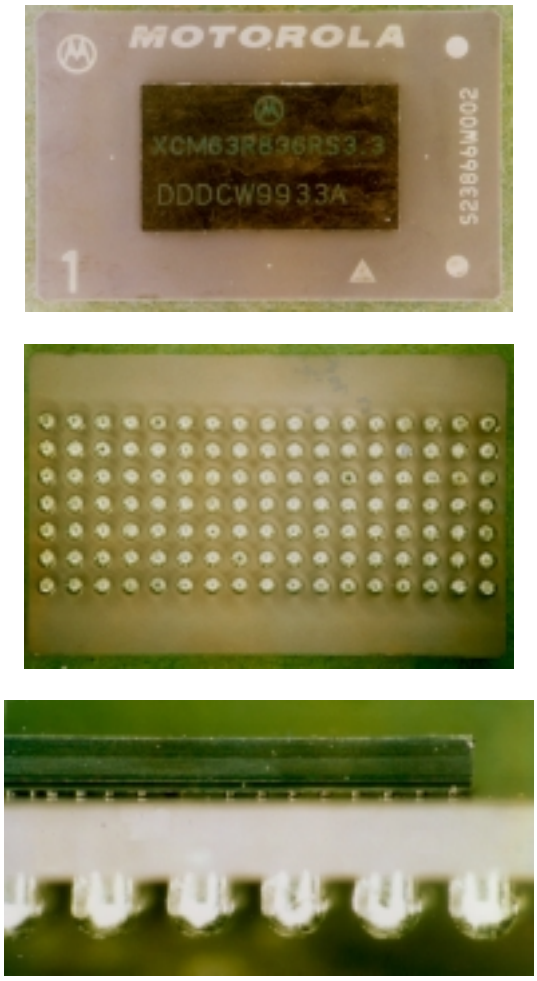


Figure 1 - External top, bottom, and side aspects of the part.

Processing And Reliability Challenges In Cu-Based Interconnect Metallizaton Microcircuits

Copper Damascene Process.

The damascene process, and its twin, the dual-damascene process, are considered to be the future technology of choice for laying metal lines and interconnects on chips [2]. The single greatest advantage is that the metal etch steps, which are notorious for process problems (corrosion, resist burn, time criticality with resist, etc) no longer exist, since all patterning is done with dielectric etching (currently, oxide etching). This enables previously unusable metals, in particular copper, to be reconsidered for interconnect metallization. Some of the key elements of copper damascene processes are described below.

Single Damascene. The fundamental difference of damascene relative to the standard processing is that the metal lines are not etched, but deposited in "grooves" within the dielectric layer, and then excess metal is removed by chemical-mechanical planarization (CMP) (Figure 2a).

Dual-Damascene. The differences of dual damascene relative to single damascene processing are that the plugs are filled at the same time as the metal lines. Several processing options exist for dual-damascene, and Figure 2b shows the currently preferred method, since the thickness of the metal lines can be accurately controlled.

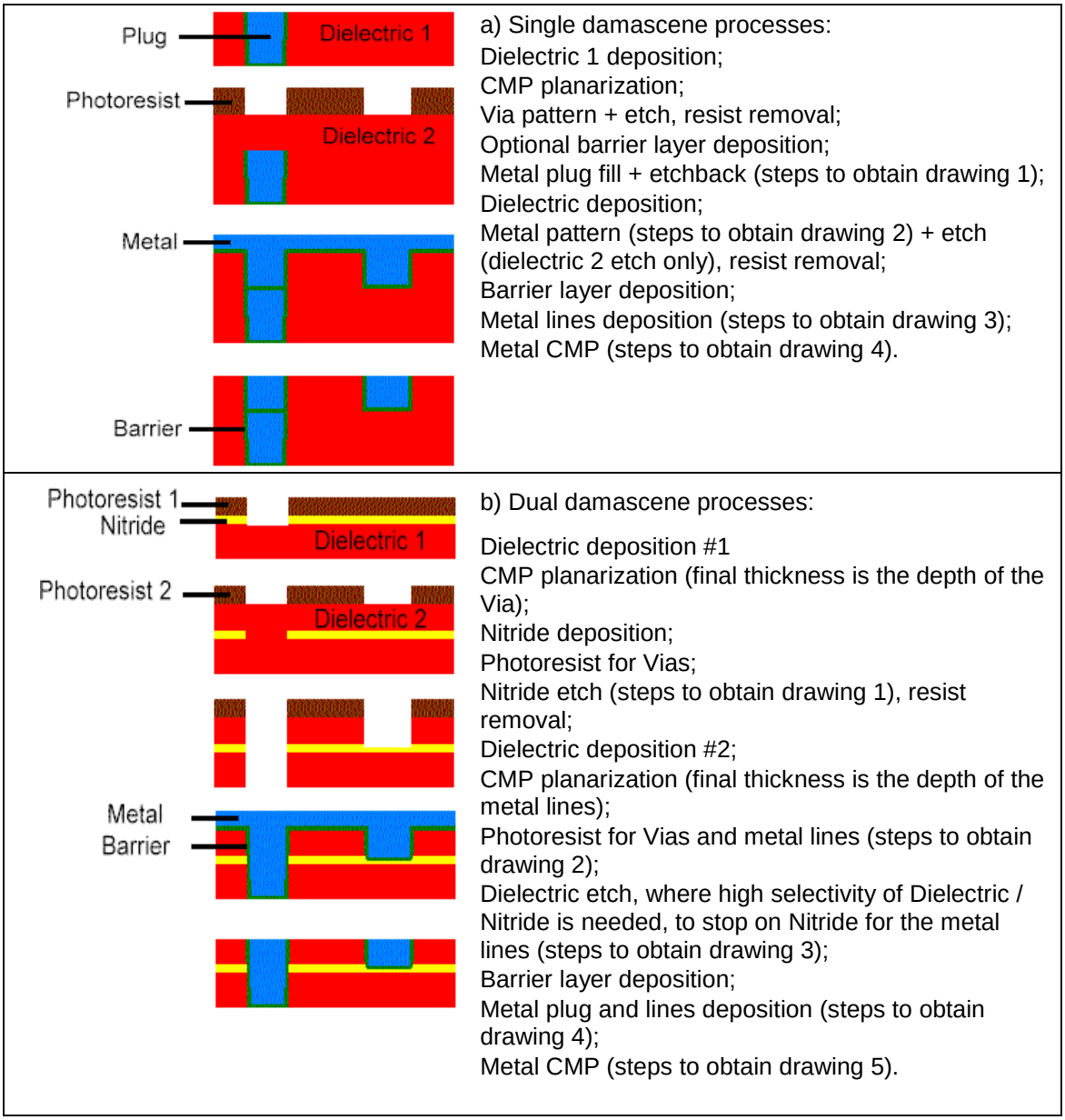


Figure 2 - Single (a) and dual (b) damascene processes.

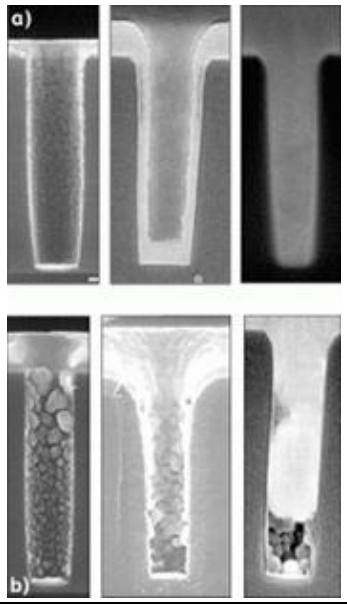
Process Challenges

Metal Deposition. The deposition of copper is made difficult since there is a need to fill holes and trenches, a requirement previously non-existent. Older physical vapor deposition (PVD) techniques were used for low aspect ratios (holes, which are not very deep or which. are wide), but they are not sufficient for the requirements of new designs.

Contemporary copper PVD seeding and subsequent fill by the electroplating technique have become the processes of choice to produce void-free fill of high-aspect-ratio (AR) damascene features

[3]. Following the barrier layer, a thin continuous copper seed layer promotes adhesion and facilitates the subsequent growth of the bulk copper fill by electroplating.

To achieve high filling performance, the incoming feature profile, seed layer attributes, and key electroplating process and chemistry parameters must be optimized to encourage acceleration of deposition near the base of damascene features ("bottom-up" fill). The success of copper plating to fill high AR features is built upon the achievement of successful nucleation followed by rapidly accelerated Cu deposition. Figure 3 shows examples of normal and defect-generating processes of copper deposition.



Cross-sectional via images showing (left to right):

a) smooth seed coverage only, metal profile following partial fill, complete fill by electroplating.

b) agglomerated seed coverage, metal profile following some electroplating, and resulting void at completion of electroplating.

Figure 3 - Normal (a) and defect-generating (b) via filling processes.

Copper Chemical Mechanical Planarization (CMP). Planarizing copper is no less challenging than depositing copper for the damascene interconnect structures. Development is complicated by new barrier materials and the material properties of copper itself [4]. Copper CMP is more complex, because of the need to remove the tantalum or tantalum nitride barrier layers without overpolishing any features. This is difficult because current copper deposition processes are not as uniform as the oxide deposition process. Finally, tolerances for erosion and dishing are much narrower for copper CMP process.

Copper has properties that add to the polish difficulties. Unlike tungsten, it is a soft metal and subject to scratching and embedded particles during polishing. Also, because copper is highly electrochemically active and does not form a natural protective oxide, it corrodes easily. Therefore, protecting the copper surface during polish, clean and subsequent processing are essential.

Barrier Layer. Copper can diffuse rapidly in silicon, silicon dioxide and low-k dielectrics, requiring that an impermeable barrier protect these dielectric layers. The barrier layer must prevent Cu diffusion, exhibit low film resistivity, have good adhesion to both dielectric and Cu, and be CMP compatible [5]. Also, the barrier layer must be conformal and continuous to fully encapsulate the Cu lines with as thin layer as possible. Due to the higher resistivity of the barrier material, its thickness should be minimized to allow

for Cu to occupy the maximum cross-sectional area.

Much research had been performed to find the optimum, manufacturable barrier material and technology. Ta and TaN_X were found to be best candidates for the microcircuits with the feature sizes below 0.25 µm. It was shown that the high temperature diffusion of copper decreases with the increase of nitrogen content.

Sealant Layer. Copper's oxidation characteristics introduce another problem. Cu oxidize relatively slow (the activation energy is about 1 eV) but forms a porous oxide with a weak adhesion. Unlike aluminum, in which initial oxidation forms a stable protective layer that prevents further oxidation, copper can oxidize indefinitely. In time, this oxidation can make copper interconnects unreliable. This poses additional problems during manufacturing and, in particular, wafer level testing. A silicon nitride film was found to provide adequate sealing for the copper metallization.

Copper Interconnect Inspection Challenges

Historically, more than 70% of the killer defects in microcircuits have been related to interconnects [6]. As such, with the introduction of new materials and fabrication techniques such as copper metallization and dual-damascene processes, defects associated with fill (voids, blocked etches, and particulates) issues will predominate. Thus, detecting hidden defects inherent in these processes becomes more difficult.

Due to special physical and chemical characteristics of copper, it will be beneficial only if it is properly processed, and insuring this may require regular process monitoring and qualification [7]. One of the most effective solutions to this problem is an employment of advanced automated e-beam system, which can detect process defects that cannot be captured by optical inspection or conventional e-beam techniques.

This advanced high-speed e-beam automated inspection systems (SEMSpec) combines a proprietary, high-brightness, thermal-field emission source, unique electron optics, and a high-speed image processor. The system inspects wafers using a low beam energy of 1.0 keV at scan speeds that are much faster than with the traditional SEMs.

The SEM image is digitized and sent to a computer, where defect detection algorithms determine the acceptability of the pattern. This e-beam technology offers high resolution and large depth of focus; it can find defects as small as 0.10 µm in size, even on densely packed, high-aspect-ratio, multilayer geometries.

Highly sensitive voltage-contrast imaging provides additional defect detection capability. Voltages induced on the surface of the circuit elements by the high beam current generate the voltage contrast. A bright electron source, high beam current, and a novel, energy-filtering secondary electron detection system, produces a high sensitivity for voltage-contrast imaging and detection at the wafer level. This identifies defects based on differences between properly and improperly formed structures and allows detection of defects at both the surface and deeper layers. Similar contrasts are difficult to observe in conventional e-beam approaches.

Cu-Interconnect Metallization Reliability Issues

Implementation of copper metallization is potentially beneficial for reliability of the microcircuits. The higher thermal conductivity of copper compared to the aluminum allows the metallization to conduct more heat away from the silicon die. This, together with the lower resistivity of copper, and consequently, lower heat dissipation in the metallization, would tend to reduce die temperature during operation, and thus

improve performance and reliability of the part. Some of the key reliability issues are listed below.

Electromigration. Copper with its potentially higher electromigration threshold as compared to aluminum is considered to be one of the most promising advantages for use of copper metallization for highly scaled microcircuits. However, some experiments indicate erratic behavior of thin copper lines under high current conditions [8]. Literature data shows a variance of the median time-to-failure (MTF) during electromigration tests from 6 hrs to 200,000 hrs for test conditions of 100 °C and 5×10^5 A/cm^2. This range is wider than the one observed for the conventional Al/Cu systems (85 hrs to 12,500 hrs).

This is mostly explained by the surface-dominated electromigration in the thin copper conductors. The metal-oxide interface, which is largely eliminated as a pathway for mass transport in Al is quite active in Cu. Lot-to-lot variations, even an issue with aluminum metallization, may be even worse for copper metallization.

The grain size to line width dependence is less important for the copper metallization than for the aluminum. This is most likely due to the specific of Cu lines structure, which are never perfect "bamboo" structures, but are generally bamboo-like, single-crystal across a given line.

Test data has shown, CVD-fill Cu lines exhibiting near-bamboo structure in sub-0.5-µm lines, moving to more mixed structures as linewidths increased, until becoming fully multicrystalline at 2 µm. However, the electromigration results were very close, which means that grain-boundaries cannot be the diffusion path for electromigration atomic flux [9]. The similarity between single- and multicrystalline line electromigration results supports the conclusion that the diffusion path is along the Cu barrier layer. If true, this suggests that the quality of the interface between the barrier and the copper seed layer is the single most important variable in the lifetime of Cu lines.

Electrochemical Migration. Application of copper metallization may introduce a new failure mechanism into the systems, which has never occurred with aluminum metallization, and that is the electrochemical migration, which can result in short circuit formation between the adjacent metallization stripes under DC bias [10].

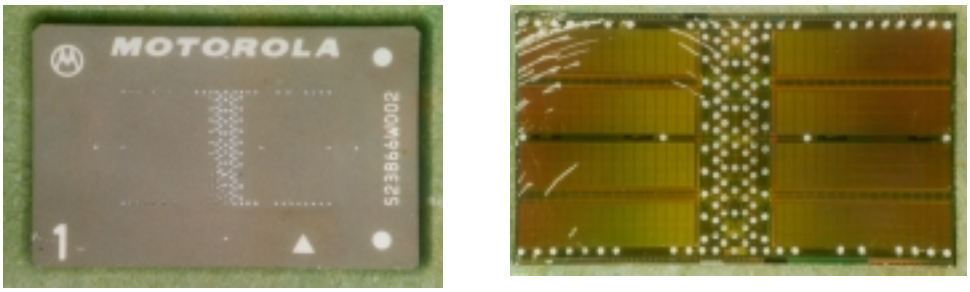
When a continuous moisture film or path occurs between two biased conductors, copper can be anodically dissolved from the positively biased line and redeposited in a dendritic form at the cathodic site. Similar failures may occur if sealing and passivation layers have pinholes and defects, which enable moisture penetration and condensation in the spacing between the copper interconnection lines.

Destructive Physical Analysis (Dpa) Of Cu-Interconnect 8m SRAMs

Optical Examination of the Die

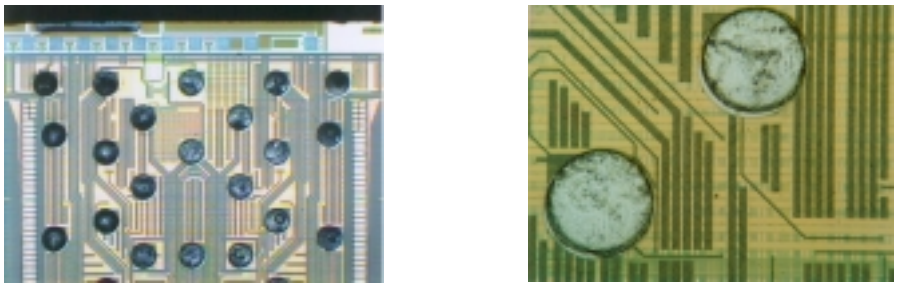
The die was removed from the ceramic board by heating up the assembly to approximately 250 °C. Figure 4 shows the ceramic substrate and the die after separation. The die had a size 12.1 mm X 7 mm and was covered with a relatively thick (approximately 4 µm) layer of polyimide film, which was removed by plasma etching for several hours. Figures from 5 to 7 show close-up views of the die surface and top level copper metallization. No patterning defects or any abnormalities on the die surface and/or the top-level metallization were observed.

Cross-Sectional Examination of the Die [The Chipworks, Inc. [1]]



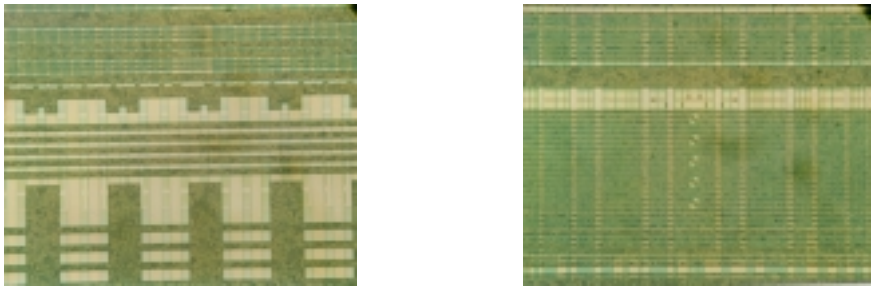
a) 4X b) 8X

Figure 4 - Ceramic substrate (a) and die (b) after the part deprocessing. The solder “threads” on the die surface (left top corner) were formed during desoldering. These "threads were located on the polyimide film and did not cause any damage to the die.



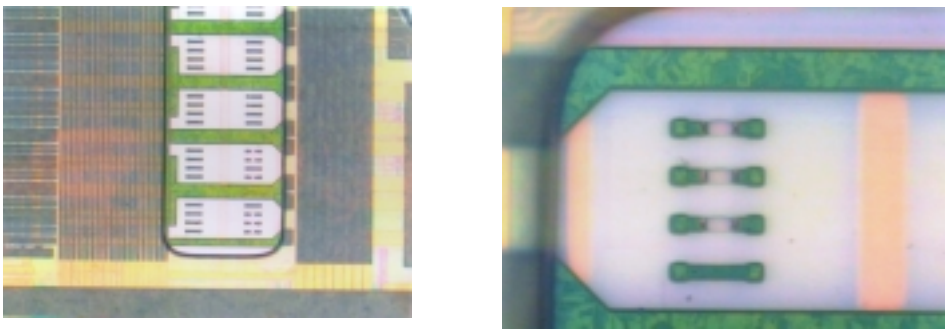
a) 50X b) 200X

Figure 5 - Close-up of the solder balls on the die.



a) 500X b) 500X

Figure 6 - Aspects of the top level copper metallization.



a) 200X b) 1000X

Figure 7 - Close-up of the fuses on the die surface.

Technique

One sample was cross-sectioned after decapsulation to evaluate dielectric and metallization properties. For objectivity, quality was assessed using MIL STD 883E, Class B criteria where appropriate, even though these devices were not procured to this specification. The dimensions used in this report are best estimates and have been obtained from the full library of images taken of this part. They are not necessarily measured from the images reproduced in this report.

Transmission Electron Microscope (TEM) analysis was performed to observe the microstructure of the copper and the barrier metal layer. Materials were identified using EDX (Energy Despersive X-ray) and EELS (Electron Energy Loss Spectrum). Secondary Ion Mass Spectrometry (SIMS) analysis was used to determine the overall concentration of different materials in the layers above the silicon substrate. Concentration traces are shown for the materials expected to be found in the device under analysis.

Die Processing Overview

The device structure utilizes four layers of copper metallization, one layer of tungsten local interconnect with tungsten plug contacts to the source/drains and gates. Shallow trench isolation is used throughout. A polysilicon layer forms the word lines and transistor gates and the minimum polysilicon wordline width is measured to be 0.15µm.

Copper Interconnect. The lowest copper layer is formed by the damascene technique 1 directly on to tungsten plug contacts. The successive copper layers are formed by the dual-damascene technique in which the contact plugs are created in the same deposition as the tracks. The anti-diffusion seal for the copper is tantalum. (No nitrogen was found in the tantalum). The lower three levels of copper tracks are sealed on the top surface by nitride. The uppermost copper layer is sealed with tantalum. Track thickness range from 0.38µm to 1.05µm and plugs range from 0.41µm to 0.76µm deep. The tantalum cap on the top metal layer is also used for fuse metallization.

Dielectric Layers. The silicon substrate and active regions are sealed with silicon nitride and several conformal layers of BPSG (Boron Phosphorus Silicon Glass), which are planarized by using CMP. Subsequent dielectric layers consist of a deposited silicon oxide layer with no boron or phosphorus doping. A silicon nitride (or oxynitride) sealant layer for the copper also acts as a diffusion barrier between the dielectric layers, and possibly an antireflection coating, while providing an indication of when to stop the CMP. The dielectric layers range from 0.24 µm to 0.84 µm in thickness.

A SIMS analysis of the dielectric layers was performed indicating that each layer with the exception of ILD1, was silicon dioxide. The ILD1 layer was BPSG composition. It is interesting to note that there is residual copper and aluminum coincident with the nitride sealant layers – probably due to absorbed copper and aluminum from an alumina-based CMP slurry.

0.18 µm Transistors. The wordline polysilicon width was measured at the cell access transistor gate oxide level on the FESEM cross-sectional micrographs and found to be 0.15 µm. The gate oxide is approximately 7 nm thick (see Figure 17).

Shallow Trench Isolation. The shallow trench isolation is about 0.33 µm. in depth and appears to be have a thermal oxide liner, which is then filled with CVD oxide and planarized by CMP (see Figure 17).

The die substrate is P+ type with an overlying P doped epitaxial layer. The die minimum dimension was 0.15 micrometers.

Tables 1 through 6 summarize constructional analysis of the 8 Mb SRAM. Figures 8 to 19 provide details of the construction analysis, design features, and various SEM/TEM cross-sectional view.

Table 1- Horizontal dimensions.

MinimumPadSize	120µm X l20um
MinimumPadWindow	65 µm. Diameter
MinimumPadSpace	202 µm.
MinimumMetal5width	1.94 µm.
MinimumMetal5space	1.56 µm.
MinimumMetal5pitch	3.50 µm.
MinimumMetal4width	1.7 µm.
MinimumMetal4space	1.7 µm.
MinimumMetal4pitch	3.4 µm.
MinimumMetal3width	0.35 µm.
MinimumMetal3space	0.52 µm.
MinimumMetal3pitch	0.88 µm.
MinimumMetal2width	0.43 µm.
MinimumMetal2space	0.35 µm.
MinimumMetal2pitch	0.78 µm.
MinimumMetallwidth	0.32 µm.
MinimumMetallspace	1.48 µm.
MinimumMetallpitch	1.8 µm.
Minimum Polywidth	0.15 µm
Minimum Polypitch	0.55 µm.
Minimum Polyspace	0.37 µm.
Cellsize	2.4um x l.8 µm.

Table 2 - Vertical Dimensions.

Die Thickness	0.70 mm.
Die coat	Polyimide 3.5 µm.
Passivation	Oxynitride 0.45 µm.
Metal5	1.05 µm (0.15um Ta + 0.8 µm Cu+0.10 µm Ta)
Interlayer dielectric (ILD)8	0.84 µm CVD oxide.
Sealant Layer (over copper metallization) on all dielectric layers above ILD2.	0.06 µm silicon nitride.
Metal4	0.5 µm (0.42 µm Cu+0.08 µm Ta)
ILDs7 and 6	0.28 µm CVD oxide+0.84 µm CVD oxide
Metal3	0.40 µm (0.32 µm Cu+0.08 µm Ta)
ILDs5 and 4	0.24 µm CVD oxide+0.84 µm CVD oxide.
Metal2	0.38 µm (0.3 µm Cu+0.08 µm Ta)
ILDs3 and 2	0.24 µm CVD oxide+0.4 µm CVD oxide.
Metal1	0.4 µm.
ILD1	0.57 µm BPSG+0.08 µm nitride
Plugs	0.76 µm.
Poly	0.15 µm.
Shallow Trench isolation	0.33 µm.

Table 3 - Dielectric Layers.

	Comments
Surface Oxide Defects	None observed.
Glassivation	0.45 µm oxynitride
Inner Layer Dielectric 8	0.84 µm oxide.
Sealant Layer (over copper metallizabon) on all dielectric layers above ILD2	0.06 µm silicon nitride.
Inner Layer Dielectric7	0.28 µm oxide.
Inner Layer Dielectric6	0.84 µm oxide
Inner Layer Dielectric5	0.24 µm oxide
Inner Layer Dielectric4	0.84 µm oxide
Inner Layer Dielectric3	0.24 µm oxide
Inner Layer Dielectric2	0.40 µm oxide
Inner Layer Dielectricl	0.60 µm BPSG (deposited in three layers) over 0.8 µm nitride layer.
Shallow Trench isolation	0.33 µm
Gate Oxide	≈7 nm.

Table 4 - Metallization.

	Plugs	Layer1
Type and Levels	Tungsten	CVD tungsten.
Minimum Dimension	0.30 µm	0.32 µm.
Minimum Spacing	0.22 µm	1.48 µm.
Minimum Pkch	0.52 µm	1.8 µm.
Thickness	0.76 µm	0.40 µm.
Quality	Good.	Good.
Voids	None observed	None observed.
Step Coverage	N/A	N/A

	Layer2	**Layer3**
Type and Levels	Dual-Damascene Copper Ta-Barrier Layer 0.08 um	Dual-Damascene Copper Ta-Barrier Layer 0.08 um
Minimum Dimension	0.43 µm	0.35 µm
Minimum Spacing	0.35 µm	0.53 µm
Minimum Pitch	0.78 pm	0.88 pm
Thickness	0.38 µm	0.40 µm
Quality	Good.	Good.
Voids	None observed.	None observed.
Step Coverage	N/A	N/A

Table 4 - Continued.

	Layer4	**Layer5**
Type and Levels	Dual-Damascene Copper Ta-Barrier layer 0.08 µm	Ta Capping Layer 0. 15 µm Dual-Damascene Copper Ta-Barrier layer 0.1 µm
Minimum Dimension	1.7 µm	1.94 µm
Minimum Spacing	1.7 µm	1.56 µm
Minimum Pitch	3.4 µm	3.50 µm
Thickness	0.50 µm	1.05 µm
Quality	Good.	Good.
Voids	None observed.	None observed.
Step Coverage	N/A	N/A

Table 5 - Polysilicon

	Comments
Type and Levels	Polysilicon
Siliciding Metal and Thickness	None observed.
Minimum Dimension	0.15 µm
Minimum Pitch	0.55 µm
Minimum Spacing	0.37 µm
Thickness	0.15 µm
Quality	Good.
Voids	None observed.

Table 6. Memory Cell.

	Comments
Cell Type	SRAM-6T
Cell Description	Load CMOS transistor
Storage Transistor Size(W/L)	0.33 µm/0.18 µm
Access Transistor Size(W/L)	0.33 µm/0.18 µm
Load Transistor Size(W/L)	0.33 µm/0.18 µm
Wordline Width/Pitch	0.18 µm/0.55 µm
Bitline Width/Pitch	0.43 µm/0.77 µm

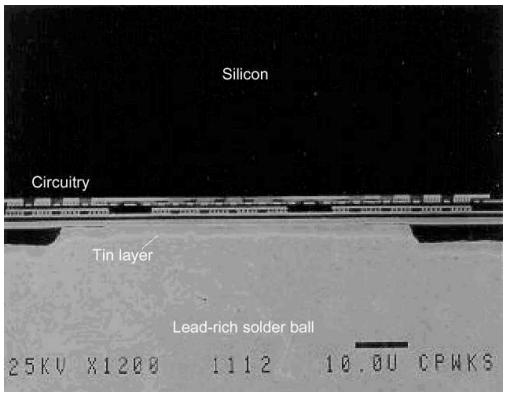
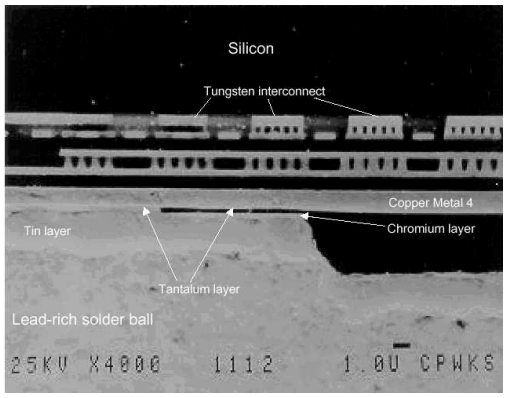
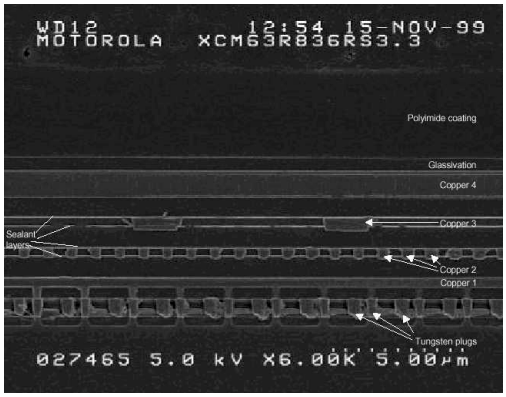
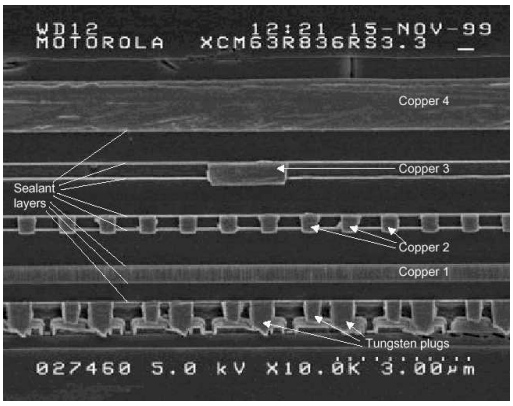
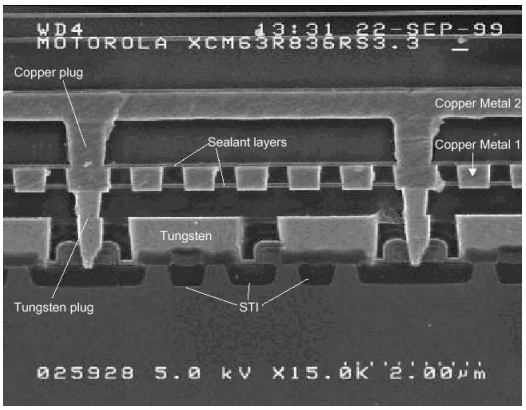
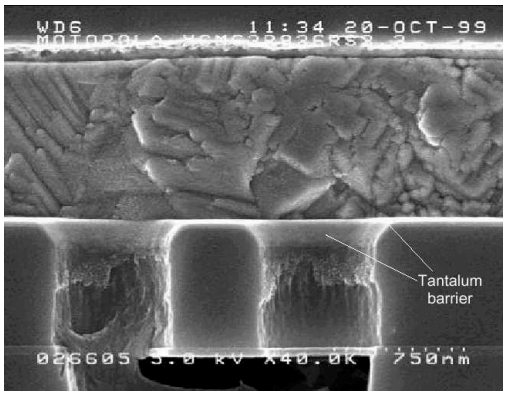
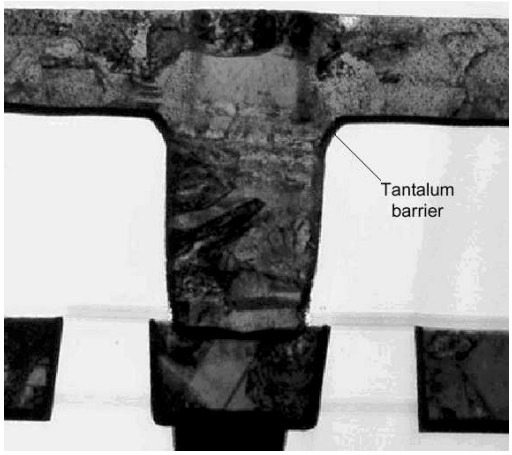
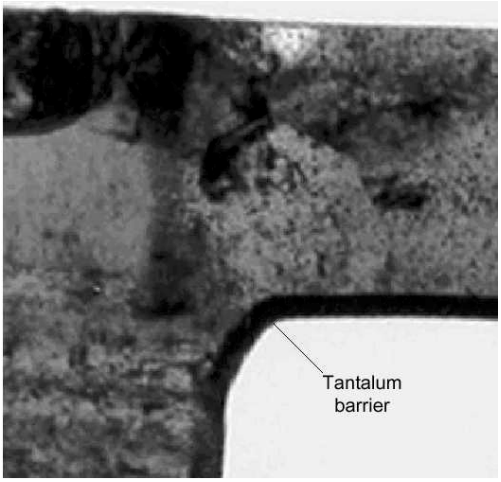


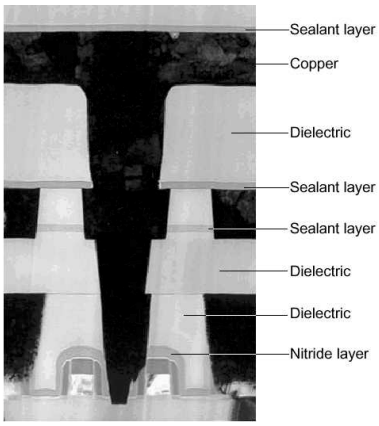
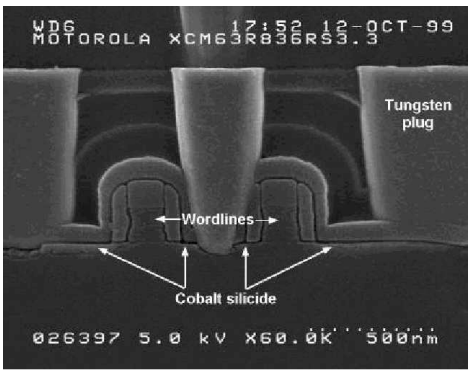
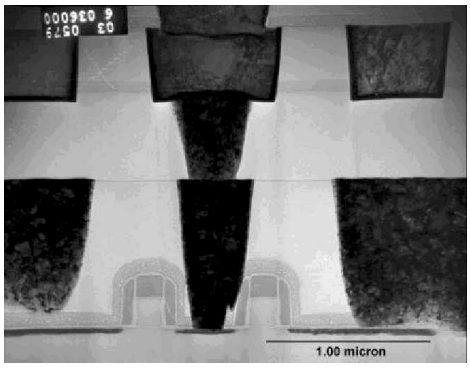
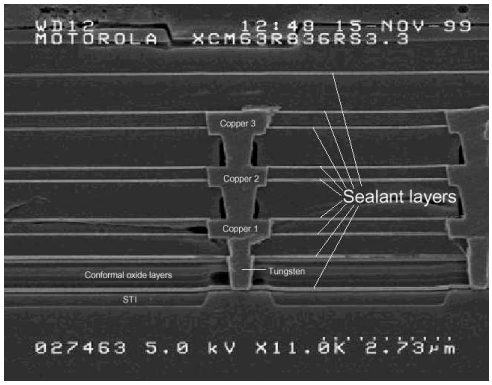
Figure 8.

SEM 1200X.

Cross-section through solder ball contact to pad metal.

	Figure 9. SEM 4000X. Cross-section through solder ball and pad metallization.
	Figure 10. SEM 6000X. Cross-section through copper and tungsten metallization structure.
	Figure 11. SEM 10000X. Cross-section through die metallization structure.
	Figure 12. 15000X. Cross-section through lower metal and dielectric layers.

	Figure 13. SEM 40000X. Cross-section through metal track high-lighting copper grain structure and tantalum barrier metal.
	Figure 14. TEM ~40000X. TEM image of cross-section showing copper grain structure and tantalum liner.
	Figure 15. TEM ~50000X. Closer view of tantalum barrier layer.

	Figure 16. TEM ~30000X. TEM image showing dielectric layers and sealant layers. Copper Sealant layer
	Figure 17. SEM 60000X. Cross-section through transistors and contacts.
	Figure 18. TEM ~39,800X. Cross-section through transistors and contacts.
	Figure 19. SEM 11000X. Cross-section of edge seal structure. (Dielectric fault is etching artifact).

Conclusions

Analysis of possible failure mechanisms specific to copper-based metallization shows that the presence of pores or defects in the sealant and/or barrier layers and voids in the copper-filled vias might have much more dramatic effect on reliability of the microcircuits compared to conventional microcircuits with aluminum metallization. The quality of sealant and barrier layers as well as the copper vias should be one of the prime concerns during destructive physical analysis of the part and might require development of special techniques for their evaluation.

The Motorola XCM63R836RS3.3 SRAM employs CMOS technology with four copper metal layers, one tungsten local interconnect layer and a single polysilicon layer. The copper metal interconnect layers are formed using dual-damascene processing with a tantalum-based barrier layer on the bottom and sides of the metal and silicon nitride sealant layer on the top. The top surface seal is formed with silicon nitride on all tracks except for the top-level metal tracks, which uses a thicker tantalum layer. This thicker cap layer is also used to form fuses. The device has tungsten local interconnect with tungsten plugs connecting to the source/drains and gates. The single polysilicon layer is not silicided in the array area. Peripheral circuitry in the SRAM is salicided with cobalt.

The construction analysis performed did not reveal any defects or obvious reliability concerns. However, test structures specially designed for a given Cu-Interconnect process evaluation, are required for technology assessment and validation.

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