ELECTRONIC PACKAGING & SPACE PARTS NEWS

EEE Links

April 1998, Vol. 4 No. 2

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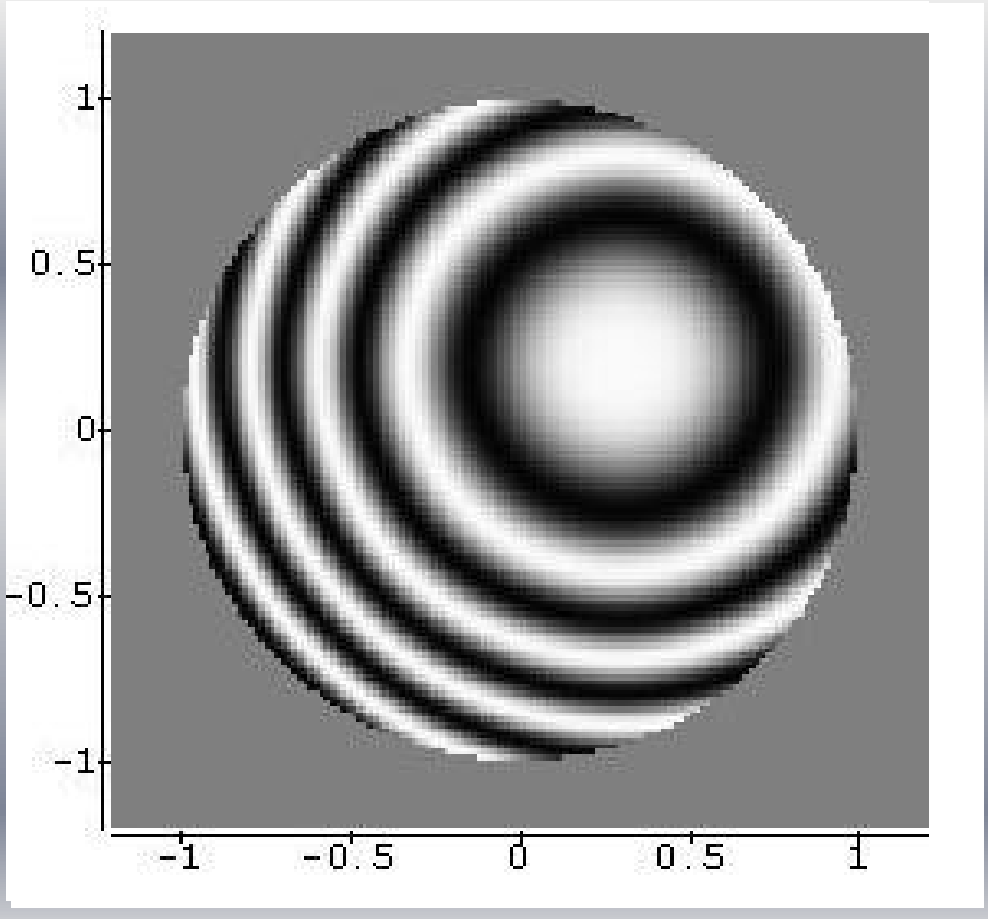

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WWW URL Address:
http://arioch.gsfc.nasa.gov/312/Linkspg.html

The cover photograph shows the mapping of the top of a fiber using Interferometry.
(See article on page 3).

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Letter from the Editor

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Welcome to the April issue of EEE Links. In an effort to improve accessibility to the electronic version of the EEE Links we have switched to a PDF format for the EEE Links Web page. This format will allow users to download the entire issue much faster and easier.

As always, please keep us informed of your questions and needs so that we may be able to serve you better.

Call for Papers
Microelectronics Reliability and Qualification Workshop
June 16-17, 1998

Jet Propulsion Laboratory
4800 Oak Grove Drive
Pasadena, California
Sponsored By: EEE Parts Program
Jet Propulsion Laboratory

The EEE Parts Program at JPL will sponsor the Microelectronics Reliability and Qualification Workshop on June 16-17, 1998 in Pasadena, California. The purpose of the workshop is to provide a forum for open discussion in all areas of microelectronics reliability and qualification for high reliability and commercial applications. Papers presenting the latest results in microelectronics device reliability and qualification methodologies or work in progress are solicited. General topics of interest include:

- Reliability
- Design of Experiment
- Qualification
- Failure Mechanisms
- Inspection and Verification
- Environmental Studies
- Process Verification
- COTS
- Compound Semiconductors
- Optoelectronics
- Low Temperature Applications
- Power Converters
- ASICS
- Mixed Signal Devices
- Memories
- Microprocessors
- Passive Components
- Reliability Modeling
- Materials Issues
- Thermal & Dynamic Analysis
- Quality Assurance Practices
- Accelerated Testing
- Production and Yield Enhancement
- Radiation Effects

PAPER SUBMISSION

Prospective authors are requested to submit an abstract of approximately 100 words in topical outline. The abstract must include the author's name, affiliation, complete address, telephone number, and FAX number and be suitable for a 20-minute presentation. The abstract must state: (1) the purpose of the work and what problems and questions are being addressed, (2) the results or conclusion of the work, and (3) how the work advances the knowledge of microelectronics reliability or qualification. Authors are responsible for obtaining all required company and government clearances prior to submission. Summaries must be received by May 1st, 1998. Authors are requested to submit a camera-ready original of view graphs at the time of presentation.

REGISTRATION

Registration fee – None.

For registration and further information, contact:
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Off-the-Shelf Class S Products

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The Class S and Class V available parts inventory publicized by the JPL Electronic Parts Engineering Office Webpage (go to *http://parts.jpl.nasa.gov/* then click on *Inventory*) has greatly enhanced part acquisition. Recent examples include:

For SeaWinds QuickSCAT TWTA, Class S parts were located, quoted, procured, and delivered within 60 days. Only one custom transistor was upgrade screened taking 12 weeks. All parts are delivered to the Program.

For SeaWinds QuickSCAT SES, Class S parts were located, quoted, procured, and delivered across the nation to our subcontractor in Florida within 30 days.

For Seawinds QuickSCAT PBIU, Class S parts were located, quoted, procured, and delivered to our subcontractor in Pomona, CA within 2 weeks. The subcontractor wrote "Under normal circumstances, this type of design, fabrication and testing takes 6 to 7 months to produce flight hardware. ... Thank you very much for meeting all our flight parts and material need dates enabling us to to meet our commitment [3 months schedule]..." "Using your help and the On Line Acquisition system, we were able to exercise a true concurrent engineering process by designing around available parts and materials rather than ordering it after design."

For SeaWinds QuickSCAT Converter, Class S parts were located, quoted, procured, and delivered within 3 weeks. An additional high power diode was located and supplied to our satellite manufacturer in Colorado within 2 weeks.

Our subcontractor Raytheon E-Systems in Florida "used the website to fulfill a USA Frequest for the Milstar Program finding all Class S parts needed on our website and available within 30 days". Additional information from the industry, is "the JPL website is extremely helpful in locating and preparing quotations in real time".

Commercial Off-the-Shelf (COTS)

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Commercial Off-The-Shelf (COTS) Plastic Encapsulated Microcircuits (PEMs) packages are widely used in the commercial electronics marketplace. They are now being considered for military applications in lieu of hermetic packages. JPL is also evaluating PEM's for Space applications. Office 507-Electronic Parts Engineering has recently evaluated plastic packages for delamination type defects using Acoustic Micro Imaging. Below is the abstract from a recently released report titled "Plastic Parts Delamination Validation Using Failure Analysis Methods". For further information contact Ken Evans (818) 354-4834 or Mike Sandor (818) 354-0681.

ABSTRACT

Acoustic Micro Imaging (AMI) was successfully employed by JPL Office 507 to evaluate Commercial Off-The Shelf (COTS) plastic encapsulated microcircuits (PEMs). A number of samples from different commercial vendors were purchased and then evaluated using C-Scanning Acoustic Microscopy (C-SAM)™ analysis. C-SAM™ is one of the Acoustic Micro Imaging (AMI) methods available for non-destructive detection of delamination. A number of interesting anomalies and potential reliability defects were found including minimum die attach (10%), voids at the leads within the encapsulant, thinning encapsulant, and mylar tape used in the assembly of the package. These anomalies detected by C-SAM™ imaging were analyzed using failure analysis cross sectioning to establish the validity of AMI as a tool. All anomalies and defects were verified. The success of the validation demonstrates that C-SAM™ can be used in screening parts for flight hardware. Parts that exhibit certain types of defects that could lead to long term reliability problems would be rejected based on risk criteria.

The NASA Parts Selection List (NPSL) is Available On-Line

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Intelligent EEE parts selection and application is critical to the success of NASA spaceflight programs. The appropriate "up-front" device choice streamlines integration and significantly improves system reliability. An improperly chosen device may have a measurable impact on project cost and schedule in the event of substandard device performance or failure.

The *NASA Parts Selection List (NPSL)* is a World Wide Web-based EEE parts selection toolkit. The NPSL provides on-line access to information that will guide the design engineer, parts engineer or experimenter to sound selection and application of EEE parts. Although the NPSL's prime beneficiary is the university experimenter or small contractor who has little or no parts engineering expertise, NASA's prime contractors and OEMs will find extensive and valuable parts information available at their fingertips.

The NPSL is fast becoming NASA's baseline parts selection guideline in lieu of MIL-STD-975 (NASA's Standard EEE Parts List which is being canceled) and Goddard Space Flight Center's (GSFC) PPL-21 (Preferred Parts List which may no longer be maintained).

Some of the improvements provided by the NPSL over its predecessors are:

- Fast, Unrestricted World-Wide Access
- Robust Selection Lists for EEE Parts for Spaceflight Applications
- Full Part Number/Ordering Explanations
- Available/Suitable Sources of Supply for the Listed Part Types
- Detailed Application Notes/Guidelines/Lessons Learned
- Dimensional Drawings/Outline Configurations/Connector Insert Arrangements
- Links to Additional Part Reliability Databases (Radiation Effects/Construction Analyses)
- Links to Manufacturer's Homepages for Catalog Info

In particular, the selection sections for connectors, wire and cable are growing rapidly and provide especially valuable guidance (connector insert arrangements, pros and cons of various wire and cable insulation types). The NPSL is a "living" homepage which is regularly updated with new parts for selection and new application guidelines to help spaceflight projects make wise parts decisions and avoid costly part problems. The administrators of the NPSL at NASA GSFC encourage your feedback to help identify areas for update and improvements that will provide the most value to the spaceflight EEE parts community.

The NPSL has been developed by NASA GSFC as part of the NASA Parts & Packaging Program administered jointly by GSFC and the Jet Propulsion Laboratory (JPL) and funded by NASA Headquarters. This toolkit is available on-line at:

http://misspiggy.gsfc.nasa.gov/npsl

Geometry Related to Fiber-End Polishing

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INTRODUCTION

An optical fiber is terminated in a ferrule. We wish to form the end of the fiber into a dome --- which we will suppose can be accurately modeled as a segment of the surface of a sphere --- satisfying two conditions:

- the center of the sphere corresponding to this dome must be co-incident with the fiber's optical axis, and
- the radius of curvature a_d of this dome must have a specified value.

Of course, each condition need only be met to within a specified tolerance.

An end-finisher is used to create the domed end-surface. This is a rotating flat disk faced with a resilient material (e.g., rubber) charged with a polishing agent. The ferrule is clamped into a fixture that holds it approximately normal to the flat rotating face, and then presses it against this face. This will polish the end of the ferrule, including the exposed end of the optical fiber, into a dome.

The radius of curvature is determined by the resiliency of the facing material and by the pressure with which the ferrule is pushed into the face. The center of the sphere is not necessarily coincident with the axis of the fiber since it is difficult in practice to achieve a precisely normal condition, and, even if this were done, the polishing action is not necessarily isotropic around the fiber axis. Thus, the usual procedure is to set the fixture at some initial (nearly normal) orientation, polish, and observe the off-set error. Then one resets the orientation of the fixture, re-polishes, and re-observes. A skilled operator is able to gradually reduce the off-set error to within acceptable limits in this way. Also, the pressure is adjusted until the desired radius is achieved: this too is accomplished by iteration.

The purpose of this article is to detail the geometry so that a procedure can be developed to adjust the orientation of the fixture so that coincidence can be reached by calculation --- this will reduce our dependence on skilled operators. Perhaps we may even be able to minimize the off-set error faster by calculation, than a skilled operator can reduce it by experience.

MAPPING THE TOP OF THE FIBER USING INTERFEROMETRY

A fixture holds a fiber optic assembly (fiber and ferrule), presenting the domed face of the fiber to an interferometer. The side view and the top view are shown schematically in Figure 1.

Note the (x,y)-coordinate system imposed onto the top view, which is a schematic of the interferogram. Figure 2 illustrates the full pattern available in a typical interferogram. (The all-over phase of the pattern depends on the choice of the reference phase plane. This image supposes that the reference has been adjusted to make the central zone bright.)

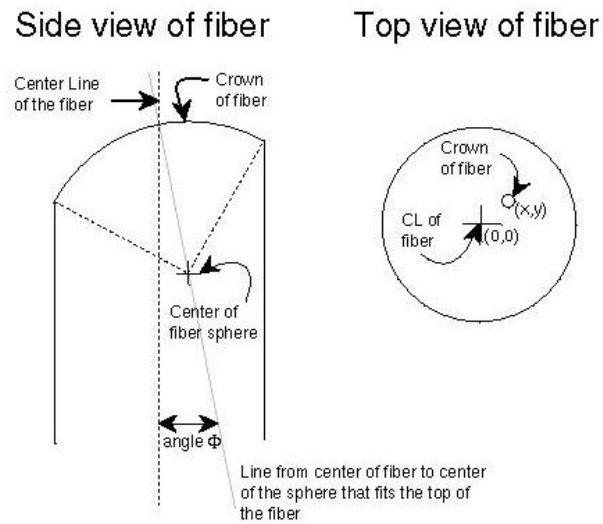

Figure 1: Fiber Drawing
Side and top view of the end of a fiber optic with a domed top. An (x,y)-coordinate system is assumed for the top of the fiber, in which the center of the fiber is at (0,0) and the crown of the dome is at (x,y).

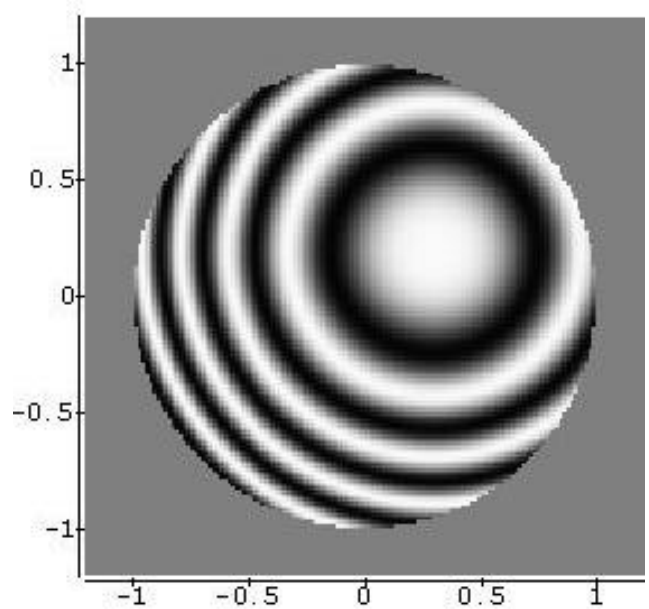

Figure 2: Interferogram
A typical interferogram. The center of the fiber is at (0.0,0.0) and the crown of the dome is at (0.3,0.2) in units in which 1.0 is the radius of the fiber.

Analysis of the interferogram makes available both the location of the dome, (x_d,y_d), and the radius of curvature of the dome, a_d. The radius of the mth bright ring is $r_m = \{[m - \phi/(2\pi)]\, a_d\, \lambda\}^{1/2}$ where λ is the

wavelength of the light in which the interferogram is made and ϕ measures the phase of the interferometer's reference plane. Thus, a plot of r_m^2 versus m gives a straight line with slope $s = \Delta(r_m^2)/\Delta m = a_d \lambda$ or

$$a_d = s / \lambda = (1 / \lambda)\ [\Delta(r_m^2)/\Delta m]$$

We do not need the value of ϕ, or the location of the interferometer's reference plane, to determine a_d. Some interferometers are equipped with software to determine a_d directly; then, there is no need for a plot.

Extending the (x,y)-coordinate system of the domed top of the fiber by adding a z-axis parallel to the fiber's axis, the equation of the domed surface is

$$(x-x_d)^2 + (y-y_d)^2 + (z-z_d)^2 = a_d^2$$

where z_d is the location of the center of the spherical surface; the center of the sphere is at the radius a_d below the crown. The angle Φ between the fiber's center line and the center of the sphere is

$$\Phi = \arcsin\{[(x-x_d)^2 + (y-y_d)^2]^{1/2} / a_d\} \text{ approx } [(x-x_d)^2 + (y-y_d)^2]^{1/2} / a_d$$

where the approximation is essentially exact for the typical practice in which the radius of curvature a_d of the domed end of the fiber is much larger than the crown's off-set distance $[(x-x_d)^2 + (y-y_d)^2]^{1/2}$, since the angle Φ is then much smaller than unity. Under such typical practice, we can safely resolve this angle into cartesian components,

$$\Phi_x = x_d / a_d, \qquad \Phi_y = y_d / a_d$$

When we see such an off-set, we adjust the fixture presenting the fiber to the end-finisher by the angles (Φ_x, Φ_y) and polish again. Upon re-inspection by the interferometer, we expect the new location of the crown to be (0,0). In practice, we can suppose that various effects (including elasticity, hysteresis, and stiction) may prevent us from obtaining exactly this condition; but we can also suppose that we will be substantially closer to the desired condition.

A POSSIBLE FIXTURE

One way to construct a fixture that would allow straightforward adjustment of the angles Φ_x and Φ_y to quickly bring the crown of the dome into alignment with the fiber's axis has been described to me by John Kolasinski (Code 565 of Goddard Space Flight Center).

We suppose the fixture pivots at a fixed point, and is pressed against set-screws at two other locations, per Figure 3.

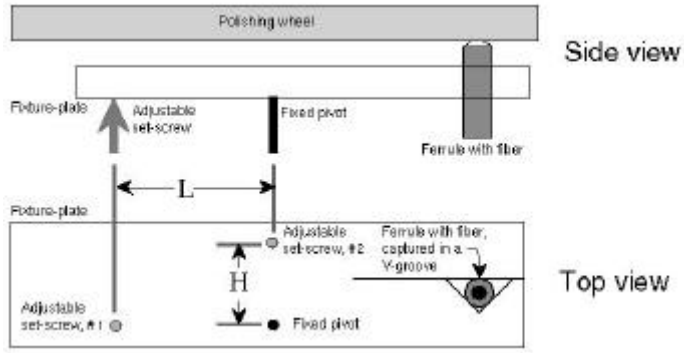

Figure 3: Fixture Drawing.
Top and side views of a possible fixture. The ferrule (containing the fiber) is captured in a V-groove in a plate. The plate is supported at one fixed point and at two set-screws, separated by *H* and *L* from the fixed point.

We ignore any elastic or plastic deformations, and suppose the simplest possible geometrical relations among the motions. We suppose that the changes in the angles about the two axes of the main split-plate are imposed precisely on the angles the fiber's axis makes with the polishing disk. The assembly holding the set-screws and fixed point (this assembly is not shown in Figure 3) is arranged to move in a friction-free manner parallel with the fiber's axis, and is dead-weight loaded. Thus, it causes the fiber to be pressed against the polishing disk with a force set by the load, independent of adjustments of the set-screws.

We suppose the x-axis in the interferogram is aligned with the long axis of the split-plate, and the y-axis is aligned with the short axis; i.e., with L and with H, respectively. The advance z_1 of the set-screw #1 is given by the product of its pitch P_1 (in inches per turn, say) and the fraction F_1 of the turn that it is rotated; thus, $z_1 = P_1 F_1$. And the same, with appropriate subscript changes, for set-screw #2.

These choices of meaning for P_1 and F_1 merit discussion:

Webster's dictionary defines *pitch* as ``the distance between any of various things,'' such as the distance

between any point on the thread of a screw to the corresponding point on an adjacent thread, measured parallel to the axis. But Webster's then defines *pitch* as the ``number of threads per inch." These two meanings are inversely related.

The *Machinery's Handbook: A Reference Book for the Mechanical Engineer, Draftsman, Toolmaker and Machinist* (1980: 21st edition, third printing. Industrial Press, Inc.) speaks to this on page 1383:

- pitch is the distance from the center of one screw thread to the center of the next one. The word ``pitch' is often, though improperly, used to denote *the number of threads per inch*. For example, a screw is spoken of as having a 12-pitch thread, when twelve threads per inch is what is really meant. The number of threads per inch is the inverse of the pitch: 1/pitch.
- lead is the distance the nut will travel forward along the screw when it is rotated once.

In a single-threaded screw, the pitch and the lead are identical; in a double-threaded screw, the lead is twice the pitch, and so on.

The fraction of a turn F is a dimensionless number ranging from 0 (no rotation) to 1 (a single rotation, corresponding to 360° or 2π radians); larger values correspond to additional rotations. Negative values correspond to rotations in the opposite sense.

Then

$$\Phi_x = z_1 / L = P_1 F_1 / L$$

$$\Phi_y = z_2 / H = P_2 F_2 / H$$

or

$$F_1 = (L / P_1)\,\Phi_x = (L / P_1)\,(x_d / a_d)$$

$$F_2 = (H / P_2)\,\Phi_y = (H / P_2)\,(y_d / a_d)$$

The last part of these two equations give the required fraction of the turn of each of the two set-screws in terms of the quantities measured using the interferogram, and the parameters built into the fixture.

Now it is time for a test of this result. This will give the best check on the importance of the ignored effects, such as elasticity, plasticity, and stiction.

Programmable Logic Application Notes

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This column will be provided each quarter as a source for reliability, radiation results, NASA capabilities, and other information on programmable logic devices and related applications. This quarter's column will include some design application notes and some recent radiation test results and evaluations of interest. Specifically, the following topics will be covered: VHDL coding styles, two techniques for SEU-hardening flip-flops using CAE tools, total dose qualification of the RH1020, initial electric and radiation evaluation of the QuickLogic pASIC 3 QL3025 FPGA, RH1020 Single Event Upset Report with a discussion of "clock upset," electrical and additional radiation characterization of the RT54SX16, and a summary of antifuse hardness data. Note that additional information on some of the topics discussed here are available at http://rk.gsfc.nasa.gov

VHDL Coding Style in ACTmap

As we move to a higher percentage of design using VHDL, it is important to understand the effects of VHDL on design efficiency and device performance. A number of tests using different coding styles have been run. Obviously, the style that allows ACTmap to recognize standard structures and call ACTgen for macro generation are very efficient, with some control over area-speed trade-offs available. However, it has been shown that certain compact flexible styles will produce lower quality netlists. In particular, the use of the for-loop construct in certain instances, such as computing the XOR of all the bits in a vector, will produce inferior results to having code that 'unrolls' the loop which in turn is inferior to the netlist produced by ACTgen. The code below shows an example of the two coding styles. More complex cases have shown, in some instances, similar results with a factor of 1.5 - 2 observed in both size and speed for identical functions coded in different styles.

For an example, a 9-bit XOR function was synthesized three ways, targeted to Act3 libraries. Using

ACTgen, 8 modules were used and the circuit had a delay of 3 gate delays. ACTmap was then used to synthesize the circuit using the for-loop construct using 19 modules and having 5 gate delays as shown below.

```
XorP: Process (X) -- 9 Element Vector
      Variable t: Std_Logic;
      Begin
        t:= '0';
        For i In (X'Length-1) DownTo 0 Loop
            t:= t Xor X(i);
            End Loop;
        Y <= t;
      End Process XorP;
```

The following VHDL code, which is more 'clumsy', had improved performance using 8 modules and 4 gate delays. Analysis of the output using Viewgen showed that a typical XOR tree was constructed using 2-input XOR gates which did not exploit the Act3 modules functionality which ACTgen did. Schematics are available on the www.

```
XorP: Process (X)
      Begin
        Y <= X(8) Xor X(7) Xor X(6) Xor
             X(5) Xor X(4) Xor X(3) Xor
             X(2) Xor X(1) Xor X(0);
      End Process XorP;
```

Flip-Flops for the Radiation Environment

In the last edition, we referenced an application note on how to use Synopsis to control flip-flop synthesis for either C-Module or TMR structures to improve the SEU-immunity over the hard-wired flip-flops present in the Actel architecture (except Act1). Here, two additional methodologies are presented.

"Hardening Flip-Flops for Actel FPGAs for schematic, macro, and HDL Design,"

Recently we've designed a library with C-Module substitutes for all S-Module flip-flops and latches with hooks are in for TMR. These libraries can be used in several ways. One, they can be used as a standard macro library and one can pick from the list. This is handy for schematic-based design and permits use of 'standard' macro definitions. For Actgen or VHDL-based designs, we have written a utility to automatically make substitute C-Module replacements for all S-Module flip-flops and latches. This can be done globally or on a case by case basis. This program and the macro library is for Viewlogic systems and it automates what one can do by hand. It should easily be ported to Orcad or other systems. Note that Viewgen will create a valid schematic file from Actgen or VHDL generated netlists permitting use of standard tools such as Actmap and post-processing the netlists.

Synplicity

Synplicity is now supporting either C-Module or TMR-generation and an application note has been written titled "Using Synplicity to Control Flip-Flop Implementation for SEU-Hardness" with the full application note available at http://rkgsfc.nasa.gov/richcontent/Software_Content/SynplicitySEUControl.htm. The following excerpt provides some comments and shows the procedure for generating C-Module flip-flops.

The following procedure, supplied by Synplicity, gives a procedure to synthesize code for "SEU-Hardness" and is geared for the Act2 devices. Either C-Mod flip-flops can be generated or TMR-triplets can be generated. In the case of the TMR triplets, 3 C-Mod flip-flops are used and one C-Mode voter for 7 modules per bit. Note that Synplicity's use of the term "rad hard" for flip-flops designates a C-Mod flip-flop implementation which would properly be classified as "rad-tolerant." Note also that there is memory (two latches) in each I/O module of Act2 devices. For the A1280A and RH 1280, these are considered to be rad-tolerant and that the TMR technique described here do not apply to the I/O modules. The files that Synplicity provides are user-customizable for different solutions.

<u>Actel RadHard (RH 1280) Usage</u>

There are certain cells in Actels ACT2 library which are RadHard. RadHard (Radiation Hardened) devices are required for many military and space applications. This technical tip will describe how to utilize the RadHard features of Actel and Synplify.

How to Use Synplify 3.0b with Actels RadHard Devices RadHard cells are not used by default. To make your design RadHard [rad-tolerant w/ C-Mod flip-flops] using Synplify 3.0b, follow the procedure be-

low. The procedure described is for a Verilog design. If you are using a VHDL design please read the info contained within the parenthesis ( ).

1. When compiling the design, first include the synplicity/lib/actel/act2.v(act2.vhd) file in the Synplify project window. This file contains the black_box declarations of the RADHARD cells.
2. Add the synplicity/lib/actel/radhard_act2.v(radhard_act2.vhd) as the second file in the Synplify project window. This file has information to substitute the sequential cells (non-radhard cells) with the radhard cells.
3. Add your design file as the third file in the Synplify project window and click on the RUN button.

The default cells used by Synplify will be the RADHARD cells.

TOTAL DOSE QUALIFICATION OF THE RH 1020

The following are excerpts from the qualification report of the RH 1020 (courtesy of Lockheed-Martin). Note that the total dose qualification report was done on a 96Å ONO antifuse thickness; some production lots have different antifuse thicknesses. The antifuse rupture data, presented later in this column, shows some additional data. For the full report, please see: http://rkf.gsfc.nasa.gov/richcontent/fpga_content/rh1020_tid.PDF

Summary

- **Part Type:** RH 1020 Field-Programmable Gate Array (FPGA), Si, CMOS, monolithic, device type #197A805, 2000 gates.
- **Part Process:** RH CMOS-4EF (L_{EFF} = 0.8 µm; V_{DD} = +5.0V; 96Å ONO).
- **Samples Tested:** Five (5) plus one (1) "control."
- **Test Lot:** T7012E.1; Manufacturing Lots #96509A.1 & #96509B.1.
- **Test Facility:** Lockheed Martin Federal Systems - Manassas (LMFS-M) J.L. Shepherd Model 109-68 (S/N 3028) gamma source.
- **Dose Levels:** 200 krads(Si), 300 krads(Si), and 600 krads(Si).
- **Dose Rate:** 125.3 rads(Si)/s.
- **Test Date:** 17 September 1997.
- **Bias Conditions:** +5.0 Vdc (exposures); +4.50 V, +4.75 V, +5.00 V, +5.25 V, and +5.50 V (measurements); and +5.5 V (anneal).
- **Test Pattern:** *ALPHA-11* with "Binning Circuit"
- **Temperatures:** ~+28 °C (exposures); +25 °C measurements; +125 °C (168-hour anneal).
- **Test Method:** Radiation-tested per MIL-STD-883E, Method 1019.4. The **D**evice **U**nder **T**est (DUT) was exposed while powered, & measured on the *ADVANTEST* logic tester. DUT's parameters and functionality measured before radiation, after each exposure, and again after 168 hours of a high-temperature (+125 °C) anneal while on bias.

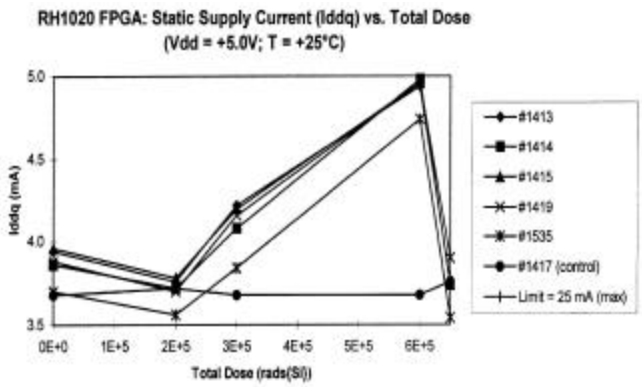


Figure 1A. Static Supply Current vs. Total Dose. The final data points are after the 168-hour high temperature anneal

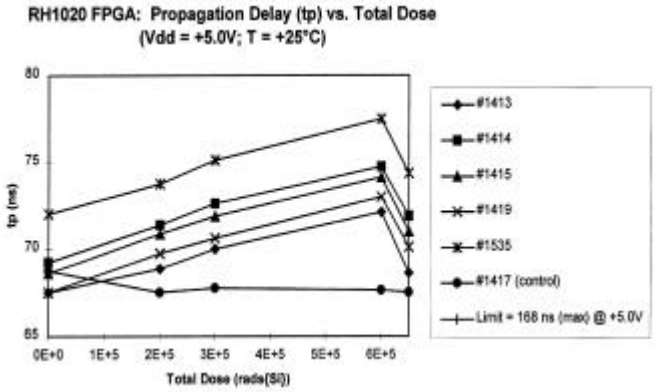
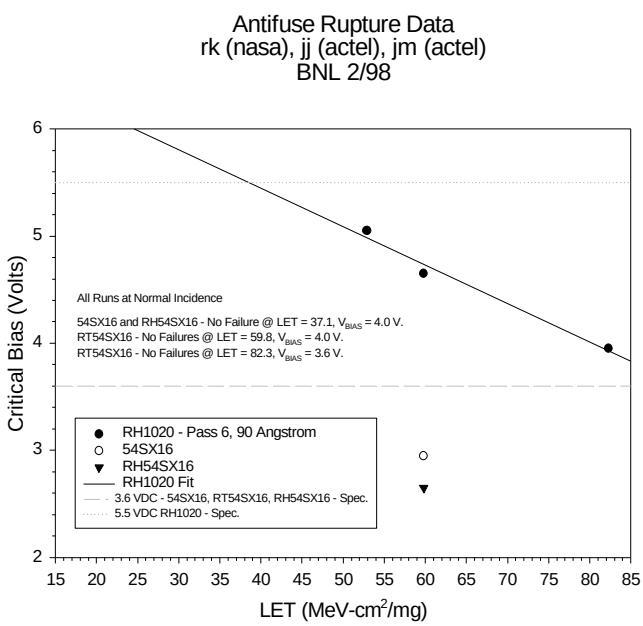
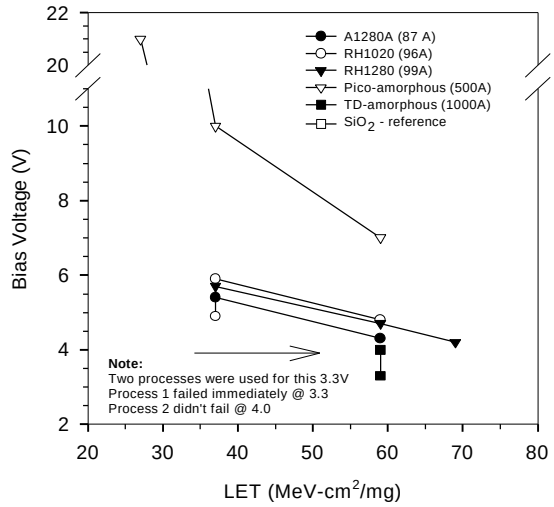


Figure 2B. Propagation Delay vs. Total Dose for the Binning Circuit. The final data points are after the 168-hour high-temperature anneal

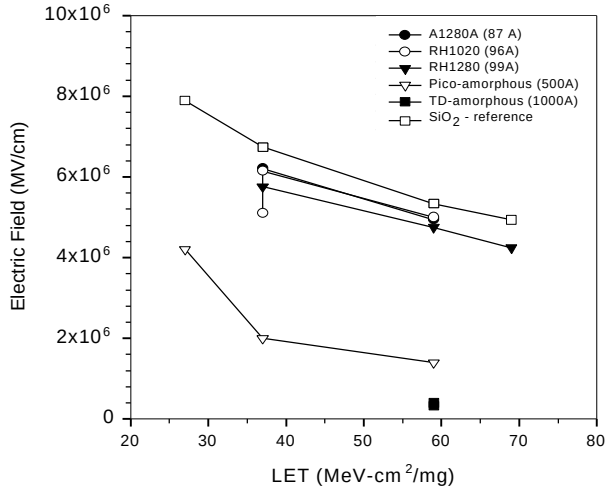
ANTIFUSE HARDNESS DATA

Antifuses have been shown to be hard to total dose effects, [see http://rk.gsfc.nasa.gov/richcontent/papers/radpal_antifuse.PDF for a recent example on amorphous silicon antifuses]. A summary of recent heavy ion data is shown in the three charts below. The first, from February, 1998, shows the performance of the production RH 1020 with 90Å ONO antifuses, used for this lot. Also shown are prototype SX series devices, employing different "recipes" of metal to metal antifuses. These early tests confirm the data from July, 1998, shown above, with no breakdown at LET = 60 MeV-cm²/mg, with the test range successfully extended to an LET of 82.3 MeV-cm²/mg. Different antifuse formulations, based on materials and thickness, showed differing SEE hardness. For the RH 1020, a linear relationship between critical electric field strength was observed, consistent with the earlier results; data points at an LET of 37 MeV-cm²/mg will be taken in June, 1998. Data on the UT22VP10 amorphous silicon antifuse PAL is still being evaluated.





Antifuse Breakdown Voltage vs. LET (MeV-cm²/mg). Devices fall into one of three classes, 12 V mixed-signal, 5 V digital, and 3.3 V digital. Only one device showed positive margin up to an LET of 60 MeV-cm²/mg.



Antifuse Breakdown E-Field Strength vs. LET (MeV-cm²/mg). The thicker amorphous silicon antifuses ruptured at low electric field strengths

INITIAL EVALUATION OF THE QUICK LOGIC PASIC 3 QL3025 AMORPHOUS SILICON ANTIFUSE FPGA

Electrical Characteristics

The QL3025 is built on a 4-layer metal, 0.35 µm bulk process. As such, the core runs on 3.3 volts, configured in a sea-of-modules architecture. This voltage results in reduced power consumption since the power is a function of the square of the voltage. This architecture does make some provision for interfacing with standard 5 volt logic for most applications. This

is achieved by allowing the system board to provide a 5V reference coupled with TTL-level input voltage thresholds. For pure 3.3 volt systems, the entire device may be run at V_{CC} = 3.3 volts. This configuration allows the inputs to interface with either TTL-level outputs or rail-to-rail switching CMOS outputs.

Device outputs, however, like many 3.3 volt devices, require careful application. It is noted from the specifications and the oscilloscope photos below that the outputs switch between 0 and 3.3 volts, even when the device is configured for 5 volt systems as our test board was. This permits direct connection to either other 3.3 volt devices or 5 volt devices with TTL-level thresholds. Typical 5 volt CMOS devices will not be reliably driven since their worst-case logic '1' threshold (with some exceptions) is 70% of the supply voltage or nominally 3.5 volts. Clearly, there is insufficient margin.

Another consideration when using modern devices of this type is signal quality. The two photos shown here, for rising and falling outputs of the QL3025, have sub-nanosecond transition times. This data was obtained with a 2.0 GigaSample/sec digital oscilloscope and active FET probes with a bandwidth of 800 MHz; the observed waveforms may be test equipment limited. Obviously, line lengths and terminations need careful consideration.

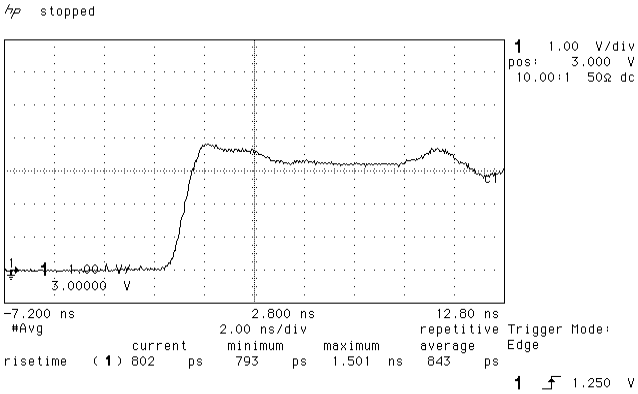


Figure 1: Sample Rise Time Characteristic of the QL3025 at Nominal Supply Voltages

The following power numbers were obtained from our test sample. For these measurements, we used the two shift registers with the rest of the chip re-

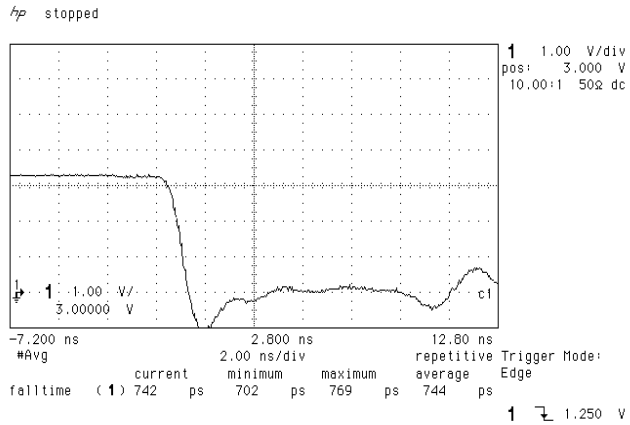


Figure 2: Sample Fall Time Characteristic of the QL3025 at Nominal Supply Voltages

maining static. Each shift register is 200 bits long with one of the two consisting of TMR-triplets along with voter circuits and error detection circuits for counting upsets that are rejected by the voter in heavy ion radiation tests. The device was tested in three modes:

1) Static;
2) Clock Distribution Network;
3) Active.

The static mode was measured with all inputs at either V_{CC} or GND; the clock distribution measurement utilized the hard macro distributing both positive and negative clocks, and the active mode had all flip-flops toggling at 500 kHz with the clock input at 1 MHz. For all tests, currents on the 5.0 VDC supply were essentially 0, registering only 210 µA on the active test and 0 elsewhere. The core 3.3 VDC supply measured 500 µA static, 1.6 mA distributing the 1 MHz clock, and 5.4 mA for the active mode.

Antifuse leakage current is an important parameter and below is some of our first temperature data on a metal-to-metal amorphous silicon FPGA. We tested several temperature cycles over the full military temperature range, (-55 °C to +125 °C) with temperature transitions of 1 °C/minute. Figure 3 shows part of our strip charts while Figure 4 shows an $I_{CCSTDBY}$ vs. Temperature curve.

Several key results are shown by these curves. First, operation of this device over the full military temperature range will consume approximately 3 µWatts which is clearly acceptable. Secondly, it is clear that the current has an exponential rise with temperature.

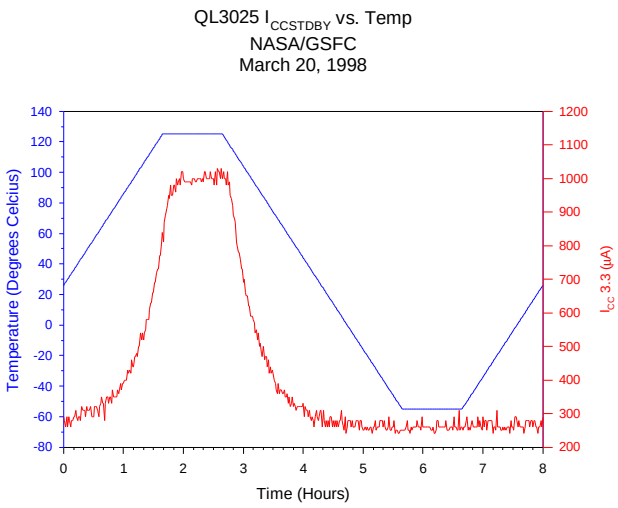


Figure 3: $I_{CC3.3}$ and Temperature Strip Chart for a Sample QL3025 pASIC 3 FPGA with Amorphous Silicon Antifuses

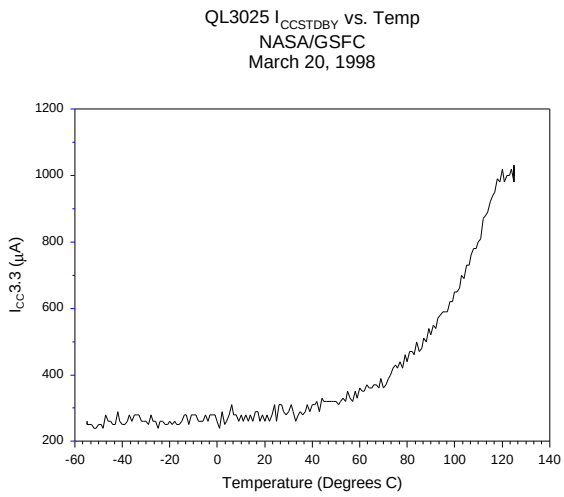


Figure 4: $I_{CC3.3}$ vs. Temperature for a QL3025 pASIC 3 FPGA with Amorphous Silicon Antifuses Showing An Exponential Relationship.

Single Event Effects

Three test devices were prepared for the February, 1998, heavy ion test at Brookhaven National Laboratory. The portions of the evaluation pattern relevant to this device were three shift registers. Two 200 element shift registers were in the device's core with one of the two being TMR-hardened with error monitoring circuits, making a total of 800 flip-flops. The third shift register was 25 elements long and was constructed in the I/O-modules.

Testing started with Titanium (Ti), which had an LET of 18.8 MeV-cm^2/mg and the device had nominal voltages applied (5.0 and 3.3 VDC). Both devices latched during each run, with S/N 001 damaged after 6 runs and S/N 002 damaged after 5. S/N 001, after damage, had 137 mA excess current and was functional; S/N 002 had 100 mA excess current and failed functional testing.

Interestingly, each of the device's supplies latched. Table 1 has a summary of some typical runs. Based on all of the runs, the rough estimate for device latchup cross-section is 2.7x10^{-5} cm^2/device. Testing was stopped after the two devices were damaged.

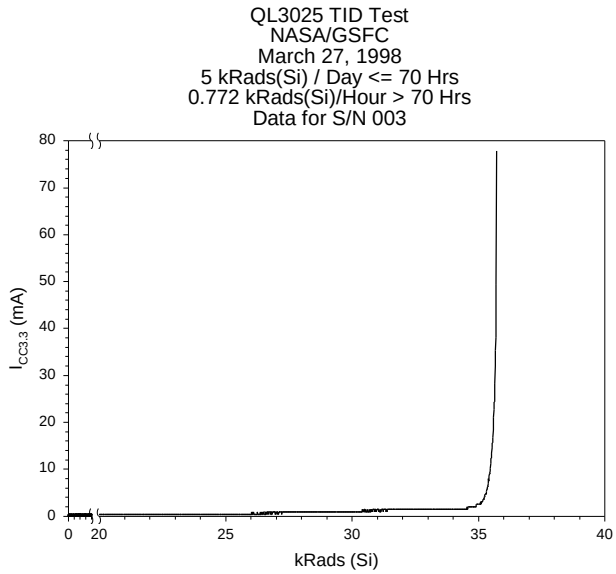
Another interesting result is that for this 0.35 µm, 3.3 VDC device, no upsets were seen in either the core or the I/O flip-flops.

Table: Summary of Some QL3025 Heavy Ion Latchups

Run Number	Fluence (ions/cm^2) (approximation)	5V Latch Current (mA)	3.3 V Latch Current (mA)
QL1T1	2.4E4		82
QL1T2	1.6E4	420	
QL1T3	2.8E4	200	380
QL1T4	2.0E4		220
QL2T1	4.7E4		165
QL2T2	2.1E4	400, >400 (2nd latch)	
QL2T3	5.6E3		170
QL2T4	1.7E4		170
QL2T5		430	170

Total Dose Effects

An initial TID test was run on the QL3025 S/N 003 device, with the results shown below.



After irradiation, the device passed functional tests and the currents on the 3.3 volts supply quickly dropped: The 3.3 VDC supply measured 19 mA static, 3.1 and 3.4 mA distributing the 1 MHz clock, with differences for loading 1's and 0's, and 8.5 mA for the active mode.

RH1020 SINGLE EVENT UPSET SUMMARY REPORT

Richard B. Katz / NASA GSFC
J. J. Wang / Actel Corp.

Prepared: March 5, 1998

1.0 BACKGROUND AND SUMMARY

This report summarizes the testing and analysis of "single event clock upset" in the RH1020. Also included are SEU-rate predictions and design recommendations for risk analysis and reduction.

The subject of "upsets" in the RH1020 is best understood by using a model consisting of a global clock buffer and a D-type flip-flop as the basic memory unit. The RH1020 is built on the ACT 1 family architecture. As such, it has one low-skew global clock buffer with a TTL-level input threshold that is accessed via a single dedicated pin. The clock signal is driven to full CMOS levels, buffered, and sent to individual row buffers with one buffer per channel. For low-skew performance, the outputs of all of the

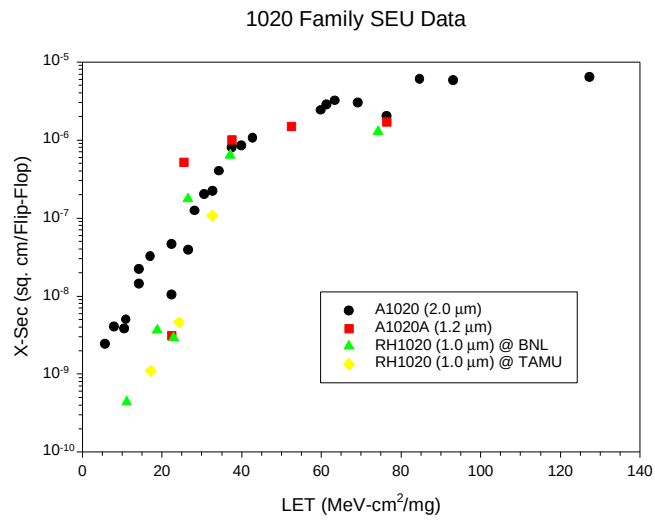


Figure 1. C-module SEU results of A1020, A1020A and RH1020

RH1020 row buffers are shorted together via metal lines. All storage in the RH1020 consists of *routed* flip-flops, constructed with multiplexors and feedback through the routing segments. A simple latch can be constructed from a single (combinatorial or C) module; an edge-triggered flip-flop is constructed using two concatenated latches. There is no storage in the I/O modules.

The front end of the clock buffering circuitry, at a common point relative to the row buffer, is a sub-circuit that was determined to be the most susceptible to heavy ions. This is due, in part, to its smaller transistors compared to the rest of the circuitry. This conclusion is also supported by SPICE simulations and an analysis of the heavy ion data, described in this report.

The edge triggered D flip-flop has two single-event-upset modes. Mode one, called C-module upset, is caused by a heavy ion striking the C-module's sensitive area on the silicon and produces a soft single bit error at the output of the flip-flop. Mode two, called clock upset, is caused by a heavy ion strike on the clock buffer, generating a runt pulse interpreted as a false clock signal and consequently producing errors at the flip-flop outputs. As shown in Figure 1, C-module upset sensitivity in the RH1020 is essentially the same as that of its ACT 1 siblings (A1020, A1020A and A1020B), which were well tested, analyzed, and documented in the literature.

RH1020 clock upset has not yet been detected directly by measuring a heavy ion induced pulse. Transmission of the clock signal via clock network interface hard

macros, routing to an output module, and driving the signal off-chip can tend to act as a low-pass filter. A more sensitive "detector" are flip-flops constructed on the die, directly hooked to the global clock network.

Detection and analysis relies on carefully designed test patterns and equipment to decompose the total number of flip-flop upsets into a C-module upset component and a clock upset component. Although in reality only the total upsets count, the separation is necessary because they have different frequency dependence and system effects. To a first approximation, the clock upset rate has a strong, linear dependence on clock frequency. The C-module upset rate is frequency independent (for all practically used frequencies). Since most applications use a clock frequency different from the SEU testing frequency, only the clock upset component has to be scaled to get an accurate rate prediction.

Conclusions from the test data indicate that a heavy ion hitting on the clock buffer will induce "clock upsets" mainly when the clock signal is transitioning. A plausible scenario is the generation of a runt pulse on the positive going transition of the clock (with respect to the device pin). This can be interpreted by the flip-flops as two clocks or "double clocking," as shown in Figure 2. The system affect is similar to other familiar problems, such as ground bounce induced problems (see, for example, "High-Speed Digital Design: A Handbook of Black Magic", by H. Johnson and M. Graham, Prentice Hall, 1993, page 69).
Clock upset has been detected in some previous Act 1 de-

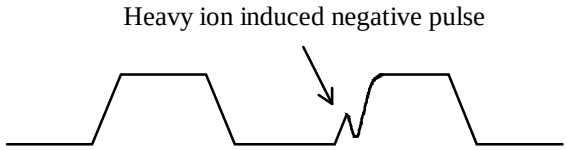


Figure 2. Double Clocking as a Result of Heavy Ion Induced Pulse

vices (see "Programmable Logic Application Notes," EEE LINKS, published by NASA/GSFC). RH1020 clock upset was initially found during QML SEU testing. It was then thoroughly investigated by heavy ion tests (four accelerator trips), laser stimulation, circuit simulation, and laboratory electrical evaluation. The most sensitive nodes were determined to be in the clock buffer. Heavy ion tests were performed, under identical conditions, on samples of all models of the A1020 series devices, confirming the earlier preliminary detection of clock upset susceptibility.

Changes to the clock buffer circuitry to reduce the sensitivity to heavy ion upsets were done without negatively affecting the product characteristics or die size. SEU testing was performed on five (5) production parts with the new design changes. The clock upset data was extracted and is presented in this summary report. We found more than an order of magnitude reduction of clock upset due to the changes made, resulting in clock upset rates being an order of magnitude smaller than one C-module flip-flop. Thus, the clock upset is minor when compared to the C-module upset for most applications. Nevertheless, for an RH1020 user to evaluate specific applications independently, we provide detailed data and methodology in this report to support the effort.

2.0 SEU TESTING AND RATE PREDICTION

2.1 Test Set Overview

The SEE test set consists of two sections, one set of equipment outside of the vacuum chamber and a DUT card mounted inside of the chamber. All power supplies are configured for remote sensing, ensuring accurate voltage settings at the DUT for all conditions. All I/O to and from the chamber is transmitted over RS-422 differential drivers and receivers, providing good noise immunity and reliable signal transmission. A 2X clock is sent to the DUT card, as are level commands. The DUT card sends back either raw data (in test mode) or error pulses.

A laboratory computer controls the test and records the data. The PC is equipped with an HP-IB interface card for computer control of the HP6629A system power supply. Also embedded in the PC is a custom RS-422 board, providing level commands, a programmable frequency clock (via an external pulse generator or crystal oscillator selection), and ten (10) 16-bit event counters.

Test control is provided through a WFI interface with real-time error counter display. Strip charts can be made of either device currents or error counters. For the clock upset tests, each mismatch triggered the recording and time tagging of the counters. Sampling was at approximately 4 kHz.

The DUT card is a multi-layer PCB with all signals transmitted and received via RS-422 buffers. The 2X clock is divided down to a nominal 1 MHz by an on-board FPGA (A1020A). All pattern generation, DUT stimulation, and error-checking/error-pulse-generation is also performed by the FPGA.

2.2 DUT (DEVICE UNDER TEST) DESIGN AND CONFIGURATION

The test pattern used for the majority of tests was the TMRA1BRB pattern, previously used on A1020, A1020A, and A1020B devices. For clock upset testing, a subset of the device's capabilities was used. Specifically, two 34-bit shift registers were used. One consisting of simple flip-flops and the other was a TMR-hardened (triple modular redundancy) string. Error monitoring circuitry is provided to count all upsets rejected by the error-correction circuitry. All flip-flops are constructed without any asynchronous preset or clear functions. This eliminates upsets on other portions of the die as a possible cause of device error.

The RH1020 is packaged in an 84-pin ceramic quad flat pack, surface-mounted to an adapter board. This multi-layer adapter includes power and ground planes, short lead lengths and is compatible with the A1460PGA207 socket on our test board. This configuration gives a good quality, realistic environment for the RH1020 and removes restrictions on beam angle to the device, a problem with the Wells ZIF socket normally used. Ground bounce and V_{CC} spikes, measured at the RH1020 pins, was minimal and comparable to typical well-built systems. The clock was driven to full CMOS levels by an A1020A. The relatively moderate output transition times of this device resulted in clock signals at the RH1020 which were clean and had minimal ringing.

The input logic pattern to the shift registers was nominally a checkerboard pattern, (i.e. an alternating '0' and '1' pattern at ½ of the clock rate). Other patterns such as all '1's, all '0's, or twisted ring counters would mask the effects of clock upsets since the output signature would be difficult or impossible to distinguish from "normal" C-module upsets. The TMR string makes the D-latch part of the shift register practically immune to SEU, eliminating the upset component of the C-modules.

2.3 CLOCK UPSET DETECTION

A runt clock pulse or "double-clocking" by one heavy ion hitting a sensitive clock node will shift the internal flip-flops and the resultant output logic pattern out of phase by one state for all flip-flops affected. A "full" extra pulse will result in all flip-flops receiving a clock pulse, with all flip-flops holding '0's changing to '1's and vice versa. Checking circuitry, external to the RH1020, would then flag 34 errors on each string as a burst. In practice, at device operating voltages of 4.5 VDC < V_{CC} < 5.5 VDC, we normally saw error bursts of approximately 17 errors on each of the two shift register strings *simultaneously*, including the TMR-hardened string. Typically, zero or only a single error would be reported on the TMR error monitor indicating that all flip-flops in the same region of the chip reacted identically to a runt pulse.

To accomplish testing in reasonable times, most runs had ion fluxes of 10^5 ions/cm^2/sec and a fluence of 10^7

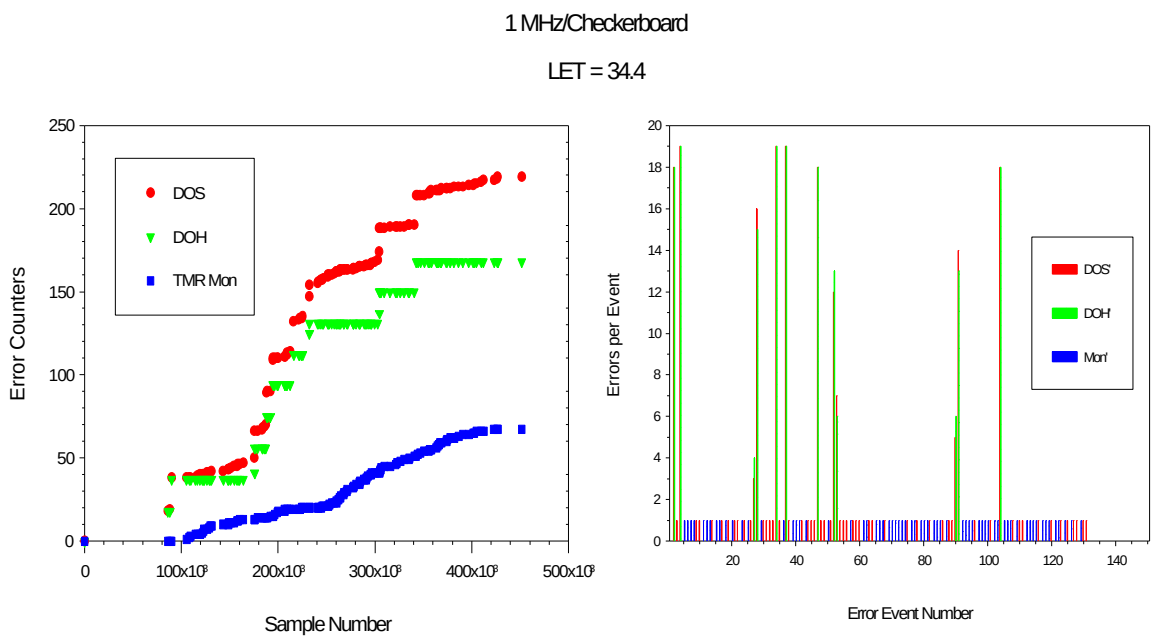


Figure 3: Typical Data Showing Cumulative and Differential Error Counts

ions/cm^2. While an estimate count could be made by watching the error counters, accurate clock upset and SEUs could be counted by our test equipment. To detect clock upset, our three error counters were monitored by the test computer at approximately 4 kHz. Any change to any of the counters resulted in each of the three counters being recorded and time stamped. By examining the change of error counts with respect to time, clock upset and all other mode of SEU are relatively easily separated and counted, even for high LET runs with a lot of upsets. Some typical data is presented in Figure 3.

2.4 TEST FACILITIES AND CONDITIONS

Most of the testing was performed at Brookhaven National Laboratory using the SEU facility in the Tandem Van de Graaff building. Other facilities included the cyclotron at Texas A&M and the pulsed laser facility at the Naval Research Laboratory. Electrical testing was performed at both the Actel Corporation and the NASA Goddard Space Flight Center. Typically, clock upsets were measured at 5 volts bias, 1 MHz clock frequency and room temperature with ion fluxes of 10^5 ions/cm^2/sec and a fluence of 10^7 ions/cm^2. The nominal V_{CC} was used over the full range of LET. The voltage dependence of clock upset is too weak to establish the worst-case V_{CC} to be 4.5 volts or 5.5 volts. Additionally, several low-flux runs were conducted, with no major dependence on flux observed.

2.5 DATA AND RATE PREDICTION

Figure 4 shows the clock SEU cross section versus LET data plot of five (5) tested devices, P6-1 to P6-5. For a sample calculation, the median data are used to fit a Weibull curve by using HITFIT utilities in Space Radiation simulator. The resulting Weibull parameters (Table 1) together with typical orbital, environmental and shielding parameters of a satellite on the geosynchronous orbit (Table 2) is then input to the heavy ions rates prediction module of the Space Radiation simulator. The result of the upset rate prediction is **3 x 10^{-8} upsets/device-day**. For comparison, the C-module upset rate in the same conditions is approximately 1 x 10^{-7} upsets/bit-day.

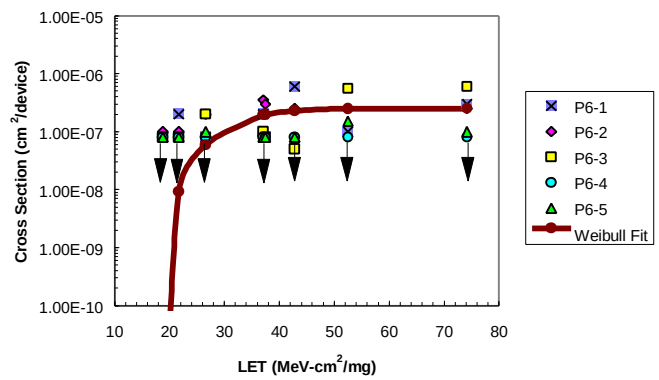


Figure 4 Clock SEU results

For a sample mission consisting of 10 RH 1020s for a duration of 10 years, the error rate is calculated to be:

3 x 10^{-8} clock upsets/device-day x 10 devices/system x 10 years/mission

or

1 upset per thousand missions per system.

Table 1 Weibull parameters

Cross Section	2.5 x 10^{-7} cm^{-2}/device
LET Threshold	18.8 MeV-cm^2/mg
Weibull Width	15 MeV-cm^2/mg
Weibull Shape	2

Table 2 Environment/shielding parameters

Orbit	36,000 km, 0°
Spacecraft Shielding	100 mil Al
Earth Shadowing	Yes
Magnetic Weather	Stormy
Solar Cycle	Solar Min (1975, M=1)

The frequency dependence of clock upset was measured using devices before the design changes were made to the clock buffer (After design changes, the upset counts are too low to make such measurements practical). Figure 5 shows the number of clock upsets versus the clock frequency of data from four parts for a fixed fluence measured at clock frequencies of 1 kHz, 10 kHz, 100 kHz and 1 MHz. LET of 37.1 to 74.2 MeV-cm^2/mg and a V_{CC} = 5 VDC and 4.5 VDC were used. The data clearly shows upset increasing with clock frequency. To a first order approximation, the upset rate can be treat as linearly proportional to the clock frequency.

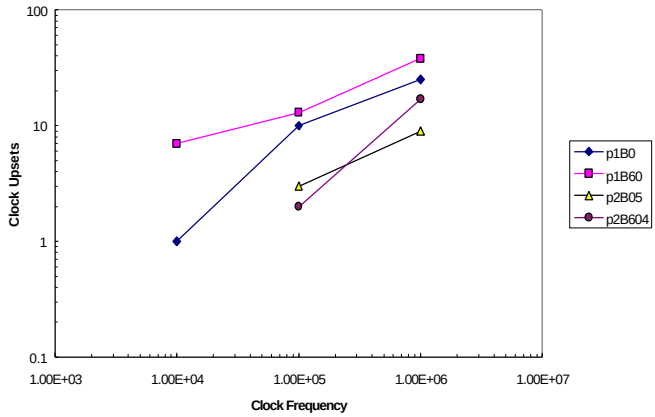


Figure 5 Frequency dependence of clock upset for a fixed fluence

3.0 DESIGN RECOMMENDATIONS

3.1 FREQUENCY DEPENDENCE

The total upset in the device and its impact at the system level is somewhat dependent on the details of the design and application. However, since we can calculate the clock upsets and C-module upsets independently, the total upsets can be calculated unambiguously. To scale the clock upset, the computed rate from the SEU testing data has to be divided by 1 MHz and then multiplied by the clock frequency of interest. For a typical geosynchronous application, if the clock frequency is ***f***, the clock upset rate is:

$$f \times \frac{3\times10^{-8}\,(\text{upset/device} - \text{day})}{1(\text{MHz})}$$

To minimize a susceptibility to the global clock upset, the clock should be run at as low a frequency as possible. For certain critical registers the system designer may want to use a separate clock which is held inactive except when updating the register's values. Based on available data and analysis, it is recommended to hold the clock high at the device's input pin.

3.2 REDUNDANCY DESIGN

If there is redundancy design for the clocked flip-flips, the redundancy should be designed across chips, if possible, similar to some memory EDAC architectures. It is preferred that redundant information not be stored in one single chip for the obvious reason that the global clock upset may simultaneously produce possible errors in all the clocked flip-flops. Separating redundant bits onto different chips may also decrease the number of single point failures (SPFs).

3.3 CLOCK UPSET TOLERANT DESIGN

For extremely critical applications, clock upsets may be dealt with at the circuit level. For example, three input pins can be used, with the generated clock being the output of a majority circuit. Using the conclusion that the circuit is more susceptible during the period of the rising edge, two clock input pins could be ANDed together, requiring both signals to go high to switch the AND gate. For either technique, note that the circuit outputs cannot access the global clock, since in the ACT 1 family the network is only accessible via the dedicated device input pin.

3.4 CLOCK UPSET AT SYSTEM LEVEL, DOES EVERYONE MEASURE CLOCK UPSET?

The RH 1020 is one of many device types, and similar questions about clock upset answered in this summary report should be asked for all digital devices in that system. Particularly important questions are: system flip-flop test methodology, flip-flop SEU rate frequency dependence, clock upset detection techniques, and separation of clock upsets and latch or flip-flop upset from the acquired datasets. Some "standard" testing techniques will not properly detect clock upset in devices. To date, the RH 1020 has been, we believe, the most thoroughly tested CMOS device for this phenomenon that is available for space-flight electronics.

CONTINUED EVALUATION OF THE RT54SX16

This section will present additional data on the RT54SX16. Recent data on antifuse radiation hardness can be found in antifuse hardness section above.

The voltage configuration and the outputs of the RT54SX16 are similar to the QL3025 described previously. Please reference that section for background information. The two charts below show some output waveforms for both rising and falling edges. Again we see 3.3 volt signal swings with extremely fast, sub-nanosecond transition times. These measurements were obtained with a 2 GigaSample / Second digital storage oscilloscope and an 800 MHz bandwidth active FET probe.

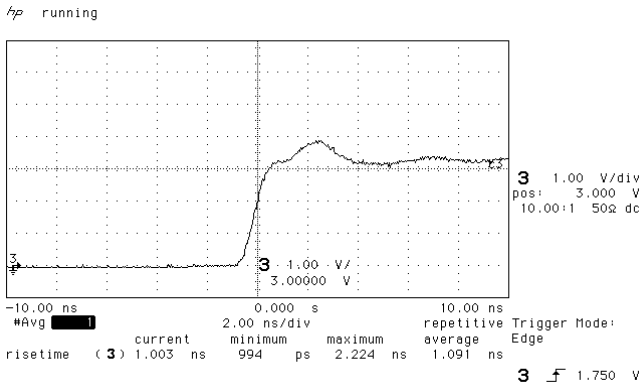


Figure 1: Sample Rise Time Characteristic of the RT54SX16 at Nominal Supply Voltages

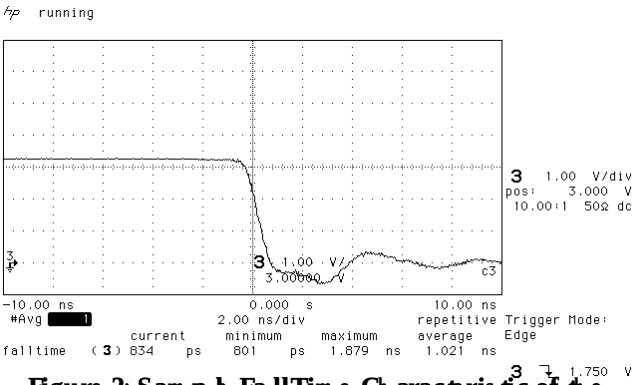


Figure 2: Sample Fall Time Characteristic of the RT54SX16 at Nominal Supply Voltages

Antifuse leakage current is an important parameter and below is some of our first temperature data on a metal-to-metal antifuse FPGA. We tested several temperature cycles over the full military temperature range (-55°C to +125°C) with temperature transitions of 1°C/minute. Figure 3 shows a part of our strip chart.

Several key results are shown by these curves. First, operation of this device over the full military temperature range will consume approximately 25 µWatts, clearly acceptable. Secondly, it is clear that the current has a linear relationship with temperature, in contrast with the QL3025 which had an exponential relationship. The slight increase in current at cold temperatures for the RT54SX16 was repeatable over several temperature cycles and profiles.

Dynamic power dissipation was also measured with results shown in Figure 4. As expected, the power consumption of the device was linear with respect to frequency.

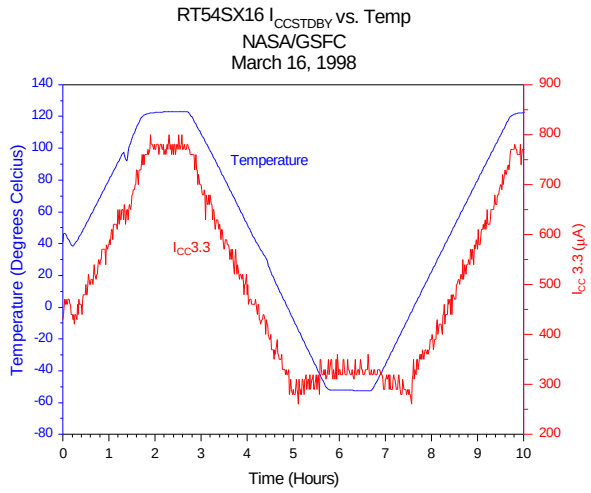


Figure 3: ICC3.3 and Temperature Strip Chart for a Sample RT54SX16 FPGA with a metal to metal Antifuse.

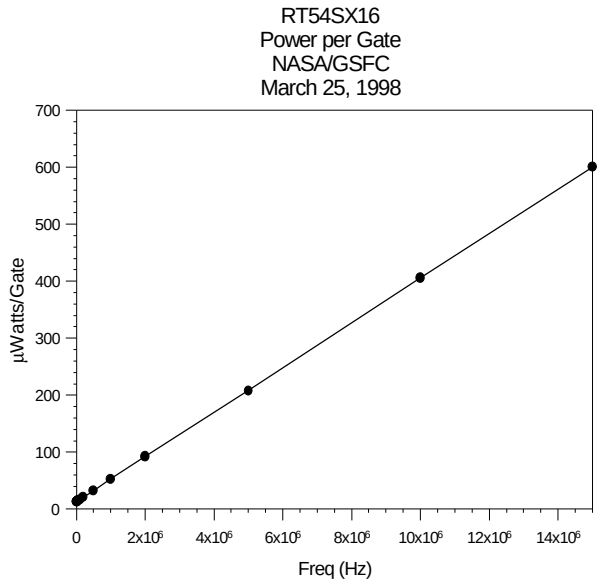


Figure 4: Power per Gate Characterization as a Function of Frequency for the RT54SX16

Additional total dose tests have been performed increasing our database and knowledge about these devices. Figures 5 and 6 below show the results. The devices were functional after exposure with the test being terminated as a result of facility availability.

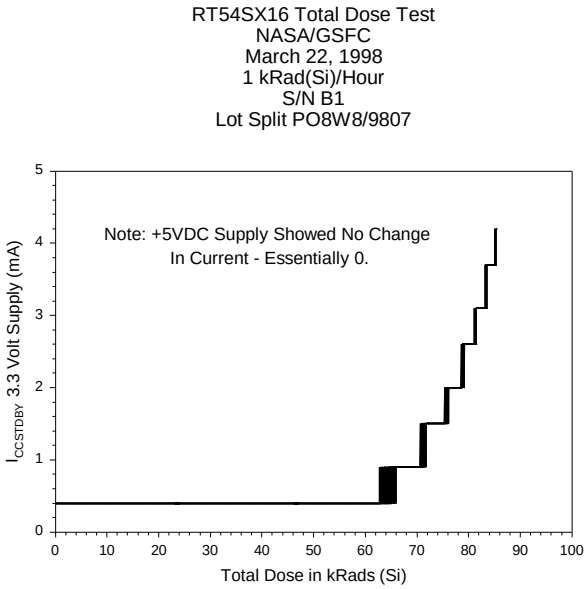


Figure 5.

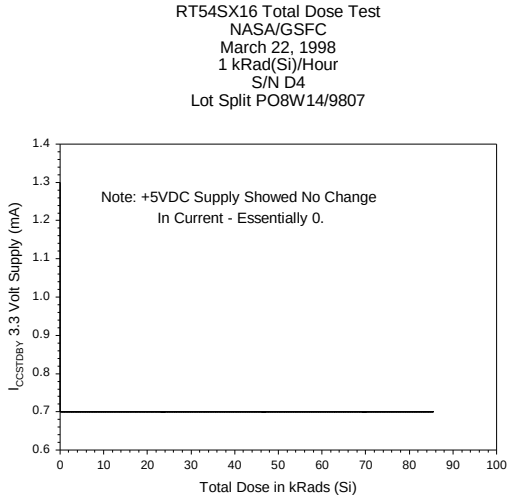


Figure 6.

Fiber Optic Cable Assemblies for Space Flight II: Thermal and Radiation Effects

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The following is being published and presented at the 1998 SPIE International Symposium on Optical Science, Engineering and Instrumentation in San Diego, at the Session on Photonics for Space Environments VI.

ABSTRACT

Goddard Space Flight Center is conducting a search for space flight worthy fiber optic cable assemblies that will benefit all projects at all of the NASA centers. This paper is number two in a series of papers being issued as a result of this task to define and qualify space grade fiber optic cable assemblies. Though to qualify and use a fiber optic cable in space requires treatment of the cable assembly as a system, it is very important to understand the design and behavior of its parts. This paper addresses that need, providing information on cable components shrinkage testing and radiation testing results from recent experiments at Goddard Space Flight Center. This work is an extension of the "lessons learned" reported in the first paper of this series entitled "Fiber Optic Cable Assemblies for Space Flight: Issues and Remedies," published and presented at the AIAA World Congress in Anaheim CA, on October 15, 1997

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12 Channel Optical Fiber Connector Assembly: From Commercial off the Shelf to Space Flight Use

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The following is being published and presented at the 1998 SPIE International Symposium on Optical Science, Engineering and Instrumentation in San Diego, at the Session on Photonics for Space Environments VI.

ABSTRACT:

For commercial telecommunications applications, a 12 channel optical fiber ribbon cable and MTP connector assembly was available from W.L. Gore for cable, and USCONEC for the MTP 12 channel connector. It was decided that for the Fiber Optic Data Bus (FODB) scheduled for flight on Earth Orbiter 1, (EO-1) that this cable assembly would be made for space flight use with as few alterations as possible, thereby providing a commercial off the shelf product for space flight applications. Technology validation techniques were used to determine the functionality of this connector/cable assembly for space flight. As part of that validation, an evaluation was conducted to determine whether all components of the connector assembly would pass space flight outgassing criteria. A technology validation study conducted on the radiation effects of the commercial fiber proposed for this application proved the commercial optical fiber from Spectran to be adequate for an EO-1 application. As a result of a high vibration environment, a larger core optical fiber (100/140 micron) was chosen to help in performance of this MTP connector under conditions that were not in the original commercial specification. Using the larger core fiber required the fabrication of connector ferrules of 140 micron outer diameter for the MTP that were previously not available. Vibration and thermal tests were conducted to determine if the commercially available 125 micron diameter connector ferrules would meet the EO-1 environmental requirements. After the technology validation was completed the final qualification testing was conducted to insure that the new space flight connector/cable assembly would perform to the FODB requirements in the space flight environment. The results and conclusions from this technology validation and qualification testing of a commercial ribbon connector/cable assembly are presented here.

Availability of Low Power High Speed Radiation Tolerant Phase Locked Loop (PLL) Frequency Synthesizers for Flight

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Up until now, the LMX23XX family of monolithic low power, high-speed *phase locked loop frequency synthesizers from National Semiconductor have been available only as commercial parts in 20-pin plastic packages. However, based on the results of their own evaluation, JPL evaluation done for the EOS-MLS project and interest from other Space users, National has announced that selected PLL products will be offered as radiation tolerant QML parts in 20-pin surface mountable ceramic packages. This provides a good example of the infusion of new COTS technology in JPL/NASA missions. The products selected for the QML offering are:

Product	Process	Status	SMD #
LMX2315	ABIC IV	In Characterization	5962-9985001
LMX2325	ABIC IV	Protos available	5962-9985002
LMX2306	ABIC V	Protos TBD	
LMX2330A	ABIC IV	Protos available	
MLX2326	ABIC V	Protos TBD	

Both the ABIC IV (0.8u feature size) and ABIC V (0.5u feature size) are state-of-the-art BiCMOS processes.

JPL performed extensive evaluation on representative devices built on the ABIC IV process, LMX2305 and LMX2325. Our evaluation shows acceptable construction, no latch up, some SEU anomalies which were found acceptable for the EOS-MLS project, and acceptable total dose (both low dose rate and high dose rate) for the EOS-MLS environment. The reliability group at National has published an application note, AN-708, which documents the hot carrier and gate oxide reliability characterization of the ABIC IV process.

JPL performed a limited evaluation of the ABIC V process as well and it showed acceptable construction and no latch up.

The parts were initially designed to work over industrial temperature range, -40C to +85C. However, by having an on-going characterization program in place, National will attempt to extend the temperature range.

* Typical supply current 4 mA at 3 V for 550MHz LMX2305, 10 mA at 3 V for 2.5GHz LMX2325.

Electronic Industries Association (EIA) G-11 Committee Meeting Summary (Feb. 1998)

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The Electronics Industry Association's (EIA) passive EEE parts user committee, known as the EIA G-11 Committee, held one of its tri-annual meetings on February 19-20, 1998 in Atlanta, GA. The G-11 Committee recommends solutions to technical problems in the application, standardization and reliability of passive EEE parts. The G-11 achieves these objectives through evaluation and preparation of proposed advancements in specifications, standards and other documents, both government and industry, to assure that parts are suitable for their intended applications and for procurement.

Membership on this committee consists primarily of major Defense and Aerospace contractors. Additional routine participation includes guest membership from NASA GSFC, the Defense Supply Center Columbus (DSCC), US Air Force, US Army and the Aerospace Corporation. NASA GSFC has actively represented the NASA Parts, Packaging and Radiation Program on the G-11 committee for many years. Through its participation in the G-11, GSFC ensures that NASA interests and the interests of the general space community are considered and adopted during development of both military and non-government specifications and standards.

The highlights of the February 1998 meeting of the G-11 are outlined in the following summary trip report. If you need further information or if you wish to suggest a topic to be discussed at the next G-11 meeting in June, please contact Jay Brusse at (301) 286-2019.

The most interesting topic of the meeting involved the discussion over the EIA U-1 Committee activities discussed below:

EIA U-1 COMMITTEE QUALIFICATION STANDARDS DEVELOPMENT

Dave Richardson of Vishay (Georgia) addressed the G-11 committee regarding the efforts of the EIA U-1 Committee (a subcommittee of the EIA P-Panels). The U-1 Committee is a passive parts "users" committee comprised mainly of EEE parts manufacturers. Their primary function is to establish industry standards for passive parts (predominantly "commercial" parts) including development of standard part values (capacitance, resistance, etc.), ratings (power, voltage, temperature, etc.) and physical sizes.

The purpose of Dave's presentation was to discuss the current U-1 Committee initiative to develop EIA standards for passive part qualification test flows for commercial products. The U-1 Committee is striving to establish "common baseline" tests for the various passive commodities which can be used by all of the manufacturers in the industry to "qualify" their commercial/industrial grade components. (At this time no EIA qualification flow standards have been finalized, although some drafts do exist). The suppl-

ers are hopeful that if they can advertise to their customer base that their products have been baselined to an established "EIA flow", then they can reduce the costly need to perform highly redundant customer specific qualification flows. In addition, an industry standard flow can be used as a baseline by which all suppliers can be benchmarked.

After further scrutiny it became apparent that the EIA currently has no "watchdog" mechanism which would oversee/audit the manufacturers to the proposed baseline flows. The existing plan would have the manufacturers "self qualify" one time (with no qualification maintenance proposal) and provide data packages to prospective customers as requested. Customers willing to accept the manufacturer's baseline flow could then request specific qualification tests for their application, which were not covered by the EIA flow. During a "brainstorming" session some G-11 participants suggested that the EIA flows should be adopted into the equivalent military specifications for the component as an "EIA Quality Level" part (in addition to the already available levels within the military specifications, NOT as a replacement). Their hope is that such an adoption would enable DSCC to become the watchdog for the EIA baseline flow. This concept has numerous potential problems:

- Potential conflict of interest for DSCC whose charter is to assure the availability of "military" parts for the "military" marketplace, not to qualify "commercial" parts for "all" markets
- Resource limitations of DSCC to audit the "commercial" product lines many of which are not the same as (or even in the same location as) the military product lines which DSCC audits
- EIA standards are intended for the entire electronics industry which means many non-military qualified sources would want to be qualified and DSCC currently has no mechanism (nor the charter) to audit the vast commercial supplier base
- Risk of watering down the military specifications and the availability of Established Reliability (or high reliability) parts

Despite the potential problems, this concept warrants further investigation as it proposes a vehicle whereby "commercial" products from a multitude of different sources may be qualified to a known baseline set of requirements. The U-1 Committee has invited G-11 representatives to participate in their April meeting to evaluate the details of the EIA developed qualification flows and to further discuss plans for implementation and oversight. In addition, both G-11 and the P-Panel will try to coordinate their autumn meetings so that some overlap/interaction between the groups would be possible.

HIGHLIGHTS OF NASA PARTS ACTIVITY

- NASA Parts Selection List (NPSL) Homepage is available on-line at:

  http://misspiggy.gsfc.nasa.gov/npsl

  This homepage is filling the parts selection and application needs of the spaceflight community in lieu of MIL-STD-975 which is to be canceled and GSFC PPL-21 which is not funded for future updates.

- NASA is encouraging a revitalization effort for MIL-STD-981 (Design, Manufacturing and Quality Standards for Custom Electromagnetic Components for Space Applications). DSCC is currently the preparing activity for MIL-STD-981. NASA plans to begin working with DSCC and others to update this document in FY98.
- GSFC has updated the GSFC procurement specification S-311-P-813 for precision metal foil resistors (similar to RNC90Y). This specification is available on-line at:

  http://arioch.gsfc.nasa.gov/311/html/specs.htm

HIGHLIGHTS OF MILITARY SPECIFICATION ACTIVITY

CAPACITORS

- MIL-PRF-55365 for tantalum chip capacitors will circulate a proposal to change the part number scheme to allow the case size to be encoded in the part number. This option would free the manufacturers to offer a discrete capacitance value in multiple case sizes depending on their processing capabilities (i.e., more capacitance in a smaller case).
- DSCC will develop drafts slash sheets for MIL-PRF-55681 ceramic chip capacitors that will cover chip sizes 0402, 0504 and 0603. Drafts are anticipated by June 1998.

- MIL-PRF-49470 for stacked ceramic Switch Mode Power Supply (SMPS) capacitors has been released. When sources begin to qualify, this specification will replace DSCC-DWG-87106. AVX Olean, Johanson, Presidio, and UTC have expressed interest in qualifying. Space level slash sheets may be added in the future.

CONNECTORS

- The Navy has proposed (and is pursuing) transfer of several Military Specification Sheets (MS Drawings) for connectors from the Navy preparing activity to the Society of Automotive Engineers (SAE). The G-11 issued a recommendation that responsibility for these drawings should be transferred to DSCC instead of SAE. This recommendation was made for several reasons including lack of influence G-11 and other military/space users have with SAE and the potential cost of renaming drawings with SAE identifiers (cost to purchase drawings from SAE, cost to change existing parts lists to reflect SAE numbers). It appears that the Navy is pursuing conversion of their specifications into Non-Government Standards (NGS) as part of their role in Acquisition Reform. The other military agencies (Army, Air Force) have taken the general approach of transferring their specifications to DSCC.

FILTERS

- Maxwell/Sierra has proposed modifications to the Class S requirements for MIL-PRF-28861/12 filters. Their proposal would allow Group B test results for one dash number to cover the Group B requirement for three other dash numbers provided the discoidal capacitors used are all from the same lot and the testing is performed on the "most complex" filter design ("L" circuit in this case). In addition, Maxwell is recommending allowing the pin ("lead") length to be "as specified" by the customer (special part marking designation may be proposed). Most end-users end up cutting the pin to a specific length (for high frequency effects) leaving exposed copper which presents a solderability problem.

RESISTORS

- MIL-PRF-914/1 and /2 (Surface Mount Resistor Networks) have been cancelled because there are no sources qualified to these styles.

TRANSFORMERS

- 1553 transformers in accordance with MIL-T-21038/27-27 may have compatibility problem with some transceivers (impedance mismatch) causing 1553 bus test errors. Ken Beymer of DSCC (614-692-0557) is a point of contact for information.
- MIL-T-21038 has been converted to a performance specification. MIL-T-21038/27 is being converted to "PRF". A new slash sheet (/28) covering dual units of 1553 data bus transformers is in draft.
- MIL-T-27 is undergoing performance conversion. A draft is expected during FY98.

OSCILLATORS

- MIL-C-55310 is in the process of being coordinated as a performance specification.

Space Parts Working Group (SPWG) Meeting Summary March 1998

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The US Air Force Space and Missile Systems Center and The Aerospace Corporation hosted the *Space Parts Working Group (SPWG)* conference on March 24 and 25, 1998 in Torrance, CA. The SPWG is an annual forum for government, international space partners, contractors (hardware builders, testers, and experimenters), and manufacturers to share their experiences with respect to manufacturing, selection and application practices for EEE parts for a variety of space flight applications. Approximately 300 people attended the conference. Common topics included:

- Approaches to parts control for space (commercial space, military, NASA)
- Approaches to the use of Commercial Off The Shelf (COTS) items in space flight programs
- Impacts of and approaches to the Department of Defense Acquisition Reform initiative (initiated by former Defense Secretary William Perry ~ 1994)

- Developments in military and industry parts control policies and procurement specifications
- Approaches to using Plastic Encapsulated Modules (PEMs) in space
- Topics in radiation effects (testing approaches, test results, product developments)
- Developments in the marketplace for space grade components
- Developments in manufacturer products for space flight

Jay Brusse from Unisys at NASA Goddard attended the conference and presented on behalf of the Components Technology Branch (Code 562) at GSFC. An overview of the highlights from this conference is provided below.

NASA PARTS PROGRAM PRESENTATION FROM GODDARD

A copy of the presentation given on behalf of NASA GSFC is available from Jay Brusse upon request. The presentation focused on the parts engineering/selection tools currently available from GSFC via the World Wide Web. These tools include such homepages as:

NASA Parts Selection List (NPSL)

http://misspiggy.gsfc.nasa.gov/npsl

EEE Parts Information Management System (EPIMS)

http://epims.gsfc.nasa.gov

Parts Analysis Web (PAWS)

http://epims.gsfc.nasa.gov

EEE Links Newsletter

http://arioch.gsfc.nasa.gov/312/Linkspg.htm

Additional topics included discussion of the deliverables produced by the Supplier Assessment Programs (PSAP – Passives, ASAP – Actives) such as the on-line "Core Suppliers Listings", information bulletins via e-mail and technology inputs into the NPSL. PSAP and ASAP personnel also participate as the voice of NASA in DoD and industry meetings for EEE parts.

COMMERCIAL OFF THE SHELF (COTS)

If there was one point that became very clear from all of the various presentations given on COTS, it would be: *there is no universal definition for COTS*. Every organization has their own interpretation of what constitutes a Commercial Off The Shelf item. Some define COTS as the manufacturer's high volume product. Some think of COTS as ANY part that can be procured directly from the vendor catalog. Others consider COTS to be defined in terms of their operating temperature range. And still others consider COTS to be any item (military grade, space grade, industrial grade or otherwise) which is readily available and can be procured without special instructions or requirements. The IRIDIUM program from Motorola defines COTS as "Industrial Grade" components purchased straight from a vendor's catalog.

Regardless of the definition used for COTS, the recurring theme from all of the presenters is that *COTS can be used successfully in space flight applications*. However, problem-free usage is contingent upon applying the appropriate engineering resources in the form of part and vendor selection, design and application considerations, parts engineering and procurement engineering. Large programs such as IRIDIUM (with well over 100 satellites in the constellation) are capable of amortizing (over a multi-billion dollar program) the Non-Recurring Engineering (NRE) costs associated with COTS selection such as source inspection and product qualification. IRIDIUM can accept additional risk due to the availability of redundant satellites. In addition, the benefits of the economies of scale with high volume procurements give the IRIDIUM procuring activity access to and influence over vendors which are critical factors to making successful product and source selections. In small programs such as those typically managed by NASA, the additional engineering costs and associated risks with using COTS may be far greater than the costs of procuring high reliability, space grade components which have a history of reliable performance.

MANUFACTURER COMMENTS ON USE OF COTS IN SPACE

The manufacturers who were represented (National Semiconductor, Harris, International Rectifier, Microsemi, Analog Devices, TI, to name a few) had common recommendations regarding use of COTS for space flight applications:

- Use robust designs capable of using the manufacturer's "standard" high volume product (NOTE: The manufacturer's "standard" product

typically has a broader distribution of parametric variables than the equivalent military specification product including some parameters which may not be specified in the catalogs or military specifications.
Ex: Inductance of resistors is typically more widely distributed in "standard" product than in military product)

- Do NOT ask the manufacturer for special processing that is outside of their normal process capabilities and flows
- Minimize handling of parts to reduce risk of damage (ESD, electrical test overstress, physical damage)
- Do NOT use COTS beyond the manufacturer's rated conditions
- Attempts to upscreen COTS will null and void all warranties and most suppliers will not provide any technical assistance in the event of failures of parts which have received third party testing/handling
- Commercial products are subject to manufacturing process and material changes WITHOUT NOTICE
- Some manufacturers may produce their commercial products in several locations each of which may use different materials and processes. This makes knowing the manufacturer and the products they supply much more difficult.
- Space flight users should try to forecast their product needs (4 years in advance) to the suppliers to help reduce obsolescence risks
- Where possible the space flight community should try to combine their product needs in order to appear as one large customer rather than several smallones. This would give the space community greater influence over market trends.

In summary, successful use of a vendor's commercial product in space flight applications requires the user to have knowledge of where and how the manufacturer builds its products and when process/material changes occur. Changes do occur and engineering resources will have to be applied in order to assess the manufacturer's "current" product. Therefore, requalification of a given commercial product may be necessary due to ongoing changes in processing and materials.

MILITARY MARKET AND SPECIFICATION DEVELOPMENTS

The following is a brief summary of the recent or in-process changes in the military marketplace and military specification:

PASSIVES:

Specification issues:

- MIL-PRF-49470 for Ceramic Switch Mode Power Supply (SMPS) capacitors has been released and several sources are in the process of qualifying (AVX, Johanson, Presidio, UTC). Most will try to qualify only the smallest sizes, but AVX Olean plans to qualify all six case sizes. This specification will ultimately replace DSCC-DWG-87106. SMPS capacitors made in accordance with 87106 have been plagued by numerous problems including thermal cracking, solder fatigue, flux entrapment, and reverse bias failures. The first qualified sources to 49470 are expected by the end of FY98.
- MIL-C-123 has been "performance" converted as of Jan. 1998. The allowable capacitance range has been increased for the CKS06 to allow for up to 1 uF.
- Many passive specifications have been modified to include a "T" level for space grade requirements and a "C" level for quasi-commercial offerings from a certified QPL line.
- Optional Surge Current testing was added to MIL-PRF-55365 (tantalum chip capacitors)
- MIL-PRF-55681 (ceramic chip caps) will soon have slash sheets offering the smaller chip sizes including 0402, 0504 and 0603. Drafts of these slash sheets are expected in June 1998.

Manufacturer Issues

- Vishay Sprague (Sanford, ME) is moving their assembly and test operation for MIL-PRF-39003 (leaded, solid tantalum capacitors) to Juarez, Mexico (initial audit occurred March 1998). Production of the anode slug will remain in the U.S. for the time being.
- Vishay Sprague is discontinuing production of CWR06 conformal-coated tantalum chip caps and promoting the form, fit and function replacement CWR09 molded chip instead.

- Dale (Bradford, PA) moved their MIL-PRF-55182 (film resistor) line to Israel in 1997. Dale still maintains a QPL facility for 55182 resistors in Nebraska.

ACTIVES:

Specification Issues

- A meeting was scheduled for April 1-2 at DSCC to discuss adding a new Class level for "Satellite Constellations" (i.e., high volume space level) in each of the key active parts specifications MIL-PRF-38535, MIL-PRF-38534 and MIL-PRF-19500. The designation for this classification is being called Class "T". A draft of the proposed changes is available.
- MIL-PRF-38535 (Microcircuits): The latest revision (12/97) has the following changes
  - Removed requirement for qualification to a minimum neutron fluence level for RHA rated parts
  - Neutron and SEE testing will be performed only if specified on the purchase order
  - HAST for PEMs increased from 50 hour test to 100 hour test
  - SEE testing moved to Appendix A
- QML-38535 (Microcircuits): There are currently 30 suppliers (10 are "V" level. 7 have Radiation Hardness Assurance [RHA] qualification). Four new sources are seeking QML certification.
- MIL-PRF-38534 (Hybrids): Proposed updates for the next revision
  - Add appendix for RHA requirements
  - Rewrite the element evaluation requirements (considering removing element evaluation requirement for JAN discretes which should be acceptable based on MIL-PRF-19500 processing/testing)
  - Change the acceleration test levels from 6000 g to 3000 g and from 10,000 g to 5,000 g respectively
  - Delete Appendix D for new technology qualification and move the key requirements into Appendix C
  - Comment was made that no one has been buying hybrids to the newer Class Levels added to the specification in 1995 (Class G = hire], Class D = consistent product, Class E = G, H or K with exceptions)
- QML-38534 (Hybrids): There are currently 44 suppliers (7 are Class "K"). Eleven new sources are seeking qualification. Three sources have opted for the Technical Review Board (TRB) option offered by this specification (Analog Devices, Remec and Lockheed Martin)
- MIL-PRF-19500: Recent changes
  - New products have been added to 19500 including Rad hard MOSFETs, SMT transistors and rectifiers, power packaging products (TO-25x types), high voltage FETs
  - Amendment 1 adds a DMS section, modifications to JANC for Class H and K hybrid use
  - Contains "Test Optimization" provisions, but no Technical Review Board

OTHER HIGHLIGHTS:

- Andrew Moor of the Applied Physics Laboratory (APL) gave a valuable presentation outlining one approach taken by APL to qualify Plastic Encapsulated Modules (PEMs) for space flight.
- Stephane Ponomarenko of the French Space Agency gave a presentation entitled "French Initiative on Commercial 3E Parts Policy for Space Applications". The primary message was "although CNES is well engaged with French industry in that field, at the project level the use is limited and implementation is selective based mainly on performance criteria".
- Wayne Daily of Motorola gave a presentation on the Parts Program for the (commercial space) IRIDIUM program.
- Alain Mouton of Matra Marconi discussed the status of an ISO standard for Parts Control Requirements (ISO-14621-2). The basic concept of this standard follows the ideas put forth in the AIAA-R-100 Parts Management specification. This standard is expected to be approved by the end of FY98.
- Leon Hamiter of CTI gave a summary of the information shared at the recent Commercialization of Space Working Group meeting in Huntington Beach, CA in February 1998. Many of the ideas shared at this conference mirror those discussed at the SPWG conference.
- Numerous presentations were given about Radiation effects: including presentations by Chuck Barnes (JPL), Lew Cohn (DSWA), Capt. Dan King

(Philips Labs), Al Kuehl (US Army), Philip Layton (SEI) and Don Mayer (The Aerospace Corp.)

- Sandy Kraft from GIDEP gave a presentation on the information available through GIDEP plus some new initiatives in data sharing by OEMs. A prototype system is being developed which will enable OEMs to have their internal databases linked/accessible to the GIDEP community (ex., contractor sharing their database on fastener testing and failures). Sandy highlighted one valuable portion of GIDEP which is often not broadly discussed is the availability of "on-line" calibration procedures shared by manufacturers of test equipment. This information could be very useful for metrology, calibration and repair organizations.

Electronic Components for the Commercialization of Military and Space Systems Workshop

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The Electronic Components For The Commercialization Of Military And Space Systems Workshop held its second annual meeting February 2 through 4, 1998, in Huntington Beach, California and attendance seemed to be even higher than last time; there were at least 400 people present. A very diverse group was in attendance, including representatives from: part manufacturing, parts engineering, circuit design, board and box assembly, system and sub-system integration, marketing, and parts management, control and test. Commercial and government military and space interests were well represented. In all, this was an unusual, possibly unique collection of interests and perspectives to be found together in one room.

The presentations covered topics as diverse as: a new failure mechanism in tantalum chip capacitors; microsatellite batteries and ruggedized PCMCIA disk drives. A majority of the presentations contained one or more of the following, recurring themes:

1) Commercial-off-the-shelf (COTS) works satisfactorily for high reliability applications including space <u>but not</u> "straight out of the box".
2) Successful use of COTS requires:
   a) Careful vendor selection.
   b) Detailed knowledge of the part – performance, strengths and weaknesses.
   c) Qualification by testing, data analysis, etc.
   d) Screening specifically aimed at potential weaknesses that could negatively impact the intended application.
   e) Ruggedized packaging, enclosures, mounting means appropriate to the application.
3) Changes to COTS product, which can affect performance in application, <u>will occur</u>. Trying to prevent this by requiring the vendor to provide notification <u>does not work</u>.
4) The commercial vendor has little or no interest in the military/space market and will do nothing to their product to help suitability for these applications. Changes/process variation can produce large variations in susceptibility to radiation effects, temperature/frequency characteristics etc., within the published catalog envelope.
5) Cost reduction is not a reason to pursue COTS for use in high reliability and space applications. The returns are generally small and the risks may be large. Most of the item cost savings are eliminated by the additional costs of the qualification, screening and selection activities necessary to assure part performance.
6) Few reportedly successful hi-rel applications of COTS are really COTS (see discussion of Mars Pathfinder below).

Two outstanding keynote presentations were given: Colonel Cardine of the US Army who talked about COTS and the Abrams tank and James Clawson of the Jet Propulsion Laboratory who discussed "Common Sense" Mission Assurance as applied to the Mars Pathfinder Project.

Colonel Cardine is the Project Manager for the latest generation of Abrams tank, which is equipped with very sophisticated electronics. The electronics are largely COTS, but heavily ruggedized COTS. Colonel Cardine's statement was "Everything does not have to

be military, it just has to be able to survive in a military environment". An example of this philosophy in practice is: a commercial 2-Gigabyte disk drive mounted in a nitrogen-filled, metal, hermetic box, equipped with internal and external shock mounts. The disk drive was COTS but the final package certainly was not!

James Clawson is now the Manager of JPL's Reliability Office and was the Mission Assurance Manager for the Mars Pathfinder Project. Mr. Clawson provided facts about the Mars Pathfinder that clearly show a lot of misinformation has been circulating about this project and its use of COTS. Somehow the rumor got started that Mars Pathfinder used "commercial parts" and Mars Pathfinder became a glowing example of COTS in space. In fact, the bulk of the electronics used for the mission were full MIL specification. Approximately 50% of the microcircuits were Class S the rest were Class B and essentially all of the passives were NASA Grade 1 (MIL failure rate level R and S). The Mars mission achieved its impressive cost control and tight schedule by utilizing a common buy of electronic parts with the CASSINI project, not by extensive use of COTS. There were COTS items used, the modems on the Lander and Rover, the cameras and power modules on the Rover, but they were in the minority and these items are not available as MIL spec. Additionally, the COTS items were upscreened for the extreme Martian environment by the use of extensive burn-in and temperature cycles. In the case of the modems, the two used for flight were hand picked out of the population of 50 units that JPL purchased. Even though the project used mostly NASA Grade 1 and 2 electronic parts, the total parts cost was <u>less than 2% of the total project cost</u>! This suggests that for projects such as one-off scientific satellites, COTS should not be pursued simply to save money.

The Workshop seemed to be in the process of a change of emphasis, away from "what is COTS and can we really use it?" to "what is COTS, how has it been used successfully and what can I learn from this?" Another Workshop is planned for around the same time next year.

Jet Propulsion Laboratory Parts Analyses

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Failure analyses (FA), destructive physical analyses (DPA) and part construction analyses (PCA) have been performed on the following part types. For a copy of the report, contact me (phone 818-354-9529, fax 818-393-4559 or e-mail to joan.c.westgate@jpl.nasa.gov) and request the desired document by "Log#".

NOTE: THE SUBJECT JPL REPORTS MAY CONTAIN PROPRIETARY INFORMATION WHICH IS SUBJECT TO LEGAL RESTRICTIONS. QUESTIONS REGARDING THIS NOTICE SHOULD BE ADDRESSED TO JOAN C. WESTGATE.

FAILURE ANALYSIS

Log No.	Manufacturer	Date Code	Part Type	Part Number
6990	Analog Devices, Inc. (ADI)	9620	10-Bit Monolithic A/D Converter	AD773
7066	Compensated Devices, Inc. (CDI)	Unknown	Surface Mount Schottky Barrier Diode	JANTXV1N5711UR-1
7069	Motorola (MOT)	8704	NPN Transistor	JANS2N2222A
7070	PPC Products Corporation	9433	NPN, Silicon Power Transistor	2N5339

DESTRUCTIVE PHYSICAL ANALYSIS

Log No.	Manufacturer	Date Code	Part Type	Part Number
6991	Siliconix	9718	Quad Transistor	SD5000I-2
6999	Lambda Advanced Analog	9507	DC-DC Converter	AHV2812TF/CH
7002	Reticon	9645	Photodiode Array	RL0128KAU
7002A	Reticon	9645	Photodiode Array	RL0128KAU
7004	BEI (Bell Industries)	None	Photocell Flatpack Assembly	621-0046-100
7005	BEI	None	IR Light Emitting Diode	611-0024-101
7009	Lambda Advanced Analog	9637	DC-DC Converter	ATR2812D/CH
7011	CTS	9730	PC Preamp Hybrid	21053819-101
7012	CTS	9730	Relay Driver Hybrid	21053901-101
7014	International Manufacturing Service	H TK-382	50K Ohm Resistor	IMS 007-1-5002 J
7024	MDI	9724	Hybrid DC/DC Power Converter	2690R
7029	KD	9721	Capacitor	87106-075
7030	KEM (Kemet Electronics Corp.)	9534KA	Tantalum Capacitor	95158-11KH
7031	KEM	9709	Tantalum Capacitor	95158-19KH
7032	KEM	9709	Tantalum Capacitor	95158-23KH
7033	Unknown	9703	Tantalum Capacitor	93026-47KS
7034	KEM	9644	Capacitor	M39014/01-1305
7035	KEM	9645	Capacitor	M39014/01-1351
7036	KD	9740	Capacitor	SM20B103K501M
7037	VIT (Vitramon, Inc.)	9620A	Capacitor	VJ0805Y332KFCAB
7038	VIT	9626A	Capacitor	VJ0805Y102KFCAB
7039	VIT	9726A	Capacitor	VJ0805Y561KFCAB
7040	VIT	9741	Capacitor	5VJ0805A681JXBMT
7041	International Rectifier	9634	Dual Diodes	12CGQ150
7042	International Rectifier	9710	Diode	22CGQ0045
7043	CDI	9434	Temp. Compensated Zener Reference Diode	JANTXV1N4569AUR-1
7044	Harris	X9645AAA8	Quad 2 Input NAND Gate	CD4011BKMSR
7045	Harris	X9645AAAB	Triple 3 Input NAND Gate	CD4023BKMSR
7046	Harris	X9705AAAP	CMOS Phase-Lock Loop	CD4046BKMSR
7047	Linear Technology	6D9713A	High Voltage Positive Adjustable Regulator	LM117H VH/883B
7054	Comm. Industries, Inc.	9642	Relay	M39016/9-060M
7084	BKC Semiconductors	Unknown	Surface Mount Schottky Diode	LL101A

PART CONSTRUCTION ANALYSIS

Log No.	Manufacturer	Date Code	Part Type	Part Number
Part Construction Analysis Reports were not submitted for publication at this time.				

Goddard Space Flight Center Parts Analyses

Listed below are the EEE parts analyses completed by the GSFC Parts Analysis Laboratory. The GSFC reports are available to NASA personnel and current NASA contractors by contacting your NASA project office.

EV JOBS							
Job Number		Manufacturer	Date Code	Part Type	Part Number	Result	Date
80626	EV	HARRIS SEMICONDUCTOR	9435, 9422	MICROCIRCUIT	HS926C31RH-Q	P	03/25/98
80651	EV	NANONICS	---	CONNECTOR	STM05510573SCAN	P	02/27/98

EC JOBS							
Job Number		Manufacturer	Date Code	Part Type	Part Number	Result	Date
88186	EC	ADVANCED ANALOG	9804	ASA2805S/CH	5962-9462901HXA	F	03/13/98
89164	EC	TRIANGLE LABS	UNKN	P W BOARD	XPAA-117	F	01/29/98
89159	EC	NORTH TEXAS CIRCUITS	00698	P W BOARD	435526 REV B	P	01/28/98
89160	EC	NORTH TEXAS CIRCUITS	00698	P W BOARD	435532	P	01/28/98
89161	EC	SOVERIGN CIRCUITS	9751	P W BOARD	7370-3140 REV A	P	01/28/98
89162	EC	SOVERIGN CIRCUITS	9751	P W BOARD	7370-1344 REV A	P	01/28/98
89163	EC	COLONIAL CIRCUITS	9750	P W BOARD	7348-3044 REV B/B	P	01/28/98
89156	EC	SPEEDY CIRCUITS INC	9752	P W BOARD	80892510	P	01/27/98
89157	EC	TYCO ENGINEERED	0198	P W BOARD	2009323-1	P	01/26/98
89145	EC	COLONIAL CIRCUITS	9750	P W BOARD	2009331-1	P	01/23/98
89152	EC	TYCO ENGINEERED	0198	P W BOARD	GC1561123-1FM	P	01/23/98
89153	EC	COLONIAL CIRCUITS	9748	P W BOARD	GD2009332-1	P	01/23/98
89150	EC	TYCO ENGINEERED	4897	P W BOARD	185353-1	P	01/22/98
89154	EC	CIRTECH INC	5297	P W BOARD	EVL2160 REV B	F	01/22/98
89155	EC	CIRTECH INC	5297	P W BOARD	EVD2170 REV A	P	01/22/98
89158	EC	TYCO ENGINEERED	5197	P W BOARD	185089-1	P	01/22/98
89148	EC	TYCO ENGINEERED	4897	P W BOARD	185323-1	P	01/20/98
89142	EC	ADVANCED QUICK	5297	P W BOARD	2009357-1	P	01/20/98
89149	EC	ADVANCED QUICK	5197	P W BOARD	185088-1	P	01/15/98
89146	EC	TYCO ENGINEERED	5297	P W BOARD	184969-1	P	01/15/98
89143	EC	ADVANCED QUICK	5297	P W BOARD	2009356-1	P	01/15/98
89147	EC	TYCO ENGINEERED	5297	P W BOARD	184968-1	P	01/15/98
89151	EC	PRECISION CIRCUITS	5297	P W BOARD	040-082	P	01/14/98
89140	EC	CIRTECH INC	5297	P W BOARD	040-057	P	01/13/98
89144	EC	COLONIAL CIRCUITS	9750	P W BOARD	2009393-1	P	01/13/98
89139	EC	CIRTECH INC	UNKN	P W BOARD	857282-1	P	01/12/98
89141	EC	COLONIAL CIRCUITS	9750	P W BOARD	2009302-1	P	01/12/98
89138	EC	NORTH TEXAS CIRCUITS	36097	P W BOARD	435529	F	01/07/98
89136	EC	ADVANCED QUICK	5197	P W BOARD	185319-1	P	01/06/98
89101	EC	COLONIAL CIRCUITS	9744	P W BOARD	GD2009296-1	P	01/05/98
89131	EC	COLONIAL CIRCUITS	9744	P W BOARD	GD2009296-1	P	01/05/98
89130	EC	COLONIAL CIRCUITS	9748	P W BOARD	GD2009332-1	P	01/05/98
89135	EC	PRECISION CIRCUITS	5297	P W BOARD	040-082	F	01/05/98
89134	EC	CIRTECH INC	5197	P W BOARD	GE1552321-3	P	01/02/98

CA JOBS							
Job Number		Manufacturer	Date Code	Part Type	Part Number	Result	Date
88194	CA	LINFINITY	9712	5962-01-239-4123	M38510/11703BXA	P	03/28/98
88191	CA	MICROSEMI CORPORATION	9713	1N5611	JANTX1N5611	P	03/26/98
88190	CA	MICROSEMI CORPORATION	8835	1N4944	JANTXV1N4944	P	03/25/98
88180	CA	UNKNOWN	9715, 9719, 9725	CAPACITOR	CDR31BX103AKW S	P	03/20/98
88171	CA	HARRIS SEMICONDUCTOR	9719	CD4049UBDMSR	5962R69663601VE C	P	03/11/98
88168	CA	ADVANCED ANALOG	9745	HYBRID	91020-02HZA	P	03/02/98
88169	CA	ADVANCED ANALOG	9750	HYBRID	ASF-461/CH FILTER	P	02/26/98
88154	CA	UTMC	9736	UT22VP10T-20U	5962R9475404VXA	P	02/25/98
88163	CA	HARRIS SEMICONDUCTOR	9721	2N7225	JANTXV2N7225	P	02/24/98
88164	CA	MICROSEMI, INC.	9713	1N5611	JANTX1N5611	F	02/23/98
88105	CA	ANALOG DEVICES	9723	MICROCIRCUIT	ADVFC32SH/883B	P	02/06/98
88142	CA	HARRIS SEMICONDUCTOR	9750	N-CHANEL MOSFET	FSJ260D1	P	02/05/98
88100	CA	LINEAR TECHNOLOGY	9449	LT1058AML/883	5962-8989701XA	F	02/01/98
88138	CA	NATIONAL SEMICONDUCTOR	9530	MICROCIRCUIT	JM38510/10702BXA	P	01/27/98
88139	CA	NATIONAL SEMICONDUCTOR	9703	MICROCIRCUIT	JM38510/10703BXA	P	01/26/98
88128	CA	BKC SEMICONDUCTORS	9649	1N6328	JANTX1N6328	P	01/26/98
88128	CA	BKC SEMICONDUCTORS	9649	1N6328	JANTX1N6328	P	01/26/98
88118	CA	MICROSEMI	9718	1N4148-1	JANTXV1N4148-1	P	01/23/98
88140	CA	NATIONAL SEMICONDUCTOR	9702	MICROCIRCUIT	JM38510/10707BYA	P	01/21/98
88143	CA	MICROSEMI, INC.	9709	1N6492	JANTXV1N6492	P	01/16/98
88110	CA	SENSITRON SEMICONDUCTOR	9735	1N4245	JANTXV1N4245	F	01/13/98
88103	CA	NATIONAL SEMICONDUCTOR	9738D	MICROCIRCUIT	LM140K-15/883	P	01/07/98

GIDEP & NASA Advisory Impact Report

NASA Advisories, GIDEP Alerts, Problem Advisories, Safe Alerts, Product Change Notices, Diminishing Source Notices and Agency Action Notices Related to EEE Parts

GIDEP & NASA Advisory Impact Report summary will no longer be included in the EEE Links publication. For the most current information on parts issues please refer to the EPIMS database on the WWW. The URL for EPIMS-WEB is : http://epims.gsfc.nasa.gov