ELECTRONIC PACKAGING & SPACE PARTS NEWS

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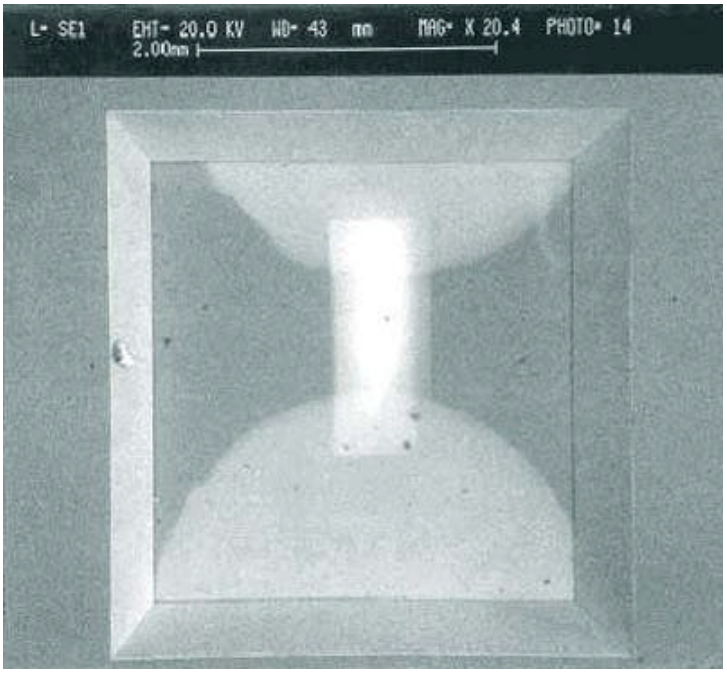
Reliability and Qualification of III/V Semiconductor Devices for Space Applications



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Cover photo shows a scanning electron micrograph of a manually assembled GMR-MEMS sensor device.

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Letter from the Editor

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Welcome to the April issue of EEE Links. As I mentioned in the last issue of EEE Links our URL address has changed. The new URL for EEE Links on the Web is http://misspiggy.gsfc.nasa.gov/ctre/hq/eee_links.

As always, please keep us informed of your questions and needs so that we may be able to serve you better.

NASA/Jet Propulsion Laboratory Electronic Packaging for Space Applications Workshop and International Microelectronics and Packaging Society SoCal'99 Symposium & Exhibition

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JPL's Electronic Packaging and Fabrication Section and the Quality Assurance Engineering Section along with three Southern California Chapters of the International Microelectronics and Packaging Society (IMAPS) are jointly sponsoring an event on May 12 and 13, 1999. This event consists of a symposium and an exhibition, and will be held at the Pasadena Convention Center in Pasadena, California.

The objective of this event, from the NASA/JPL perspective, is to provide a forum for the exchange of information between spacecraft electronic systems designers and those who are engaged in developing and validating advanced electronic packaging techniques having potential uses in spacecraft and associated instruments. This exchange of ideas, achievements and requirements, hopefully, will promote a more coordinated effort in the advancement of spacecraft electronics. The work being done by the NASA Centers under the NASA Electronic Parts and Packaging Program will be highlighted, but discussions of other activities in advanced packaging for space applications will certainly be encouraged and included in the program. The cognizant persons at the participating NASA Centers, including JPL, have been contacted, and technical papers for presentation have been solicited.

The IMAPS Southern California Symposium & Exhibition has a broader view of microelectronics which encompasses all areas of advanced electronic packaging. IMAPS has notified its membership of the event and has been soliciting papers presenting achievements of industry, government, and academia. The SoCal'99 committee views this event as an opportunity to enhance its range of technical topics through the cooperation of NASA/JPL and, possibly, to provide a vehicle for introduction of new packaging technology into space, heretofore, not being applied within the NASA programs.

The technical presentations will be scheduled for both days. Because of the expected number of papers, two tracks of presentations have been planned, and attendees will be able to move between tracks in accordance with their individual interests. An agenda of selected papers will be available in early April. In addition to the technical presentations, IMAPS SoCal'99 will host an exhibition of industry products, tools, and services related to microelectronics packaging. A display area in the Pasadena Convention Center will be devoted to this purpose on the second day of the event.

There will be no registration fee for attendees, but advanced registration is encouraged and advised. Registration can be made via the Website exclusively devoted to this event. The Website will also contain abstracts, the agenda, maps of the Pasadena area, suggested hotels, and other helpful information for the attendees. It will be maintained and updated as new information is available. The published proceedings will contain only the abstracts of the final papers.

The Website for this event is:
http://137.79.61.135:2001/workshop/package.htm

Radioactive Parts

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Summary: Exposing space flight hardware or component parts to neutrons or high-energy protons can induce radioactivity. These parts may have enough activity to warrant special handling and shipping. Check with the facility operator prior to shipping parts to insure that the items do not require a license to possess them and that they are being correctly packaged for shipment.

NASA researchers sometimes require certain electronic parts be tested in radiation environments such as those found at a nuclear reactor or an accelerator facility. Neutrons from reactors and high-energy protons from accelerators can induce radioactivity in metals and plastics. This exposure actually changes the materials to radioactive isotopes that usually have varying half-lives, depending on the energy of the neutrons or protons used.

Please insure that the GSFC Radiation Protection Officer is notified prior to activation of materials that are to be sent to our Greenbelt or Wallops facilities. There may be Nuclear Regulatory Commission (NRC) licensing requirements or US Department of Transportation regulations that must be reviewed prior to shipping these materials to GSFC.

If you have any questions, please contact the GSFC Radiation Protection Officer at 301-286-8482.

Variables Affecting CSP Reliability

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ABSTRACT

Although the weakest link of chip scale package (CSP) assembly reliability has been often internal package failure, solder joint fatigue is still considered to be the key factor for reliability. Other key factors that affect solder joint reliability including package type, package build, board design, assembly variables, and accelerated environmental testing are also discussed. The reasons for unrealistic life projections for CSP assembly reliability by numerous modelers is also examined. It was concluded that availability of meaningful assembly reliability test results are needed to accelerate implementation of this technology. The JPL-led CSP consortia are addressing many of these issues.

CSP RELIABILITY

The CSP packages provide the benefits of small size and performance of the bare die or flip chip, with the advantage of standard die packages. Although CSP was defined by “industry experts” as a package that is up to 1.2 or 1.5 times larger than the perimeter or the area of the die, many manufacturers refer to the package that is a miniaturized version of the previous generation.

There are many factors that affect CSP assembly reliability. These include design, package build, solder paste, assembly, underfill, and type of test for reliability evaluation. In the following a few of these variables are discussed.

DESIGN

PWB pad design

For BGAs, discussions on use of solder mask defined vs. non-solder mask (SMD vs. NSMD) were hot subjects for a short period. There were two camps, one showing the improvement due to use of SMD– reasoning that masks over copper are needed for improved adhesion as well as the potential benefit of cycles to failure increased due to increase in solder joint height. The other camp showed that crack initiation in solder, due to overlaying of the mask, could reduce the number of cycles to failure. NSMD is now commonly recommended.

The pad size design relative to package has its own supporters. As a rule of thumb, the board pad size should be the same as the package. A slight unbalance in this relationship could result in failure at the board or package. Optimized conditions might differ for different packages depending on the ball attachment configuration.

PACKAGE VARIABLES

Die bond on interposer

There are various techniques that are used to transfer the die I/O to the interposer within the package. Each element of the package internal form has its own effect. For TAB CSP (Tape Automated Bonding), the TAB is the weakest link. For flip chip die in a flip chip CSP, the failure was observed on the C5 (board level) solder joint interconnection, when subjected to thermal cycling. This might not be the general case for the flip chip die. CSPs and BGAs with flip chip dies are more susceptible to internal package failure than their wire bond versions.

Interposer thickness

When the interposer was increased from 0.4 mm thickness to 0.6 mm, cycles to failure increased from 400 to about 800 cycles (-25/125°C). Data for a flip chip CSP, indicates that semi-rigid interposer would have 1.88 times the number of thermal cycles. Is the rigidity equivalent to thickness change or possibly because of materials change? The answer is not known. Interposer CTE also has significant affect on the board reliability.

Interposer materials

CSPs with different interposer materials showed significantly different cycles to failure– about a three times increase (Sony, IMAPS '97). In an experiment, it was found that a factor of about three times will be achieved when a low CTE interposer was used (1200 vs. 400 cycles, -25/125°C).

Die size

In one study it was shown (R. Darveaux, ECTC '98) that when die size increased from 6.4 mm to 9.5 mm, the first cycles to failure decreased from 1500 to 900 cycles in the range of -40°C to 125°C.

SOLDER BALL

Solder composition

Eutectic solder (63/37) is the most commonly used solder due to it having many desirable attributes, including low temperature melting. To improve fatigue characteristics, small amounts of silver (2%) have been added to this composition. Additive materials have the potential of formation of brittle intermetallic phases as well as softening by precipitation formation. These metallurgical transitions are further accelerated by increases in temperature. Effect of five element alloy was shown to improve thermal cycling reliability by 1.2 to 1.5 times (Ano, SMI CSP Symposium Proceedings '97).

Ball shape attachment

For BGAs, it has been demonstrated that the DBGAs (Dimple BGA) improve reliability. This might be the case for CSPs too, but its significance is yet to be demonstrated.

ASSEMBLY VARIABLES OF RELIABILITY

Solder joint height

The effect of solder joint height on reliability has been widely discussed for BGAs. One reason for the use of an SMD pad for PBGAs, with collapsible solder, was to increase solder ball height and hence increase reliability. Height was also increased by use of columns in the ceramic column grid arrays to achieve significant reliability improvements compared to the ball grid array version. Improvement was shown for CSPs when ball heights are increased (Kosuga IMAPS 97). When solder height is doubled, cycles to failure for the board tripled– a Coffin-Manson exponential value of β=1.6.

Underfill

One key advantage of CSPs over flip chips is that ideally there is no requirement for CSPs to be underfilled. The assemblers for consumer products prefer packages with no underfill one process step is eliminated and reworkability is permitted. However, for high reliability applications where vibration and shock are key in ruggedness, use of underfill might be the only solution now known to meet the harsh requirements.

For flip chips with very short cycles to failure, it has been shown that underfill will improve cycles to failure reliability an order of magnitude (5-10 at least). This is very similar to the results shown for the wafer level miniBGA packages with and without underfill.

Double Reflow

There are many concerns when double sided boards are assembled. Reliability reduction is one. For heavy BGAs, one concern was potential part fall from the assembled side during the second reflow. Similar concerns might be true for CSPs with the small solder volume; not enough tension force to hold even the small size of CSPs. In addition, it has been shown that

for two sided packages, reliability of board assembly was half of the single sided (Kosuga, IMAPS '97). Recently, similar test results were presented for another CSP package (Juso, ECTC 98). Double sided assemblies with packages on directly opposite sides of the board showed lower cycles to failure. This was improved with partial relative package offsets on the two sides.

FAILURE MECHANISMS AND CSP RELIABILITY

Solder joint interconnects were considered to be the main cause of assembly failure. Failure at the board level could also be caused by the internal failure of the package. For example, package internal TAB lead failures at heels were reported for the CTE absorbed CSP— a fatigue failure shift from the solder joint to the internal package. This new type of failure is in contrast to the traditional theoretical wisdom where the solder joint failure is generally considered to be the weak link in solder joint assemblies. This and other failure mechanisms, which are being established for CSPs, must be understood by a modeler before he/she is to predict a meaningful reliability projection.

Table 1 includes four projections from different modelers and experiment test results. It is interesting to compare the theoretical values with those experiment test results for numerous CSPs. It becomes obvious that these calculations are at least 5 to 20 times higher than the test results. To date, the highest value test results reported for CSPs are in the range of 500 to 1,000 cycles. Projections of more than 20,000 cycles to failure in the range of -55 to 125°C is very unrealistic and are misleading.

Misleading results could also occur when DNP (distance to neutral point) is used as indicator for cycles to failure. In the IPC report J-STD-012 (Joint Industry Standard Implementation of Flip Chip and Chip Scale Technology), assembly reliability projections were based on flip chip die being attached to the board. DNPs were used for calculation of the first failure and projection of failure with size of package. This is not valid for most CSPs, except possibly for a few wafer level CSPs without underfill. Although there is a relationship between an increase in die size and reliability, the relationship is not linear and depends on many parameters. For example, fan-out packages with small die will not follow the DNP indications.

Table 1. Misleading CSP Cycles to Failure Projections by Modeling

Package Type	I/O	Cycle Profile	Cycles to Failure Projection	Test Results
TAB CSP	46	-55/125°C	7,000	500-1,000
WAFER CSP	96	-40/125°C	3,200	200-500 8 failures
FLIP CHIP CSP	N/A	-55/125°C	20,000	N/A
LOW COST CSP	N/A	-40/125°C	21,000	N/A

LESSONS LEARNED AND RECOMMENDATIONS

Board reliability information is essential for CSP implementation for high reliability applications and to ease their use in commercial sectors. For wider application of this technology, the potential user will need design reliability data since they often do not have the resources, time, or ability to perform complex environmental characterizations. To help build the infrastructure in these areas, nearly 200 test vehicles were assembled by the JPL-led consortia to address many technical issues regarding the interplay of package types, I/O counts, PWB materials, surface finishes, and manufacturing variables for the quality and reliability of assembly packages. Results will be published as they become available.

REFERENCES

Four main sources of information for the text were from:

1. SMI '97, Proceedings of Chip Scale Packaging Symposium, SMI, Sept. 7-11, 1997
2. IMAPS '97, Proceedings of International Symposium on Microelectronics, Philadelphia, October 14-16, 1997
3. CSI '98, Proceedings of Chip Scale International, San Jose, May 6-7, 1998
4. ECTC '98, Proceedings of 48th Electronic Components & Technology Conference, Seattle, May 25-28, 1998

ACKNOWLEDGMENTS

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Giant Magnetoresistive (GMR) Sensor Microelectromechanical System (MEMS) Device

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The measurement of acceleration has been accomplished using several technologies in high-reliability applications such as guidance control, detonation, and shock/vibration measurement. Electromechanical, piezoelectric, piezoresistive, and capacitive acceleration sensors are available and the literature pertinent to giant magnetoresistive sensors (GMR) for the above applications are scanty.

The GMR effect was recently discovered in sputtered metallic thin films consisting of magnetic layers a few nanometers thick separated by equally thin nonmagnetic layers. Large decrease in the resistance of these films is observed when a magnetic field is applied. The cause of this effect is the spin dependence of electron scattering and the spin polarization of conduction electrons in ferromagnetic metals. With layers of the proper thickness, adjacent magnetic layers couple antiferromagnetically to each other with the magnetic moments of each magnetic layer aligned antiparallel to the adjacent magnetic layers. Frequent scattering of electrons results in high electrical resistivity of the GMR device. If an external field overcomes the antiferromagnetic coupling, it achieves parallel alignment of moments in adjacent ferromagnetic layers; the spin dependent scattering of conduction electrons is decreased and resistivity decreases. The size of this decrease in resistivity can be 10% to 20% and higher in GMR materials with multiple nonmagnetic layers. The significant advantage of GMR sensor materials is the greater sensitivity to applied magnetic fields. This increased sensitivity of the sensor materials makes it possible to detect smaller change in the magnetic fields. Large signals from GMR material structures also help overcome electronic noise.

GMR sensors are composed of four thin films such as a sensing layer, a conducting spacer layer, a pinned layer, and an exchange layer. The thickness of all these layers is very thin except for the exchange layer which will allow the conduction of electrons to frequently move back and forth between the sensing and pinned layers via the conducting spacer layer. The magnetic orientation of the pinned layer is fixed and held in place by the adjacent exchange layer, while the magnetic orientation of the sensing layer changes in response to the external magnetic field. A change in the magnetic orientation of the sensing layer will cause a change in the resistance of the combined sensing and pinned layers.

GMR sensors directly detect the magnetic field and they are sensitive to small changes in the magnetic fields, and can be used to measure position or displacement in linear and rotational systems. Some of the applications for GMR magnetic sensors are current sensing, linear or rotatory motion detection, linear or rotatory position sensing, ignition timing, throttle position sensing, etc.

DC magnetron sputtering has been used to deposit thin film multilayers in a nanometer thickness range in UHV chamber to fabricate GMR sensor element. The silicon dioxide has been grown over Si substrate using thermal oxidation, which was used as a substrate in this study to fabricate GMR sensor element. The sputtering of GMR element materials was performed at room temperature in a Argon ambient. The structure of a typical spin valve is silicon/silicon dioxide/tantalum/copper/cobalt/FeMn/tantalum. Cobalt layer has been inserted between the permalloy and copper to enhance the GMR ratio and that will protect permalloy from mixing with the copper. Carbon and oxygen impurities in various layers have been observed to be reducing the GMR performance.

Thickness of the copper spacer layer, temperature stability, electrostatic discharge, change in magnetization, patterning of GMR element by lift-off process, annealing of hard magnetic thin film, and the field damage will influence the reliability of GMR characteristics. Cobalt and copper do not mix at moderate temperatures, however permalloy and copper do mix and if permalloy is used adjacent to copper, the spin valve will degrade around 200°C. GMR layers are extremely thin, only about 300 – 400 Å, so the temperature rise from a voltage spike can possibly melt the layers. There is also other possibility that of the magnetization changes if the temperature of the layer exceeds the Neel temperature of the

antiferromagnetic layer. The GMR sensor material should have resistance to electrostatic discharge and resistance to thermal degradation.

The fabrication of GMR sensor involves three steps and they are as follows: a. fabrication of GMR sensor on the substrate, b. fabrication of the movable microstructure such as a membrane and finally, c. deposition of hard magnetic thin film onto the movable microstructure. Critical issues associated with the fabrication of a GMR sensor device are signal to noise ratio, geometry and lithographic definition of the spin valve on the substrate, magnetic properties of hard magnetic thin film, and process integration with surface and bulk micromachining processes.

Figure 1 shows the schematic of the complete GMR / MEMS sensor device. A silicon substrate has been chosen in this study and silicon nitride was deposited using low-pressure chemical vapor deposition (LPCVD) process. Silicon nitride on one side of the silicon substrate was patterned and plasma etched down to the silicon substrate. The silicon substrate was anisotropically etched until silicon nitride onto the other side of the silicon substrate to fabricate very thin silicon nitride membranes. Another silicon substrate has been chosen and the growth of silicon dioxide was performed by thermal oxidation. Giant magnetoresistive element has been fabricated using lift-off technique onto the silicon dioxide. These two chips can be bonded using anodic bonding or any other appropriate technique to assemble the device as shown in the Fig. 1. Figure 2 shows the manually packaged complete GMR sensor device that includes GMR element, silicon nitride microstructure, and a hard thin film magnet deposited over the microstructure.

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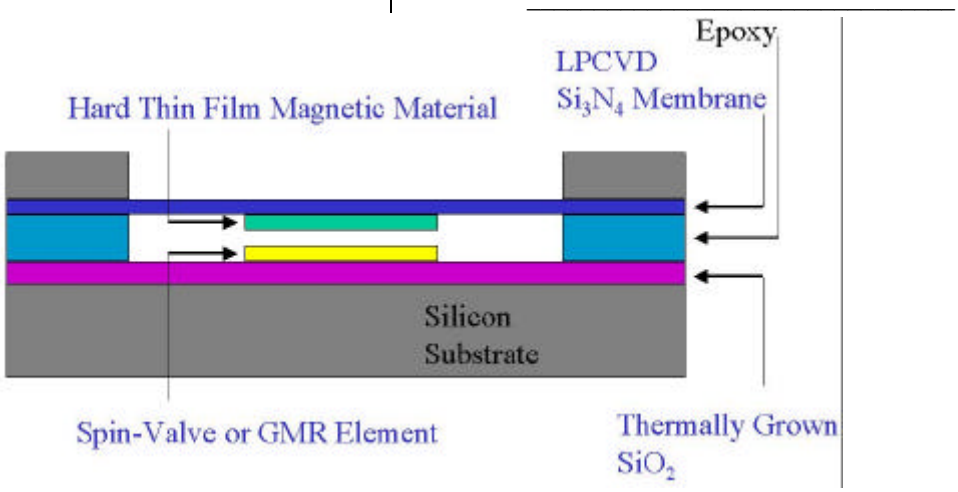

Figure 1. Schematic diagram of complete giant magnetoresistive (GMR) sensor device fabrication
***Ref.:* Ramesham**

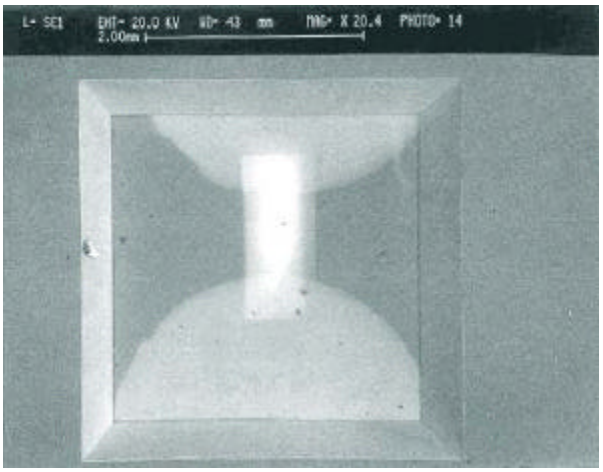

Figure 2. Scanning electron micrograph of the manually assembled GMR-MEMS sensor device.
***Ref.:* Ramesham**

Chlorine Contamination Diffusion in Silicones

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Using the diffusion cell technique and autoclave tests of aluminum corrosion test structures it has been shown that silicones are much more permeable for volatile chlorine containing contaminants than for nonvolatile. The estimated diffusion coefficient at 121°C is less than $(4 – 7) \times 10^{-11}$ cm^2 / s for nonvolatile chlorides (NaCl) and $(4\text{-}9)\times 10^{-9}$ cm^2 / s for volatile ones (HCl). The activation energy of diffusion is estimated to be 0.3-0.4 eV in the first case and approximately 0.1 eV in the second. Due to the different permeability for volatile and nonvolatile chlorides, silicones provide protection in moisture environments as conformal coatings on boards and are much less effective as buffer layers in plastic encapsulated devices.

Silicones have been used for many years as glob-top encapsulating compounds, buffer layers in plastic encapsulated devices, and conformal coatings in electronic assemblies due to the perfect combination of mechanical, thermal, and electrical characteristics. Although silicones have relatively low moisture sorption coefficients, their diffusion coefficient is significantly larger (approximately two orders of magnitude) than in epoxies resulting in a relatively high permeability to moisture. The ability of polymer material to provide environment / corrosion protection to electronic elements depends not only on their moisture characteristics but on their permeability to ions and in particular, chlorine ions. Unfortunately, ion permeability of encapsulating materials has not been addressed thoroughly yet. Studies started in CALCE center and reported in [1] indicate that epoxy molding compounds may not provide sufficient protection against ion contamination.

In this study the diffusion coefficient of chlorine contamination in silicones has been estimated using two techniques. One technique is the autoclave (121°C, 2 atm.) test of aluminum test structures (corrosion susceptibility). The other is based on measurements of conductivity of the sodium chloride electrolyte in a diffusion cell.

EXPERIMENTS AND RESULTS

A scheme of the diffusion cell technique is shown in Figure 1. Approximately 10 mg of NaCl was placed in a silicone cell with a wall thickness S = 0.7 mm. The cell was placed in a container with 100 ml of deionized water at 100°C. Electrodes were inserted for conductivity monitoring. The diffusion delay time θ in the conductivity variance with time gives the diffusion coefficient:

$$D = \frac{S^2}{6 \times q}$$

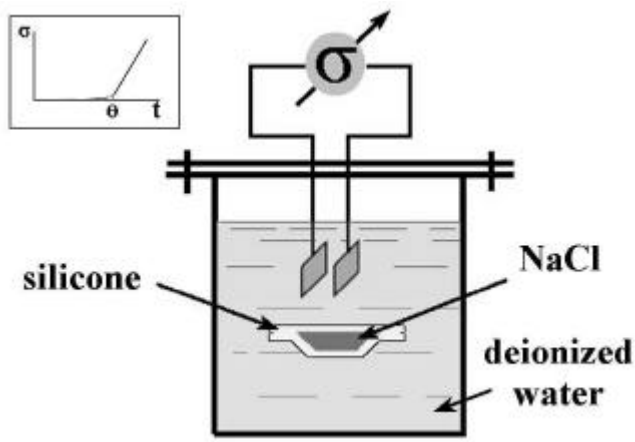

Figure 1. Scheme of the diffusion cell technique. Insert shows expected variance of the water conductance vs. time.

Two types of RTV silicones, SC1 and SC2, have been tested with similar results. Figure 2 shows typical results of these experiments. A sharp increase in water conductivity was found to be due to cracks in the silicone caused by the osmotic pressure in the cells. The cells without cracks withstood more than 1200 hrs of the extraction at 100°C without any noticeable conductivity changes. This indicates that the diffusion coefficient of the NaCl salt in silicones was less than 1.9×10^{-10} cm^2 / s.

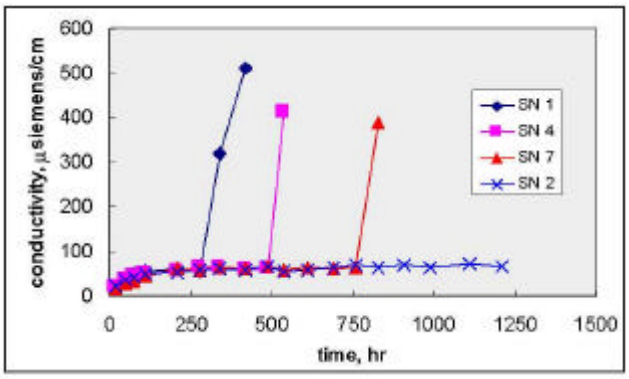

Figure 2. Conductance variance with time of extraction.

The diffusion coefficient varies with temperature according to the Arrhenius law:

$$D = D_o \times \exp\left(-\frac{E_D}{kT}\right)$$

The activation energy E_D can be estimated using the Van Krevelen empirical rule for molecular diffusion in rubber polymers [2]. Assuming that the diameter of the hydrated chlorine ion is d = 6-7 Å and the diffusion process of the hydrated ions in silicone rubbers is similar to the process for simple gases, which depends on the size of the diffusing molecule and is proportional to d^2, the value of activation energy of the diffusion, E_D, can be estimated as $E_D = 0.12\ (d/3.8)^2 = 0.3 – 0.4$ eV. This value is close to the activation energy of $CaCl_2$ diffusion in polyethylene (0.43 eV) reported in [3].

At 121°C the calculated coefficient of diffusion is less than $(3\text{-}4)\times10^{-10}$ cm^2/s. To verify these calculations, an autoclave corrosion test was performed using 15-20 corrosion test structures covered with two types of silicone RTV compounds (thickness 0.3-0.4 mm). Test results showed no difference in corrosion of samples preconditioned in a salt solution and control samples (see Table 1). This means that the chlorine ions did not penetrate during 1000 hours and the coefficient of ion diffusion at 121°C was less than $(4 - 7)\times10^{-11}$ cm^2/s which agrees with previous results. With the activation energy of 0.3-0.4 eV the expected coefficient of diffusion at room temperature would be less than 10^{-12} cm^2/s and the diffusion delay time more than 25 years.

Table 1. Proportion (%) of failures after 1000 hours of autoclave test. (Aluminum corrosion test structures)

Silicone coating	NaCl treatment*	Control**
SC1	8	13
SC2	8	8

* 8 hours, 85°C, 5% NaCl solution;

** 8hours, 85°C, deionized water

To estimate the diffusion coefficient in silicones to volatile chlorine contamination, the autoclave test was performed using 10% and 1% HCl solutions instead of deionized water. Results of these tests are shown in Table 2. All samples failed the test with 10% HCl solution after 8 hours. The first failures during the 1% HCl test occurred after 4 and 16 hours for SC1 and SC2 coatings respectively. Assuming that the diffusion delay time at 121°C is 4-16 hours, the estimation of the coefficient of diffusion for volatile chlorine contamination gives $(4\text{-}9)\times10^{-9}$ cm^2/s which is approximately two orders of magnitude larger than for nonvolatile chlorides. As the size of HCl molecule (2.8 Å) is much less than of hydrated chlorine ion, the activation energy of diffusion is expected to be less than 0.1 eV. With such a small activation energy the diffusion process will only slightly depend on temperature (less than threefold decrease of the diffusion coefficient is expected when temperature is decreased from 121°C to 25°C). This results in more than three orders of magnitude difference between diffusion coefficients for volatile and nonvolatile chlorides at room temperature.

Table 2. Proportion of failures (%) during HCl autoclave test. (Corrosion test structures).

Time in autoclave, hrs	SC1	SC2		
	10% HCl	1% HCl	10% HCl	1% HCl
4	N / P	6	N / P	-
8	100	12	100	-
16	-	85	-	12
32	-	-	-	55
64	-	-	-	80

APPLICATION OF SILICONES

The difference in permeability of silicones for volatile and nonvolatile chlorides should result in the difference of their protection capability in different applications.

Two types of potential chlorine containing contamination are known for electronic parts encapsulated in epoxy plastics: the epoxy compound itself (internal source) and contamination from the printed wiring board, PWB (external source).

Hydrolyzable organic chlorides in epoxy resins are considered a major factor affecting corrosion of aluminum metallization in plastic encapsulated devices. Decomposition of these chlorides in a moisture environment results in release of HCl molecules which are extremely corrosive. As it was shown above, silicones do not prevent permeation of these molecules to the die surface and thus application of silicone coatings before epoxy encapsulation will not improve the moisture resistance of the part. Experiments with corrosion test structures encapsulated in TO-220 packages using epoxy molding compound with a relatively high concentration of hydrolyzable chloride (100 ppm) confirmed these expectations (see Table 3). No significant increase in the median time-to-failure, τ_{50}, for structures with silicone buffer coatings occurred. Both types of structures (with silicone coatings and without coatings) failed within several tens of hours during the autoclave test.

Table 3. Effect of silicone coatings in TO-220 packages on the median time to failure during the autoclave test. (Corrosion test structures, 121°C)

Coating	τ_{50}, hr
Without coating	31
SC1	39
SC2	61

Contamination on PWBs is usually comprised of various nonvolatile carboxylic acids, organic, and inorganic salts. In this case one may expect better moisture resistance for boards covered with silicone coatings. It should be noted that in polyethylene the permeability of different halide ions (from water solutions of NaF, NaCl, NaBr, and NaI) varied less than 5 times [3]. As the diffusion in silicones is of a similar nature we can assume that in silicones different chloride salts would have diffusion coefficients of the same order of magnitude and the diffusion delay time at 121°C would be more than 1000 hours.

Table 4 shows results [4] of the autoclave test performed on transistors encapsulated in SOT-23 plastic micropackages and soldered on a standard PWB (15 transistors on each board). The first board was coated with epoxy conformal coating, the second with silicone conformal coating, and the third board was not covered and used as a reference. At 121°C the calculated moisture diffusion delay time did not exceed several hours for the epoxy coating and several minutes for the silicone coating (coatings thickness was 0.5 - 1 mm). This means that, compared to the times to failure during the autoclave test, neither of the coatings presents a barrier for moisture. A significant increase (more than 2000 hours) in the median time-to-failure for the board, which was covered with silicone, can be explained by a low diffusion of contaminants from the board surface to the die. In the case of epoxy coating the failure rate increased as compared to the uncoated board. Most likely the epoxy resin was an additional source of contamination which penetrated to the die surface relatively easily.

Table 4. Effect of conformal coatings on moisture resistance of transistors soldered on PWB. (Autoclave test).

Coating	τ_{50}, hr
Without coating	1900
Silicone	4100
Epoxy	650

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MEMS Reliability Assurance Activities at JPL

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ABSTRACT

An overview of MEMS reliability assurance and qualification activities at JPL is presented along with a discussion of characterization of MEMS structures implemented on single crystal silicon, polycrystaline silicon, CMOS, and LIGA processes. Additionally, common failure modes and mechanisms affecting MEMS structures, including radiation effects, are discussed. Common reliability and qualification practices contained in the MEMS Reliability Assurance Guideline are also presented.

INTRODUCTION

Micro-Electro-Mechanical Systems (MEMS) devices and structures are a key enabling technology for creating cost-effective, ultra-miniaturized, robust, and functionally focused sensors and actuators for space applications. However, the reliability of MEMS devices for space applications has not been established and qualification requirements have not been clearly defined. Process characterization and determination of active failure mechanisms affecting this new and promising technology are critical to understanding the reliability of MEMS processes and are determining factors in the suitability of this technology for insertion and application in high reliability systems. Here, we present our general approach for understanding MEMS reliability issues and related failure mechanisms. In addition, we present the current MEMS reliability assurance activities at JPL along with a discussion of the "MEMS Reliability Assurance Guideline for Space Application" which was developed to help users and manufacturers of MEMS devices.

MEMS RELIABILITY ACTIVITIES

The approach at JPL for understanding the MEMS reliability issues and related failure mechanisms has been concentrated around three general activities:

- Process characterization
- Environmental test and characterization, and the
- Identification of MEMS related failure modes and mechanisms.

PROCESS CHARACTERIZATION

In order to ensure robust operation, reliability and process test structures designed to provide information on the stability of the manufacturing process, material characteristics and the reliability of the structures, are utilized. It is the analysis of these test structures which will enable the insertion of advanced MEMS devices into designs with a high degree of confidence in their reliability. At JPL, reliability and process monitor test structures have been utilized to understand process stability and help identify common failure modes and mechanisms of the processes and designs under consideration. This activity has been carried out in collaboration with our MEMS Reliability Assurance Alliance partners where the design, fabrication, test and characterization of the structures are performed by various partners and the data shared for the benefit of the whole. Examples of these test structures include, Beam Stubs to indicate process stability, Resonant Beam Structures (Figure 1) to measure beam stiffness, Cantilever Beams used to measure stresses, and Stress/Strain Gauges used to measure residual stresses.

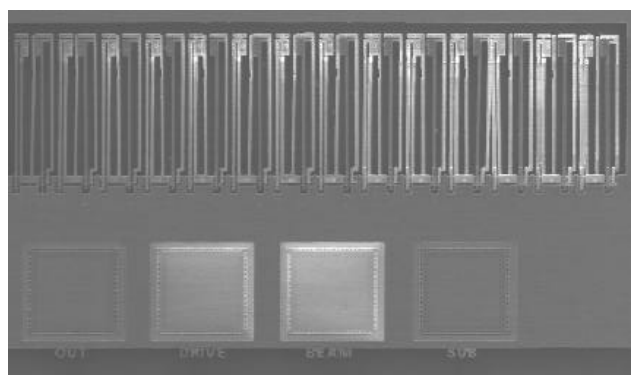

Figure 1. Resonant beam array

ENVIRONMENTAL CHARACTERIZATION

Long term reliability and survival of MEMS devices require effective demonstration of reliable and robust operation in the intended mission environment. The purpose of environmental verification and testing of a device is to demonstrate the quality and reliability of a design and its suitability for the intended application, and to screen for manufacturing workmanship

defects. For space applications, the purpose is also to simulate the launch environment and to qualify the design for launch and in-service conditions.

An environmental verification and testing program typically involve a series of dynamic and thermal tests, which include pyroshock, acoustic noise, acceleration, random and sinusoidal vibrations; and thermal-vacuum, thermal dwell, and thermal cycling. For devices that are sensitive to electromagnetic fields, an electromagnetic compatibility test should be conducted. Evacuated, sealed MEMS packages generally undergo a pressure leak test to ensure the integrity of the packaging. For MEMS devices operating in the radiation field of space, radiation testing is also recommended. This program should be designed to characterize the device for a specific application.

The JPL micro-gyroscope (Figure 2), developed for application in a miniaturized inertial navigation unit, consists of four single crystal silicon square cloverleaves. The structure, 4mm wide by 26 microns thick, is suspended from the substrate by four silicon springs. In the center is a brass post, 4mm tall, which provides gyroscopic motion for the sensor. Two of the four cloverleaves are used as oscillators to move the post along the x axis, while the other two cloverleaves are used as sensors to detect rotational deviations in the path caused by Coriolis forces. The majority of stress upon the device occurs along the spring edges, as they experience the greatest strain from device motion. With the sensitivity of this device largely dependent upon the Q of the structure, and thus its resonant frequency, the structural integrity of the springs is vital to maintaining optimal device performance and is thus an area of great survivability concern.

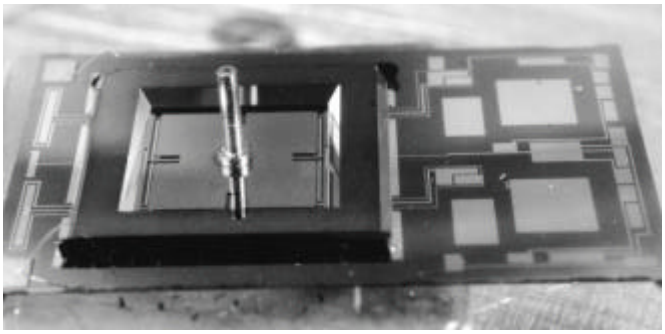

Figure 2. MEMS Microgyro

The devices were exposed to an environmental vibration profile to satisfy the X-33 launch environment [1]. This was equal to a three minute vibration test along the x and z axes using a B&W BW-100C2 vibration bench. On each device, the z axis was subjected to the out-of-plane vibration spectrum, followed by the x plane being exposed to the in-plane vibrations. After each test, the gyroscopes were carefully examined for any signs of structural failure. The vibration profile tests were repeated to verify the suitability of the devices for this launch environment.

MEMS RELIABILITY GUIDELINE

The “MEMS Reliability Assurance Guideline for Space Applications” was developed as an aid to help in the understanding of MEMS reliability and to facilitate the insertion of this technology into high reliability applications [2]. The guideline is structured as an educational guide, offering descriptions of the most common device structures and technologies and the steps required to meet the demands of the space environment. The document is intended as a reference for understanding the various aspects of MEMS with emphasis on device reliability. Material properties, failure mechanisms, processing techniques, device structures, and packaging techniques common to MEMS are addressed in detail. Additionally, design and qualification methodologies provide the reader with the means to develop suitable qualification plans for insertion of MEMS into the space environment.

FAILURE MODES AND MECHANISMS

A critical part of understanding the reliability of any system comes from understanding the possible ways in which the system or its element may fail. In MEMS, there are several failure mechanisms that have been found to be the primary sources of failure within devices. In comparison to electronic circuits, these failure mechanisms are not well understood nor easy to accelerate for life testing. The activities at JPL have concentrated on identifying failure modes and related mechanisms relevant to MEMS structures and processes of interest [3,4]. In this process, the most common failure modes were identified and related to their sources. Some examples of the failure modes include the following:

STICTION

One of the biggest problems in MEMS has been designing structures that can withstand surface interactions[6]. This is due to the fact that, when two polished surfaces come into contact, they tend to adhere to one another. While this fact is often unimportant in macroscopic devices, due to their rough surface features and the common use of lubricants, MEMS surfaces are smooth and lubricants create, rather than mitigate, friction. As a result, when two metallic surfaces come into contact, they form strong primary bonds, which joins the surfaces together. This is analogous to grain boundaries within polycrystalline materials, which have been found to be often stronger than the crystal material itself. However, adhesive boundaries are usually not as strong as grain boundaries, due to the fact that actual area of contact is limited by localized surface roughness and the presence of contaminants, such as gas molecules.

In most MEMS devices, surface contact causes failure. When MEMS surfaces come into contact, the Van der Walls force is strong enough to irrevocably bond the two surfaces (Figure 3). Although some devices, such as micro-switches, are designed to combat this problem through strong actuator networks, most devices must be designed to eliminate any surface interactions, in order to avoid the effects of undesired surface adhesion and stiction.

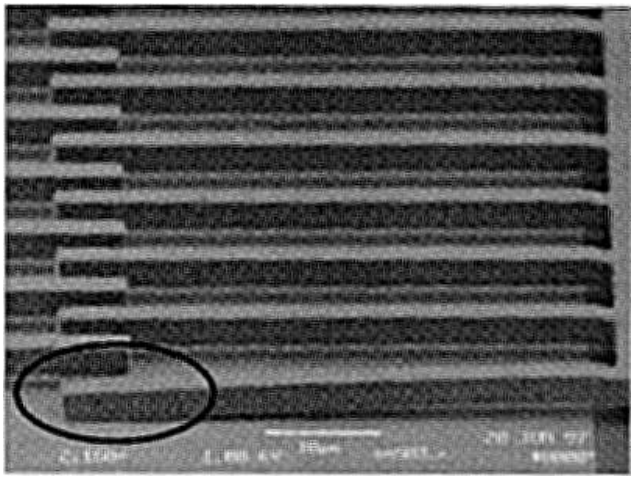

Figure 3. Polysilicon cantilever adhering to substrate

VIBRATION INDUCED FAILURES

Due to the sensitivity and fragile nature of many MEMS structures, external vibrations can have disastrous implications. Either through inducing surface adhesion or through fracturing the device support structures, external vibrations can cause catastrophic failure. Long-term vibration will also contribute to fatigue. For space applications, vibration considerations are important, as devices are subject to large vibrations in the launch process (Figure 4). Identifying the physical limitations of various test structures and devices through environmental test and characterization under controlled conditions has provided a better understanding of this failure mode and it's related mechanisms.

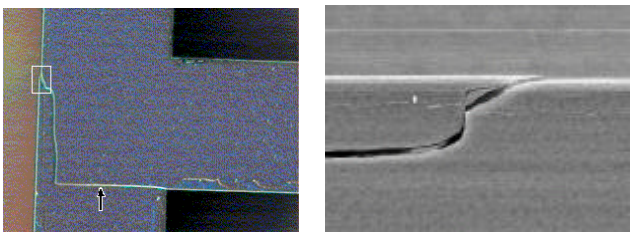

Figure 4. Cracks in single crystal silicon support beams caused by vibrations from a launch test.

RADIATION EFFECTS

While still in its infancy, the field of radiation effects on MEMS is becoming increasingly important. It has long been known that electronic systems are susceptible to radiation, and recent research has raised the possibility that mechanical devices may also be prone to radiation induced damage. Especially sensitive to total ionizing dose (TID) radiation will be devices that have mechanical motion governed by electric fields across insulators, such as electrostatically positioned cantilever beams. The cumulative radiation-induced deposition of charge can cause a shift in electrical behavior of the insulator which, in turn, alters the cantilever deflection.

Since biased insulators are also susceptible to dielectric rupture caused by energetic, charged ions, there is a distinct possibility that these devices will have decreased performance and even catastrophic failure in the space environment due to interactions with galactic cosmic rays (GCRs) and high energy protons.

A further complication is the fact that high levels of radiation can cause bulk lattice damage and make

materials more susceptible to fracture. This effect, called displacement damage, is due to collisions of bombarding radiation particles, such as protons, electrons, neutrons and heavy ions, with lattice atoms in metals and semiconductors. Displacement damage-induced alterations in the Si on which the MEMS is fabricated can also change the electrical characteristics of the Si and hence the behavior of the MEMS.

Of particular importance for establishing radiation hardness assurance (RHA) for MEMS is the fact that microelectronic devices are often integrated on the same chip or substrate as the mechanical portion of the MEMS, and these devices can be much more susceptible to radiation than the microelectromechanical device itself. This is especially important when considering the use of commercial-off-the-shelf (COTS) MEMS in space systems.

Recent work confirming that dielectric layers will trap radiation-induced charged particles, creating a change in electric field [5,7], is illustrated in Figure 7. This permanent field effect will change resonant characteristics and alter the output of many sensors. As shown in Figure 7, test results of a group of surface micro-machined devices exposed to gamma radiation exhibit radiation-induced effects that are different from the usual response of CMOS devices to radiation. In addition, there is a dose rate effect as shown by comparing the two curves for 25 krad irradiations.

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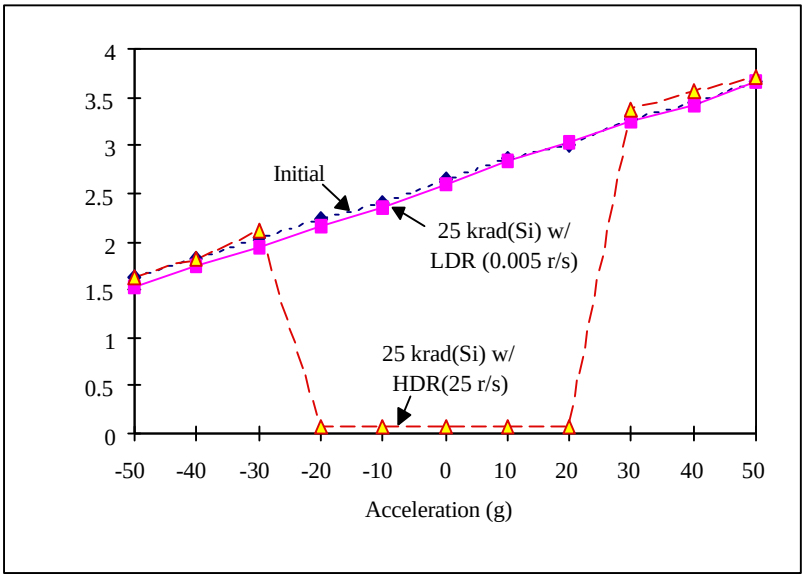

Figure 7. Effect of total ionizing dose on output of an ADXL50 microaccelerometer [6]

Reliability and Qualification of III/V Semiconductor Devices for Space Applications

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ABSTRACT

This paper provides a description of the reliability and qualification issues related to the application of III/V semiconductor devices in critical space systems. A discussion of common failure mechanisms, radiation effects and other reliability concerns is provided along with a discussion of methods for technology qualification for high reliability space applications.

INTRODUCTION

The explosive growth of the WLAN, PCS, DBS, GPS, and cellular telephony markets has resulted in substantial improvements in processing methods, fabrication yield, and overall quality of commercially viable compound semiconductor devices. Many manufacturers now fabricate their standard commercial product line utilizing statistical process control for repeatability and uniformity. This has greatly reduced the infant mortality population without having to impose the traditional high reliability part specification. However, reproducibility of a product does not guarantee reliability in the intended application. For critical space applications where the success or failure of a mission hinges on the lifetime and performance of a single device it is critical that all aspects of the reliability and the various known failure modes and mechanisms be addressed prior to the insertion of the component in the application [1].

Inasmuch as semiconductor manufacturers have reduced the infant mortality population by improving repeatability in fabricating the devices, the long-term failure mechanisms of compound semiconductor devices cannot be assumed to be predictable based on knowledge of silicon technology. The high reliability user must understand that many of the failure mechanisms associated with silicon devices do not apply to GaAs and other compound semiconductors, and new device structures bring new failure mechanisms. Many of the traditional assumptions for mean-time failure rate predictions do not hold for these new devices. Thus, today's high reliability user must be more aware of measurement based predictions of long term failure rate over calculation based predictions.

RELIABILITY AND FAILURE MECHANISMS

Device reliability involves probability statistics, time, and a definition of failure. Given a failure criterion, the most direct way to determine reliability is to submit a large number of samples to actual use conditions and monitor their performance against the failure criteria over time. Since most applications require device lifetimes of many years, this approach is not practical. To acquire device reliability data in a reasonable amount of time, an accelerated life test at high temperatures is used. By exposing the devices to elevated temperatures, it is possible to reduce the time to failure of a component, thereby enabling data to be obtained in a shorter time than would otherwise be required. Such a technique is known as "accelerated testing" and is widely used throughout the semiconductor industry. The rate at which many chemical processes take place is governed by the Arrhenius equation:

$$R = A \exp(-E_a / kT)$$

Where
R = rate of the process
A = a proportional multiplier
E_a = activation energy, a constant
k = Boltzman's constant, 8.6×10^{-5} (eV/K)

This equation has been adopted by the semiconductor industry as a guideline by which the operation of devices under varying temperature conditions can be monitored. Experimental data obtained from life tests at elevated temperatures are processed via the Arrhenius equation to obtain a model of device behavior at normal operating temperatures. Rearranging the Arrhenius equation allows the temperature dependence of component failure to be modeled as follows:

$$\ln(t_2 / t_1) = E_a / k \, (1/T_2 - 1/T_1)$$

Where
$t_{1,2}$ = time to failure
E_a = activation energy in electron volts
T = absolute temperature in Kelvin

FAILURE MODES AND MECHANISMS

Failures in electronic devices can be classified as either catastrophic failures or degradation failures. The exact mechanism which causes the failure is normally dependent on the material structure, processing

methods, application, and stress conditions. Device bias, resultant channel temperature, passivation, and material interactions may all cause or contribute to different failure mechanisms. Furthermore, device handling, especially during wire bonding and die attach and packaging may also cause failures [2].

Some of the most common failure mechanisms include:

Gate-Metal Sinking

The performance of GaAs-based devices relies heavily on the quality of the active channel area of the device. The Schottky gate metal-to-semiconductor interface directly influences the device electrical parameters, such as the drain saturation current and reverse breakdown. The gate structures are based on the industry standard multi-layer Au/Pt/Ti or Au/Pd/Ti on GaAs. Inter-diffusion of gate metal with GaAs results in a reduction of the active channel depth and a change in the effective channel doping. This effect is termed "gate sinking." This process is affected by the surface conditions of the GaAs material at the time of deposition, the deposition parameters, and the choice of deposited materials [3,4].

Ohmic Contact Degradation

The most common system for ohmic contacts is AuGe/Ni, which is alloyed into the GaAs at temperatures in excess of 400°C to provide the necessary low contact resistance (0.1 to 0.5 Ω/mm). A thick Au layer is then deposited on top of the alloyed contacts to provide conduction. This structure, employed at the drain and source contacts, has been shown to degrade at elevated temperatures. The degradation is the result of Ga out-diffusion into the top Au layer and the diffusion of Au into the GaAs causing an increase in the contact resistance. The Ni layer used in the ohmic contact is intended as a Au- and Ga-diffusion barrier. Some other materials such as Cr, Ag, Pt, Ta, and Ti have been used as barrier materials with varying degrees of success. The activation energy associated with ohmic contact degradation varies between 0.5 eV and 1.8 eV. This activation energy may provide reasonable contact life at low operating temperatures (<100°C) but it also indicates rapid deterioration at elevated temperatures [5].

Channel Degradation

Degradation observed in device parameters can sometimes be attributed to changes in the quality and purity of the active channel area and a reduction in the carrier concentration beneath the gate Schottky contact area. These changes have been postulated to be a result of diffusion of dopants out of the channel or diffusion of impurities or defects from the substrate to the channel. Deep level traps have also been postulated to cause similar degradation in MESFETs.

HEMT devices, being strongly dependent on the properties of the interface of the AlGaAs/GaAs heterostructure, can suffer a related failure mechanism. A decrease in electron concentration in the channel, caused by a de-confinement of the 2DEG, was postulated to be the cause of the observed failure mechanism.

HEMT devices can also suffer from metal-diffusion-related mechanisms, which are manifested as channel-related degradation. Lateral diffusion of Al into the gate recess region changes the conduction band discontinuity and consequently the confinement of the channel electrons. Gold diffusion from the ohmic contact into the active channel region under the gate can also cause similar degradation. Lastly, vertical diffusion of Al from the AlGaAs donor layer and Si from the n^+ AlGaAs layer into the channel layer causes an increase in the impurity scattering in the undoped GaAs, thus deteriorating the high electron mobility of the 2DEG [6].

Surface State Effects

The performance of GaAs-based devices depends highly on the quality of the interface between metal and GaAs or the passivation layer (Si_3N_4 or SiO_2) and GaAs. The quality of the interface can depend on the surface cleaning materials and procedures, the deposition method and conditions, and the composition of the passivation layer. The main effect of an increase in surface state density is the lowering of the effective electric field at the drain/gate region, which results in an increase in the depletion region and a change in the breakdown voltage.

Unpassivated devices can be susceptible to surface oxidation and loss of arsenic, which may result in an increase in gate leakage current and a reduction of the breakdown voltage. Devices passivated using SiO_2

may experience surface erosion due to the interaction of SiO_2 with GaAs [7].

Electromigration

The movement of metal atoms along a metallic strip due to momentum exchange with electrons is termed electromigration. Since the mechanism is dependent on momentum transfer from electrons, electromigration is dependent on the temperature and number of electrons. Therefore, this failure mechanism is generally seen in narrow gates and in power devices where the current density is greater than $2x10^5$ A/cm^2, which is normally used as a threshold current density for electromigration to occur. This effect is observed both perpendicular and along the source and drain contact edges and also at the inteconnect of multilevel metallizations.

The metal atoms that migrate along the line tend to accumulate at the grain boundaries. The accumulation of metal at the end of the gate or drain contact can create fingers of metal that can short the device. Material accumulation and void formation perpendicular to the source and drain contacts can cause hillock formation over the gate structure. This may result in shorting the gate to the source or drain which may result in catastrophic failure.

Hot Electron Trapping

Under RF drive, hot electrons are generated near the drain end of the channel where the electrical field is the highest. A few electrons can accumulate sufficient energy to tunnel into the Si_3N_4 passivation to form permanent traps. These traps can result in lower open-channel drain current and transconductance, and higher knee voltage, leakage current, and breakdown voltage. Since the traps are located above the channel, there is usually little change in the dc or small signal parameters near the quiescent point. Further, since the traps are located beside the channel, Schottky-barrier height and the ideality factor often remain constant. This selective change in device characteristics helps distinguish hot-electron effects from thermal or environmental effects [8].

Hydrogen Effects

Degradation in I_{DSS}, V_p, g_m, and output power was observed on GaAs and InP devices tested in hermetically sealed packages or under hydrogen atmosphere. The source of the degradation has been attributed to hydrogen gas desorbed from the package metals (Kovar, plating, etc.). The exact mechanism by which hydrogen degrades the device performance and the path by which hydrogen reaches the active area of a device are not known and have been under investigation [9].

Earlier research on GaAs transistors identified the diffusion of atomic hydrogen directly into the channel area of the device where it neutralizes the silicon donors as the possible mechanism. It is believed that atomic hydrogen diffuses into the GaAs channel and forms Si-H, thereby neutralizing the donors. Experiments have shown that exposure of Si-doped GaAs to RF hydrogen plasma results in neutralization of the Si donors. Infrared spectroscopy data have also given evidence of $(SiAs_3)$As-H complexes.

The neutralization of donors can decrease the carrier concentration in the channel, which, in turn, can decrease the drain current, transconductance, and gain of the device. Hydrogen effects in FETs with either Pt or Pd gate metals have been observed. Recent research has concluded that the diffusion of hydrogen may occur at the Pt side-walls and not at the Au surface of the Au/Pt/Ti gate metal.

Other research on GaAs PHEMT and InP HEMT in a hydrogen atmosphere has shown that the drain current may increase in some cases. This observation has led to the conclusion that the hydrogen diffuses into the semiconductor surface where it is thought to change the metal-semiconductor built-in potential.

Manufacturers and users of GaAs devices used in hermetically sealed packages are currently pursuing an acceptable solution to this problem. Some of the possible solutions include thermal treatment of the packaging materials to reduce the amount of desorbed hydrogen after the seal, the use of hydrogen getter materials in hermetically sealed packages, and the use of barrier materials that do not contain the Pt/Ti or Pd/Ti structure. These solutions have limitations and possible instability problems that must be fully understood prior to implementation in high reliability systems.

QUALIFICATION

Qualification can be defined as the verification that a particular component's design, fabrication, workman-

ship, and application are suitable and adequate to assure the operation and survivability under the required environmental and performance conditions.

Traditional qualification methods require extensive test and characterization of the specific component using a predetermined set of tests and characterization conditions. This approach has been very costly in schedule and expense and typically results in very little interaction between the device manufacturer and the user.

A methodology for qualification based on continual interaction between the device manufacturer and the user is described in this paper. This interaction results in a detailed understanding of the device design, fabrication, and limitations along with the specific application conditions and expected operating environment. The methodology is divided into three main categories; Process Qualification, Product Qualification, and Product Acceptance.

Process Qualification

Is a set of procedures the manufacturer follows to demonstrate the control of the entire process of design and fabrication using a specific technology (MESFET, HEMT, HBT, etc.). It addresses all aspects of the process including the acceptance of starting materials, documentation of procedures, implementation of handling procedures and the establishment of lifetime and failure data for devices fabricated using the process. Since the goal of process qualification is to provide assurance that a particular process is under control and known to produce reliable parts, it needs to be performed only once, although routine monitoring of the production line is standard. It is critical to remember that only the process and basic circuit components are being qualified. No reliability information is obtained for particular component designs.

Although process qualification is intended to qualify a defined fabrication procedure and device family, it must be understood that the technology is constantly evolving, and this technology evolution requires the continual change of fabrication procedures. Thus, strict application of the commonly used phrase, “freezing the production process,” does not apply.

The qualification process also involves a series of tests designed to characterize the technology being qualified. This includes the electrical as well as the reliability characteristics of components fabricated on the line. Some of these tests are performed at wafer level and include the characterization of Process Monitors (PM), and Technology Characterization Vehicles (TCV). Others tests require the mounting of circuits or elements into carriers. All of these tests and the applicable procedures are an integral part of the qualification program and provide valuable reliability and performance data at various stages in the manufacturing process.

Product Qualification

Is the verification that a component will satisfy the design and application requirements under the specified conditions. The information sought after in this approach is design specific and applies to devices fabricated on qualified process lines. This qualification step is composed of Design Verification and Product Characterization.

Design Verification is one of the best ways of reducing engineering costs and improving reliability. Design reviews with the participation of the device manufacturer and the device user is one of the means of accomplishing this verification of model or simulation and layout of the design prior to fabrication.

Product characterization is another important aspect of product qualification. Thermal analysis and test to determine the thermal characteristics of the design, along with ESD sensitivity tests, voltage ramp tests, and temperature ramp tests are all essential in obtaining an understanding of the limitations and characteristics of the design.

Product Acceptance

Although devices may be designed by highly qualified personnel, fabricated on a process qualified production line, and verified through measurements to meet the design goals; parts with poor reliability characteristics still may exist. This may be due to variations in the fabrication process, or material flaws that were undetected, or, as is more often the case, to the device package and stress imposed on the device during packaging. Regardless of the cause, these weak devices must be found and removed before they are integrated into the system. Therefore, manufacturers of high reliability systems require the devices to pass a series of product acceptance screens, whose sole

purpose is to increase the confidence in the reliability of the devices. This step in the qualification methodology is the major difference between space-qualified devices and commercial grade devices.

The level of testing performed under product acceptance is a function of the form of the deliverable. For example, the first level of acceptance testing, called "wafer acceptance test" is performed at the wafer level to assure the uniformity and reliability of the fabrication process through a wafer to wafer comparison. "Lot acceptance test for die" is a second level of testing that provides further reliability information, but only on a sample of the devices because of the difficulty in performing full characterization on non-packaged devices. "Packaged device screen" is performed on 100% of the devices if the deliverable is a packaged product.

RADIATION EFFECTS

The use of microelectronic devices in both civilian and military spacecraft requires that these devices preserve their functionality in the hostile space environment throughout the mission life. An important feature of this environment is the presence of radiation of various types, including that from man-made sources. Unlike other aspects of reliability, radiation is unique and is not a requirement for nearly all other high-reliability applications, such as automotive, medical and terrestrial communications. Thus, because of the distinctive nature of the radiation environment, it is important to understand the effects of radiation on microelectronic devices and circuits used in space systems.

From the radiation point of view, the most important feature of GaAs is the lack of SiO_2 dielectric layers as gate insulators or as isolation insulators. In addition, the very high surface state densities typically found in the AlGaAs/GaAs system pin the Fermi level at the surface and effectively prevent radiation-induced surface inversion and its associated leakage currents from occurring. These differences result in GaAs devices being immune to total dose effects until very high doses are reached where the rare displacement damage events caused by Compton electrons formed from Co^{60} gamma rays finally have an effect. GaAs being a direct band gap material, leads to the minority carrier lifetimes in GaAs being much less than those for Si. Thus, more displacement damage is required to affect GaAs devices that depend on minority carrier lifetime for their successful operation. The best example of this is the increased radiation hardness of GaAs solar cells relative to Si solar cells. In addition, the ability to perform "band gap engineering" in which layers of various materials can be grown on each other with little change in lattice constant, provides increased flexibility in the case of III-V materials relative to Si [10].

Ionizing Radiation Effects

As noted above, GaAs devices in general are relatively immune to total dose effects resulting from the deposition of ionizing energy. This is due to the absence of an oxide that can trap charge and alter the operation of the device. Tests have shown immunity to total dose effects up to 100 Mrad (GaAs). In contrast with the relative immunity of GaAs devices to total-dose effects, transient, high-dose-rate pulses can severely affect these devices. GaAs devices and circuits are typically fabricated on semi-insulating GaAs substrates, which afford a natural isolation between individual transistors on the chip. However, in a transient radiation environment, this attractive feature becomes a liability because the transient photocurrents generated in the substrate are much larger than the transients generated elsewhere in the device. During the ionizing pulse, the large excess carrier densities that are generated in the semi-insulating substrate temporarily cause it to be a good conductor, allowing shunting of the transient photocurrent across transistor sources and drains. Under these conditions, upset levels in GaAs devices can be of the order of 10^{10} rad (GaAs)/s, or even less. Fortunately, these effects can be minimized by properly placing bonding pads and metal interconnects, and using various types of blocking layers [11].

Displacement Damage Effects

As pointed out earlier, GaAs devices are relatively insensitive to displacement damage effects when compared to Si devices. Generally, this is due to the shorter minority carrier lifetimes and higher doping levels found in GaAs devices and circuits. Since the displacement damage introduction into the semiconductor material reduces the minority carrier lifetime, the mobility, and the carrier concentration, device properties that depend on these parameters will be affected by displacement damage. Generally, the longer the lifetime, the higher the mobility, and the

smaller the carrier concentration the more effective displacement damage in altering these parameters. Thus, semiconductor devices with short lifetimes, low mobility, and high carrier concentrations will be relatively immune to displacement damage effects. GaAs has the characteristics of short lifetimes and high mobility. Therefore, we can expect GaAs device to suffer from reduction in mobility and carrier concentration as a result of displacement damage.

Single Event Effects

Studies of charge collection in GaAs devices have shown the charge generated by a single particle can be collected by a greater variety of mechanisms than in Si devices. In GaAs MESFETs, the collection from deep within the device is limited because the recombination rate in GaAs is high and because the diffusion length is short due to small minority carrier lifetimes. However, relative to Si, this is offset by the fact that more regions of the device are sensitive than in the case of a Si MOSFET. In a GaAs MESFET, the source and drain regions are sensitive to upset as well as the gate region. Collection mechanisms for the various regions in the device have been studied, and these include a back channel turn-on mechanism, a bipolar source-drain collection mechanism, and an ion shunt mechanism.

SUMMARY:

The application of compound semiconductor devices in high reliability space systems requires a thorough understanding of the technology's reliability issues and methods for risk mitigation and qualification. Failure mechanisms related to materials, processes, environments and application of the devices must be addressed. Also, interaction between the device manufacturer and user for the understanding and implementation of a meaningful qualification program is essential to assure successful insertion of this technology.

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Jet Propulsion Laboratory Parts Analyses

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Failure analyses (FA), destructive physical analyses (DPA) and part construction analyses (PCA) have been performed on the following part types. For a copy of the report, contact me (phone 818-354-9529, fax 818-393-4559 or e-mail to joan.c.westgate@jpl.nasa.gov) and request the desired document by "Log#".

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FAILURE ANALYSIS				
Log No.	**Manufacturer**	**Date Code**	**Part Type**	**Part Number**
8064	Harris Semiconductor	9516A	8 Input Multiplexer	54HCS151
8076	Harris Semiconductor	9817 (1ea.) 9824 (2ea.)	Quad 2-Input NAND Gate	ACS03KMSR
8077	National Semiconductor	9820A (1 ea.) 9823A (2 ea.)	VME Transceiver	54FCT245FMQB
8078	National Semiconductor	9728B	Octal Buffer	54ACG244FMQB
8082	Harris Semiconductor	None	Radiation Hardened Octal Inverting Tri-State Buffer	ACTS240
DESTRUCTIVE PHYSICAL ANALYSIS				
Log No.	**Manufacturer**	**Date Code**	**Part Type**	**Part Number**
6998	Interpoint	9726	DC-DC Converter	MHF+28512T
7063	ILC Data Device Corp.	9749	1553 BC / RT / MT W / SRAM Hybrid	BU-61582F1-300
8014	CDI	8704	Diode	1N4109
8015	NES	9746	Transistor	2N3700
8016	Harris Semiconductor	9702	Transistor, Logic IC	4013B
8017	SCN	9808	Diode	1N6122
8018	TIX	9749	Operational Amplifier	OP27A
8054	Linear Technology	9831C	12-Bit A / D Converter	LTC1279ISW
8055	Teledyne	9827	Hybrid DC / DC Converter	2301470-1
8075	Omnirel	9750	Voltage Regulator	7915
8076	Harris Semiconductor	9817 (1ea.) 9824 (2 ea.)	Quad 2-Input NAND Gate	ACS03KMSR
8077	National Semiconductor	9820A (1 ea.) 9823A (2 ea.)	VME Transceiver	54FCT245FMQB
8078	National Semiconductor	9728B	Octal Buffer	54ACT244FMQB
8079	McCoy	9815J	40 MHz Crystal Oscillator Hybrid	
8080	Kemet	9828	Ceramic Chip Capacitor	

PART CONSTRUCTION ANALYSIS				
Log No.	**Manufacturer**	**Date Code**	**Part Type**	**Part Number**
6852	Analog Devices, Inc.	9627	3V, CMOS, 500 µA Signal Conditioning ADC	AD7714
6853	Burr-Brown Corporation	9621	24-Bit Delta-Sigma A/D Converter	ADS1210
8039	Hewlett Packard	N/A	Custom Auto Digital Correlator Specrometer	128
8083	Analog Devices, Inc.	AR9821	Dual 16MHz, Rail-to Rail FET Input Amplifier	AD823

Goddard Space Flight Center Parts Analyses

Listed below are the EEE parts analyses completed by the GSFC Parts Analysis Laboratory. The GSFC reports are available to NASA personnel and current NASA contractors by contacting your NASA project office.

CA JOBS						
Job Number	**Manufacturer**	**Date Code**	**Part Type**	**Part Number**	**Result**	**Date**
99558 CA	INTERPOINT	9705	MSA2815S/ES	MSA2815S/ES	P	03/09/99
99728 CA	OPTEK	9823	2N5796U	JANTXV2N5796U	P	03/08/99
FA JOBS						
Job Number	**Manufacturer**	**Date Code**	**Part Type**	**Part Number**	**Result**	**Date**
99699 FA	ANALOG DEVICES	9616	LM108	M38510/10104BGA	F	03/08/99
99271 FA	AEROJET	UNKN	MIXER ASSEMBLY	13350 19-4, SNF05	F	02/25/99
99272 FA	UNKNOWN	UNKN	CONNECTOR ASSEMBLY	UNKNOWN	F	02/16/99
99266 FA	UTMC	9703	MICROCIRCUIT	5962R9654201QXA	F	02/12/99
EC JOBS						
Job Number	**Manufacturer**	**Date Code**	**Part Type**	**Part Number**	**Result**	**Date**
90885 EC	RIGIFLEX TECHNOLOGY	4498	PWBOARD	IM-EP-5208-1	P	01/25/99
90886 EC	ACTION COMPUTER	9841	PWBOARD	LCD11006412-1 REV 4	P	01/25/99
90887 EC	ACTION COMPUTER	9819	PWBOARD	731-001149-1 REV A	p	01/25/99
90888 EC	ACTION COMPUTER	9850	PWBOARD	731-000203-1 REV B	P	01/25/99
90881 EC	ACTION COMPUTER	9839	PWBOARD	731-000218-1 REV A	P	01/22/99
90882 EC	ADVANCED QUICK	5198	PWBOARD	GC2035088-1	F	01/22/99
90878 EC	ALLIED SIGNAL	9852	PWBOARD	3050786-001 REV C	P	01/20/99
90879 EC	ACTION COMPUTER	9842	PWBOARD	731-000215-1	P	01/20/99
90880 EC	ACTION COMPUTER	9842	PWBOARD	LCD11006046 REV F	P	01/20/99
90889 EC	RIGIFLEX TECHNOLOGY	3198	PWBOARD	1309193	F	01/19/99
90883 EC	ADVANCED QUICK	5198	PWBOARD	GC2035089-1	P	01/15/99
90884 EC	SIERRA CIRCUITS	5298	PWBOARD	12083-001 REV A2	F	01/14/99

EC JOBS (Continued)							
Job Number		**Manufacturer**	**Date Code**	**Part Type**	**Part Number**	**Result**	**Date**
90866	EC	YOUNG ELECTRONICS	9733	PWBOARD	8170463-1	P	01/12/99
90874	EC	ALLIED SIGNAL	9846	PWBOARD	3050710-001 REV G	P	01/11/99
90868	EC	YOUNG ELECTRONICS	9747	PWBOARD	8177130-1	P	01/08/99
90869	EC	AMBITECH INC	9802	PWBOARD	8170482-1	P	01/08/99
90877	EC	BF GOODRICH	658	PWBOARD	PB605710403-01 REV B	F	01/08/99
90867	EC	YOUNG ELECTRONICS	9734	PWBOARD	8165944-1	P	01/07/99
90875	EC	CIRTECH INC	3298	PWBOARD	3050814-001 REV A	P	01/07/99
90876	EC	SAS CIRCUITS, INC.	5098	PW BOARD	WB548596-001 REV B	P	01/07/99
90861	EC	YOUNG ELECTRONICS	9730	PWBOARD	8148601-1 REV D	P	01/06/99
90864	EC	YOUNG ELECTRONICS	9731	PWBOARD	8148648-1 REV F	P	01/06/99
90865	EC	YOUNG ELECTRONICS	9731	PWBOARD	8148643-1 REV D	P	01/06/99
90857	EC	YOUNG ELECTRONICS	9720	PWBOARD	8158766-1	P	01/05/99
90862	EC	YOUNG ELECTRONICS	9730	PWBOARD	8148723-1 REV G	P	01/05/99
90863	EC	YOUNG ELECTRONICS	9731	PWBOARD	8148281-1 REV D	P	01/05/99
90850	EC	YOUNG ELECTRONICS	9728	PWBOARD	8147531-1 REV E	P	01/04/99
90854	EC	YOUNG ELECTRONICS	9728	PWBOARD	8148366-1 REV F	P	01/04/99
90860	EC	YOUNG ELECTRONICS	9729	PWBOARD	8165944-1	P	01/04/99