

NASA ELECTRONIC PARTS & PACKAGING (NEPP) PROGRAM

EEE Links

August 2000, Vol. 6 No. 2

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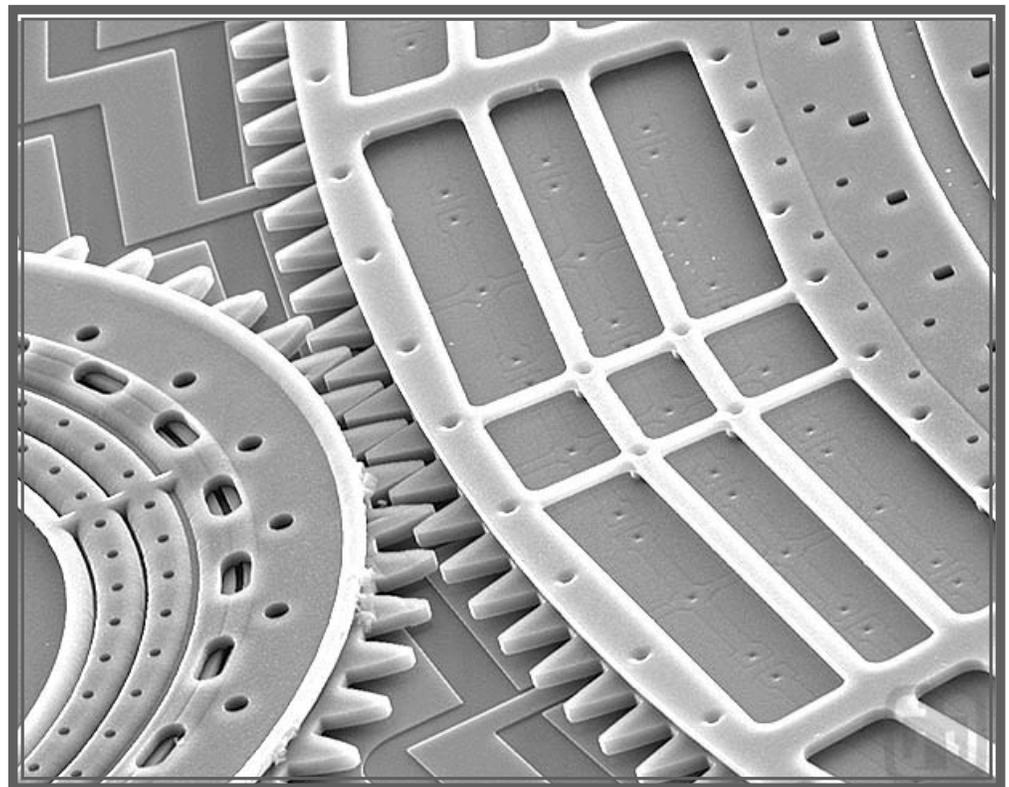
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*COTS MEMS Advances in
Applying Integrated Commercial
Off-The-Shelf Micro Electro-
Mechanical Systems*

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Cover photo shows Precision MEMS Gears/
Courtesy of Sandia National Labs

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Letter from the Editor

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Welcome to the August issue of EEE Links. As mentioned in the last issue of the EEE Links Newsletter, EEE Links is now being published under the auspices of the NASA Electronic Parts and Packaging (NEPP) Program. The NEPP Program is responsible for performing technical assessments, characterizations, and evaluations of newly available and advanced (emerging) electronic parts and packaging, to enable their rapid infusion into NASA's hardware projects, thereby reducing the cost of mission success. These responsibilities all provide for a strong assurance function to develop and relate information regarding parts and packaging capabilities and limitations in order to assist NASA projects in decision making.

This will be the last issue that Esther Bailey our Desk Top Publisher will be working on. Esther has been the Desk Top Publisher for the EEE Links since I took over as Editor back in November 1996. Everyone involved with the EEE Links would like to thank Esther for all her hard work and dedication in putting the EEE Links together. We all wish Esther good luck and much success in her career.

As always, please keep us informed of your questions and needs so that we may be able to serve you better.

EPIMS 2.0

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The EEE Parts Information Management System (EPIMS) provides automated engineering information management for EEE parts reliability, quality assurance, design support, and cost control with an agency-wide, integrated, on-line data system accessible to all NASA projects, contractors, and supporting personnel. The scope of EPIMS includes storage of and access to EEE part selection, availability, qualification,

usage, test, field history, and inventory data; electronic submittal of contractual data requirements; and automated support for parts management tasks for all NASA projects and for the NASA Electronic Parts and Packaging (NEPP) Program.

The EEE Parts Information Management System (EPIMS) version 2.0 was released on March 6, 2000. General information about EPIMS can be found on the EPIMS home page: <http://epims.gsfc.nasa.gov>

An overview of EPIMS 2.0, including a synopsis of the current system functions, can be downloaded in PDF format: http://epims.gsfc.nasa.gov/epims_pub/epims_overview.pdf

New features in this release of EPIMS include:

- The new "Upload a Parts List" function, which provides the capability to upload parts lists via the user's Web browser and check them into the system (the user must have a "Project Data Administrator" role on a project ... see details below).
- An enhanced Parts/Components "Usage Search" functions, that now provides:
 - a "Where-Used Summary", which reports all projects and design items in EPIMS that use any parts matching the search criteria.
 - a "Manufacturer CAGE Summary", which provides a key with the names of all manufacturers whose CAGE codes appear in the search results.
 - "Pop-up" kiosks to display summary information on vendors (by CAGE code), points-of-contact, parts lists, systems, and projects.

Parts Usage searches take noticeably longer than they did in the previous version of EPIMS, because of the additional information that is gathered in the Where-Used Summary -- typical search times are on the order of 20-30 seconds. The increase in search time results from the process of finding all parts information relevant to the search criteria from a database of over 250,000 parts in 6,819 parts lists, and the vendor CAGE information from a table containing over 750,000 CAGE codes.

Help documentation for uploading parts lists is being updated -- the current version is available at: http://epims.gsfc.nasa.gov/epims_pub/help/import_help.html

Notes providing guidance are also displayed during the upload process.

With the release of EPIMS 2.0, the definitions of the user roles "Project User" and "Project Data Administrator" have changed somewhat: the Project User is allowed to add and modify Non-Standard Part Approval Request (NSPAR) data, but cannot upload parts lists. The Project Data Administrator's role is required to upload project parts lists into EPIMS. For definitions of all EPIMS user roles, see: http://epims.gsfc.nasa.gov/epims_pub/help/person_role_help.html.

(Note that there can be more than one Project Data Administrator on a project; also, any PDA can check-in a parts list for any item on their project[s], even if another PDA owned the previous version of that item's parts list ... this rule may be subject to change based on user feedback -- right now it is geared toward simplicity and mutual benevolence among PDA's.)

If you need access to the "Upload a Parts List" function, contact Steve Waterbury at:

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"JPL Chip Scale Packaging Guidelines" Report Being Distributed By Interconnection Technology Research Institute

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A report on the activities and results of the JPL-led Microtype BGA Consortium was recently released by Interconnection Technology Research Institute (ITRI). This group conducted a design of experiments on eleven different Micro Ball Grid Array (BGAs) and Chip Scale Packages (CSPs) assembled on both conventional and microvia Printed Wiring Boards (PWB). The report describes the step-by-step process used by the consortium to select the packages, design the test vehicles, create the design of experiments, assemble the test vehicles, and conduct the evaluations. In ad-

dition to the CSP packages and PWBs, factors such as surface finish, solder paste type, underfills, placement accuracy, thermal cycle profiles, and both single and double sided placement were evaluated. Results of all of the evaluations, conclusions and lessons learned based on the experiences of the consortium team are included. The report is 190 pages with 122 figures many in color, 26 tables, and references. This is the most comprehensive evaluation of the new CSPs and their reliability when assembled on microvia and conventional PWBs that has been conducted to-date. The information in this report will be invaluable to anyone using or considering using these technologies. For information please visit the ITRI web site,

<http://www.ITRI.org>,

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COTS MEMS Advances in Applying Integrated Commercial Off-The-Shelf Micro ElectroMechanical Systems

*August 3 & 4, 2000 • The Claremont Resort & Spa •
Berkeley, CA, USA (Knowledge Foundation)*

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Micro ElectroMechanical Systems (MEMS) is a rapidly growing, exciting technology, slated to reach a significant commercial market in the automobile, space, biological, and mechanical industries early in the new millennium. The innovative conference provided a forum for presentation and discussion of recent advances facilitating development of COTS MEMS relating to various critical applications in, but not limited to these market sectors, and initiated a constructive stimulant and proactive dialogue between industry, government laboratories and academia, about the issues and challenges associated with developing and integrating viable commercial off-the-shelf MEMS products. Program coverage included:

Commercial Off-The-Shelf Micro ElectroMechanical Systems and Devices for Critical Applications

- Single Crystal Silicon Technologies
- Biomedical Microfluidic Systems
- Performance-Oriented Sensor Applications
- Thin-Film Shape-Memory Alloy Technology
- Principles and Applications of a Digital Micromirror Device

Commercial Off-The-Shelf MEMS Software Packages

- Methodologies for Rapid MEMS Device Development and Package Design

Micro ElectroMechanical Integration Strategies

- New Directions in Integrated Microsystems Technology

- COTS MEMS in Atmospheric Observing Systems
- Microfluidic and MEMS Platforms for Diagnostic and Drug Discovery Technologies

Reliability and Quality Assurance of COTS MEMS

- Reliability Issues of COTS MEMS for Automobiles, Medical Devices and Aerospace Applications
- Design for Reliability of MEMS for Lightwave Telecommunications
- Test Development Principles for MEMS Devices
- Hermetic Packaging of COTS MEMS Market Opportunities and Applications
- Silicon Carbide-Based Microsystems for Harsh Environments
- A Consortium Approach to Accelerating MEMS Commercialization

As many governments are investing in the development of MEMS, a significant market awaits those industries that are able to capitalize on this urgent need for off-the-shelf sensor devices. This conference provided a one of a kind opportunity to hear from many of the industry's leading experts working to rapidly and cost-effectively bring MEMS products to market. The comprehensive program agenda included presentations from the Leading Developers of MEMS Technologies for Commercial Off-the-Shelf Devices:

- Alberta Microelectronic Corp.
- ACLARA BioSciences, Inc.
- Air Force Research Laboratory
- Bell Labs, Lucent Technologies
- Berkeley Sensor & Actuator Center, University of California at Berkeley
- Cepheid
- DARPA
- Endevco
- Glennan Microsystems Initiative
- IntelliSense Corporation
- Jet Propulsion Laboratory
- Lucas NovaSensor, Inc.
- MEMSCAP S.A.
- Microelectronics & Computer Technology Corp.
- Microcosm Technologies, Inc.
- Motorola

- National Center for Atmospheric Research
- Texas Instruments
- TiNi Alloy Company

More details on the conference:

<http://www.knowledgefoundation.com/cotsmems.html> or contact the Program Chair.

NEPP News

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The First Annual NEPP Conference was a success!

Eighty-six attended the Electronic Parts and Packaging for Space and Aeronautic Applications Advanced Technology Workshop co-sponsored by the NEPP Program and the International Microelectronics and Packaging Society (IMAPS) held May 22-24, in Washington, D.C. The ATW included the following sessions:

- High Density Interconnect Microelectronics
- Radiation Characterization
- Photonics/Optoelectronics
- Reliability of Electronics under Extreme Environments
- MEMS and Sensors

NASA attendees included representatives from the Jet Propulsion Laboratory, Goddard Space Flight Center, Glen Research Center, Langley Research Center, Marshall Space Flight Center, and Johnson Space Center.

- The NEPP Electronic Radiation Characterization Project (ERC) **Homepage has been launched** at <http://erc.gsfc.nasa.gov>
- Research partially funded by NEPP was presented in an article titled, "Changes in Luminescence Emission Induced by Proton Irradiation: InGaAs/GaAs Quantum Wells and Quantum Dots", by R. Leon, G. M. Swift, B. Magness, W. A. Taylor, Y. S. Tang, K. L. Wang, P. Dowd, and Y. H. Zhang, was published in *Applied Physics Letters*, Vol. 76, No. 15, p. 2071 (2000).
- Professor Michael Wnuk from the University of Wisconsin, Milwaukee, and Dr. Rajeshuni Rame-

sham, a NEPP Research Task Manager, have co-authored a paper titled "Physics and Mechanics Related to Adhesion and Bonding Intended for Space Applications", which has been accepted for presentation at the 33rd Solid Mechanics Conference, Zakapone (Poland), September 5-9, 2000.

- Dr. Rosa Leon, a NEPP Research Task Manager, gave an invited talk at the Spring meeting of the Materials Research Society, San Francisco, April 24-28, titled, "Interactions, Interdiffusion and Segregation in Quantum Dot Ensembles". Dr. Ghaffarian, a NEPP Research Task Manager, and Dr. Namsoo Kim, of Boeing, co-authored a paper which was presented at the 50th Electronic Components & Technology Conference held in Las Vegas in May 21-24. The presentation was titled "CSP Assembly Reliability and Effects of Underfill and Double-sided Population". The presentation included the environmental test results performed at JPL and Boeing under the JPL-led Microtype BGA Consortium.
- Dr. Ghaffarian, a NEPP Research Task Manager, submitted the final version (5th draft) of a chapter for an electronic handbook to be published by Chapman-Hall Book Company. The book is being edited by Dr. Karl Puttlitz and Dr. Paul Totta of IBM. The chapter, titled "Chip Scale Package (CSP) Assembly Reliability", covers a review of key reliability parameters for CSP technology and presents reliability data generated under the Consortium organized by the Jet Propulsion Laboratory Quality Assurance Office and funded by the NEPP Program.

Parts and Packaging Events

Advances in Applying Integrated Commercial Off-The-Shelf Micro ElectroMechanical Systems, August 3 & 4, 2000 • The Claremont Resort & Spa • Berkeley, CA, USA. See article in this edition of EEE Links for details about this conference.

Newly Developed Low Voltage, Radiation Hardened, Space Level Components for use on NASA Projects

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JPL Office 514, the electronic parts engineering, has been working with the manufacturers of electronic components to develop parts that would meet the requirements of new NASA missions such as the X2000, STM, and others. Some of those requirements are: low power/low voltage operation (3.3V +/- 10%), high radiation tolerance (total dose levels of 100krad and higher), high reliability (QML V or equivalent) and long mission life (up to 15 years). The intent of this article is to advise the NASA user community as to the progress that has been made towards that goal. The following products are now being built for our projects and they are expected to be available as standard catalog items very soon.

Crystal Oscillators

High reliability, radiation hardened crystal oscillators that would operate at 3.3V are being built by Q-Tech Corporation. The parts will be available in 20-pin ceramic flatpacks. The manufacturer intends to add the 3.3V product line to their standard space level offering in frequencies upto around 100MHz. Contact Q-Tech for more details.

RS422 Driver/Receiver Pair

Intersil is building 3.3V, radiation hardened, high reliability version of RS422 driver and receiver pair. The new parts will be labeled HSX-26CLV31RH-Y and HSX-26CLV32RH-Y* and will be available as standard space level parts. Refer to Intersil's website or contact them directly for cost, schedule and other information.

- X denotes the package type (1 for DIP, 9 for flat-pack, etc.) and Y the QML level (-Q for QMLV, -8 for QMLQ, etc.).

There are other evaluations in progress which will be reported on as the products come to fruition.

Living With COTS: Tracking Industry's Roadmaps

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In order to meet the needs of NASA's electronic designers, parts engineers and procurement offices have to stay in touch with conditions and issues which impact the quality, availability and price of parts that they will be asked to evaluate or buy for use in flight hardware. The political, economic and technological conditions today make it unattractive to most parts and assemblies producers to service the high reliability, low volume users such as NASA and the military; volume being the more significant discriminator. NASA needs to understand this landscape in order to make good short and long term decisions about how it will get the materials it needs for the medium to fast cycle programs it is funding.

The IPC, the electronics interconnection and packaging trade organization, held their Technology Market Research Council meeting in Washington, DC in June. The topic was: The Impact of Telecommunications on the PWB and EMS Industries (EMS = electronic manufacturing services). In today's economy, there hardly could have been another focus. Telecommunications technologies are the ones which are driving the most aggressive changes in electronic packaging, namely miniaturization and high volume manufacturability. From these pressures comes new underfill materials, high temperature processes and boards which can stand up to those temperatures, embedded passives, ultrafine linewidths, manufacturing processes which use high fidelity vision such as X-ray for alignment control and more dependence on the evolution of systems on a chip.

Dr. Peter Cochrane, Chief Technologist for British Telecom, made a convincing case for the ultimate dominance of wireless technology wherever we'll need to communicate a bit of information. Though fiber networks will provide the mainframe of the network centers, Dr. Cochrane predicted that we as individuals will increasingly interface with wireless networks. Efficient routing by computers and low power, hand held terminals (cell phones or the like) will drive this. Microsoft's launch of a location inde-

pendent computing identity reduces the need to own large boxes which run and store applications and focuses functionality of the portable unit on communications functions and reading and writing data. The original equipment manufacturers (OEM) understand this and are moving fiber and wireless based technology manufacturing as fast as they can. Large system manufacturing will be dominated by breadbox to garage sized switching stations.

Edward Sokolowski showed Nortel's technology roadmap for interconnection technology starting with the current 2.5 Gb/s electrical backplane. Nortel sees 10 Gb/s in 2001, jitter minimization through SiGe chips in 2002, MEMS photonic crossconnects and impedance controlled vias in 2003, 40 Gb/s PCB traces in 2004 and optical backplanes in 2005. In and among these are 10 Gb/s embedded shielded microvia stripline technology, thermally tuned lasers and tuned DWDM, all-optical lambda converter and 40 Gb/s MEMS crosspoint technology. Some of these technologies are emerging right now making these estimates plausible. Mr. Sokolowski reminded the audience that the limitation on the bandwidth performance of optical networks will track with the evolution of the electronics. The inability of the electronics to fully realize the bandwidth potential of the fiber will drive their replacement by optical circuitry. The development of these optical and electrical components is occurring simultaneously.

Cell phones were often used for illustrating the fast pace of miniaturization technology development and the insatiable market for portable electronics. Mitsubishi's 0207 cell phone is 43% the weight of Nokia's 1997 model 6110. Application specific integrated circuits (ASICs) and chip scale packages (CSP's) can largely take the credit for this. Other technologies which will continue this "growth" in miniaturization are laser drilling and multilayered substrates, BGA MCM's and flip chip. Advances in battery technology have not kept pace with semiconductor and packaging improvements and was seen as the area most likely to be the future developmental bottleneck.

Several market analyses were presented. The trends continue to go up in all electronics sectors; aerospace and military being the slowest in growth potential. A startling find was that PC boards have become a commodity rather than a value added product. It is

no longer seen as an engineered product with a unique collection of features. One presenter suggested the need for more modularity at the assembly level which will create some of this commodity character to overtake assembled hardware as well. The majority of the profits in the supply chain, below the original equipment manufacturer (OEM) level, are being realized by the board assemblers who are offering miniaturization and ASIC based solutions.

While OEM's are divesting themselves of in-house assembly facilities, they are feeling the delays associated with sharing the supplies with the rest of the industry. Orders for raw materials such as glass and epoxy are becoming backlogged while components continue to be a production bottleneck. The reaction is that OEMs are returning to captive relationships with independent assembly houses. Infrastructure is being put into place where volume throughput is not high enough, preferred commodity providers are being identified and commodity orders are being placed years in advance. Lead times associated with part shortages is seen as a significant concern going forward. News just in indicates that some component manufactures are simply refusing to sell to government customers at all.

Japan continues to push the technology and dominate volume production; however, the IPC predicts that in a couple of years, China will be producing the same volume as Japan does. The market volume is so high though that this will not eliminate continued upward production trends for U.S. production.

The IPC is condoning efforts to find lead-free alternatives to tin-lead solder. Though manufacturers believe the risks associated with the small amounts of lead in the solders they use are miniscule, they are accepting that the public will increasingly reject products with any amount of lead in them. Manufacturers who are using lead-free solders are labeling their products as "green", or environmentally friendly, and this is becoming a marketable feature. Alternative materials being looked at are: SnAgCu, SnCu, SnAgBi, SnAgBiCu, SnAgBiCuGe, SnBi, SnZn, and SnAg.

The concerns of commercial industry will be the concerns of NASA when we use COTS. These concerns are also indicators for part availability in the high-rel

sector as well. More work is planned through the NEPP program to reduce the roadmapping data produced by electronic industry to extract strong technology and availability trends which will impact the spaceflight industry.

Programmable Logic Application Notes

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This column will be provided each quarter as a source for reliability, radiation results, NASA capabilities, and other information on programmable logic devices and related applications. This quarter will start a series of notes concentrating on analysis techniques with this issue's section discussing worst-case analysis requirements. If you have information that you would like to submit or an area you would like discussed or researched, please give me a call or e-mail.

2000 MAPLD Conference

September 26-28, 2000
Kossiakoff Conference Center
JHU/Applied Physics Laboratory
Laurel, Maryland

The 3rd annual Military and Aerospace Applications of Programmable Devices and Technologies Conference will address devices, technologies, usage, reliability, fault tolerance, radiation susceptibility, and applications of programmable devices and adaptive computing systems in military and aerospace systems. The program will consist of approximately 60 oral and poster technical presentations and 20 industrial exhibits. The majority of the conference is open to US and foreign participation and is unclassified. There will be one classified session at the secret level, for U.S. citizens only. For conference information, please see Programmable Technologies Web Site (<http://rk.gsfc.nasa.gov>).

At the time of this printing, the oral presentations will have been selected. Submissions for poster papers and industrial exhibits will still be accepted and authors may submit abstracts.

The invited speaker program features an excellent set of talks. This includes Eldon Hall, a designer of the Apollo Guidance Computer (AGC), the keynote address by space historian Henry Spencer, and Tom Jones, NASA astronaut. Dr. Massengill of Vanderbilt University will discuss emerging technologies and J. Kinnison of JHU/APL will be our AIAA invited speaker. More information and abstracts are available at: <http://rk.gsfc.nasa.gov/richcontent/MAPLDCon00/InvitedSpeakers00.html>

Presenters this year will have the option of having their work, subject to peer review, published in the AIAA **Journal of Spacecraft and Rockets**. The special editor is Dr. Tanya Vladimirova of the University of Surrey.

We also wish to acknowledge our new conference sponsor, the IEEE Aerospace & Electronic Systems Society.

Registration for the conference is now open. Please see: <http://rk.gsfc.nasa.gov/richcontent/MAPLDCon00/Reg/Registration.html>.

What's New?

A large amount of data, reports, papers, application notes, and conference information are being stored on our companion Programmables Technology www site, <http://rk.gsfc.nasa.gov>. In order to make it easier to keep readers up-to-date, all new additions to the site are being listed, in chronological order on our "What's New" page. This can be found at: http://rk.gsfc.nasa.gov/What's_New.htm

Analysis Techniques

The following application note on worst-case analysis requirements was contributed by Dr. R. L. Barto of Spacecraft Digital Electronics. In 1991 Dr. Barto received the NASA Public Service Medal for the Galileo AACCS design. This note is the first in a series on analysis techniques.

An Outline of Worst-Case Analysis Requirements for Digital Electronics

Every designer's goal is mission success: the production of a correctly functioning system. One of the keys to achieving that goal is the worst-case analysis (WCA). A detailed WCA, if performed during the

design phase, can find design problems that may not be found during the test phase. Timing errors, interface margin problems, and other design flaws may manifest themselves only under limited operating conditions that are not present during test, such as temperature extremes, age, or radiation, or in limited operating modes that are not exercised in test. The only way to guarantee that no design flaws exist in a circuit is to carefully analyze the circuit and prove their absence.

The purpose of a WCA is to prove the design will function as expected during its mission. The spirit of analysis is proof: all circuits are considered guilty of design flaws until proven innocent. The following is an outline of WCA requirements, which introduces the circuit design items that must be reviewed as part of the WCA.

1. PART PARAMETERS AND DERATINGS

Data book part parameters often do not match the part's intended operating environment. Each parameter must be derated from the data book value for the intended environment to compensate for the effects of temperature, age, voltage, and radiation where applicable. A derating for excess load capacitance must also be given when high capacitive loads are driven. This information forms the database on which the analysis is performed.

2. TIMING ANALYSIS

A complete timing analysis will contain, for each clocked device in the system, a proof that all of the derated timing parameters are met:

- 2.1 Set-up and hold times at all clocked inputs, including the data inputs, synchronous sets, clears, and enables, and any inputs for which a set-up or hold time is specified;
- 2.2 Pulse widths of clocks, and asynchronous set, clear, and load inputs, and any input for which a pulse width is specified;
- 2.3 Set and clear recovery time -- the set-up time from the release of an asynchronous set or clear until the next clock edge.

In addition, all clock inputs and asynchronous inputs such as sets, clears, and loads must be shown to be free from both static (010 or 101) and dynamic (001011 or 110100) hazards.

- 2.4 CMOS Parallel Clocking
- 2.5 Timing of Analog Circuitry
- 2.6 Minimum Propagation Delays
- 2.7 Calculation of Pulse Shortening
- 2.8 Consideration of Transition Times in Delay Calculations

3. GATE OUTPUT LOADING

The analysis must show that no gate output drive capacities have been exceeded. Unusually high output drive currents may affect output voltage levels and propagation delays, and may cause thermal problems resulting in part damage.

4. INTERFACE MARGINS

The interface margin analysis must show that all of the gates have their input logic level thresholds met. For gates within the same family, and assuming no unusual loading, this analysis is only a formality. However, where different families, or digital and analog parts, interface, each different class of interfaces must be analyzed. Decreased interface margins cause circuits to be more susceptible to noise and can affect the operation of some parts.

- 4.1 CMOS to Non-CMOS Interfaces
- 4.2 Variation of CMOS I_{CC} With Input Voltage Level
- 4.3 Input Transition Times
- 4.4 Input Requirements of Analog Devices
- 4.5 Driving Mixtures of TTL and CMOS

5. STATE MACHINE TRANSITIONS

State machines must be analyzed to assure that they will not exhibit anomalous behavior, such as system lock-up.

- 5.1 Unused States
- 5.2 Simultaneous Assertion of Flip-Flop Sets and Clears
- 5.3 Asynchronous State Machines
- 5.4 Reset Conditions and Homing Sequences

6. ASYNCHRONOUS INTERFACES

An asynchronous interface is one for which the set-up and hold times of incoming signals at receiving latches or flip-flops cannot be guaranteed. An example is data generated on one clock being transferred to flip-flops on a second clock having no synchronous relationship to the first, even if the two clocks have the same frequency. The analysis must show either that asynchronous signals are properly synchronized to the appropriate clock or that the circuitry receiving asynchronous signals will function correctly if set-up and hold times are not met.

7. RESET CONDITIONS AND GENERATION

All circuitry must be shown to be placed into a known state during reset. The width of the reset pulse should be longer than the longest reset T_{PW} specified for any of the parts. In general, a reset should be treated as an asynchronous input to a sequential circuit and should be synchronized with the clock used by the devices being reset.

- 7.1 Reset Duration vs. Supply Voltage Level and Ramp-up Timing
- 7.2 Unintended Execution of External Commands on Power-up and After Reset
- 7.3 Synchronous Resets and Oscillator Start-up Time
- 7.4 Reset Release Timing

8. PART SAFETY CONDITIONS

The analysis must prove that the circuit is designed to prevent its parts from being damaged. Part damage can result from a design which does not protect ESD sensitive parts, allows interfaces between incompatible parts families, or fails to provide for other requirements of the parts.

- 8.1 Protection of ESD Sensitive Parts
- 8.2 Input Voltage Levels
- 8.3 Tri-State Output Overlap
- 8.4 Floating Inputs
- 8.5 Use of Internal IC Protection Diodes
- 8.6 Use of Parts Outside of Manufacturers' Recommendations

9. CROSS-STRAP SIGNALS BETWEEN REDUNDANT MODULES

The requirements for cross-strap signals can be derived from their basic purpose, that of fault isolation. It must therefore be shown that isolation between boxes is actually achieved.

- 9.1 Undesirable Powering of Modules via Cross-Strap Circuitry
- 9.2 Sharing of Cross-Strap Gates

10. CIRCUIT INTERCONNECTIONS

The analysis must show that circuit interconnection requirements are met from the standpoint of signal quality as affected by edge rates, loading, and noise. Circuits of interest here include connections on and between PC boards and with peripheral units.

- 10.1 Termination of High Edge-Rate Signals
- 10.2 Off-Board Connections of Edge-Sensitive Inputs
- 10.3 Edge Rates of Harness Signals
- 10.4 Calculation of Harness Noise Threat Model
- 10.5 Noise Susceptibility Analysis of Input Circuitry
- 10.6 Drivers and Receivers for Off-board Signals

11. BYPASS CAPACITANCE ANALYSIS

The analysis must show that the amount of on-board bulk and bypass capacitance is appropriate for the circuitry. The analysis will consider power supply line inductance, circuit operating frequency, and component current requirements. The choice of capacitors must be shown appropriate based on their frequency response.

Conclusion

A complete WCA contains an analysis of many circuit requirements that will be difficult or impossible to prove met by test. The correct time to perform the analysis is during the design phase. Putting off the analysis until after the design is completed invites costly redesign and system failure that could be avoided by doing the analysis before the hardware is built.

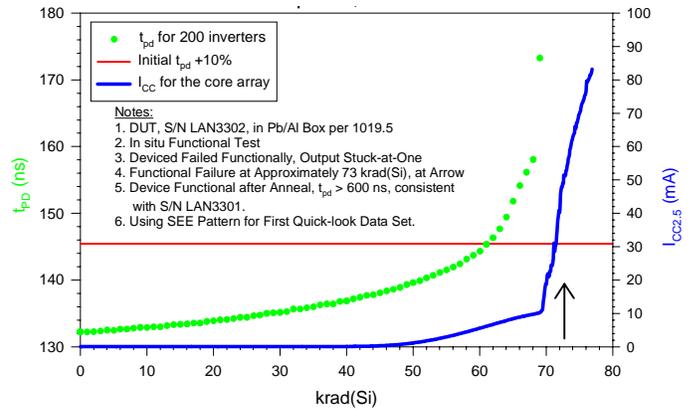
Nonvolatile, Reprogrammable FPGA Data

Two Actel A500K050 prototype FPGAs were subjected to a total dose test. These devices, packaged in PQFP208 packages, were irradiated at 1 krad(Si)/Hour at the NASA/GSFC total dose facility. The test pattern for this first look was primarily designed for an SEE evaluation. A serial string of inverters was included in the design to enable delta t_{PD} measurements for an initial assessment of total dose performance. An initial SEE evaluation should be completed by press time for this column.

The A500K050 is the smallest device in this series, with 43,000 "typical gates." The data sheet shows the A500K510 as the largest with 410,000 "typical gates." These devices are reprogrammable and nonvolatile. Flash technology is utilized for the switch and no boot device is required. The data sheet claims the device is "live at power-up." The device implements the TRST* pin as part of the IEEE 1149.1 JTAG TAP controller. The logic array of this device utilizes a 2.5 VDC power supply. A bias voltage of 3.3 VDC was also supplied.

The first device, S/N LAN3301, was used to obtain an initial understanding of the characteristics of this new technology. Several results came from this first run. First, ICC, by itself, was not a good predictor of performance. Secondly, there was a significant degradation in t_{PD} as a function of total dose. After the first run, it was found that t_{PD} increased by several times. Consequently, the instrumentation plan for S/N LAN3302 was developed. For this test, in situ measurements were made of ICC, functionality (using the inverter string), and t_{PD} . ICC was monitored at 5 minute intervals with an over current protection circuit constantly enabled. Functionality and t_{PD} was measured at 1 krad(Si) intervals. After completion of the test, a full functional test was made in the lab.

The data from the S/N LAN3302 run is shown in the figure above. At the completion of the run, functional failure was found, at a modest current level. The chart includes a reference line at a level corresponding to a +10% increase in t_{PD} from the initial value. This level is frequently the limit used by analysts for delta propagation delay and thus makes a convenient reference point. It is seen that this limit is exceeded at the moderately low level of ICC of approximately 6 mA.



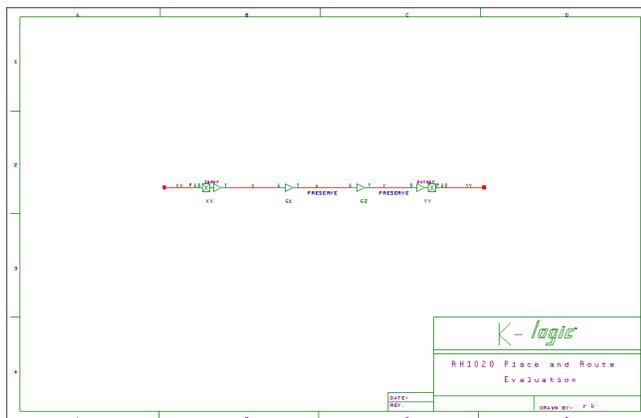
P&R and Propagation Delay

Previous application notes have discussed the use of local, high-skew clocks for elements such as shift registers and parallel counters. In general, one should use the global, low-skew clocks that the manufacturer provides. In some cases, however, that is either not possible or not desirable. For example, a low power circuit may not wish to drive the entire global clock network for only a few flip-flops. In other cases, the system design may require more clocks than are present in the device being used. There are reliable techniques for designing with high-skew clocks such as opposite edge clocking for edge-triggered flip-flops and use of a two-phase non-overlapping clock for latches. Unfortunately, many designs still utilize a single edge, single-phase clock and a high-skew route.

The term "sequentially adjacent" refers to two flip-flops clocked by the same clock that are connected by combinational logic and routing. If they are triggered on the same edge, then it is required, for reliable operation, that the minimum propagation delay ($t_{CLK \rightarrow Q} + t_{ROUTE}$) be greater than the maximum clock skew and t_H . Although a "wire" on a schematic drawing appears as a wire, when implemented in an FPGA there can be considerable delay transporting a signal across a wire. This delay is dependent on the placement and routing and the particular microcircuit. Note that for Actel FPGAs, for example, the resistance of an antifuse will vary from microcircuit to microcircuit and must be treated as a random variable.

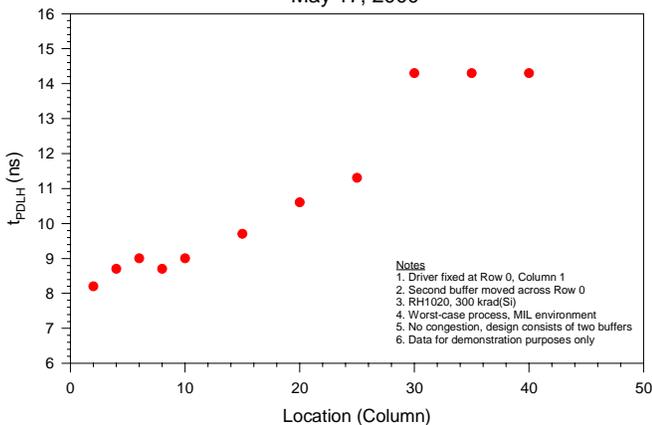
As a demonstration for the effects of placement and routing, a simple design consisting of two buffers was analyzed. The RH1020 was used and the conditions were set to worst-case, 300 krad(Si), and MIL standard voltage and temperature. The RH1020 consists of 14 rows and 44 columns. The time measured, t_{PDLH} , was

from the input of the first buffer to the input of the second one. The preserve property was used so that the Combiner would not eliminate any of the logic elements. The first buffer, G1, was fixed at Row 0, Column 1. The second buffer, G2, was varied in position. For each change in position, the place and route tools were run with standard settings. The times reported are in a sense "best-case" since the virtually empty chip will ensure that there was no routing congestion and all routing segments were available. The numbers shown here are for demonstration purposes only. For an actual design, post-layout extracted parameters should be used.



The first run moved buffer G2 down Row 0. The effects on propagation delay are shown in the chart below. While the data is clearly not monotonic, it is seen that in general the delays increase as the buffers are separated, as would be expected. Additionally, once a certain distance is exceeded, there is no further increase in propagation delay. By moving the location of the buffer G2, the propagation delay can increase by almost a factor of 2.

RH1020 P&R Analysis
Effect of Row Position on Prop Delay
May 17, 2000

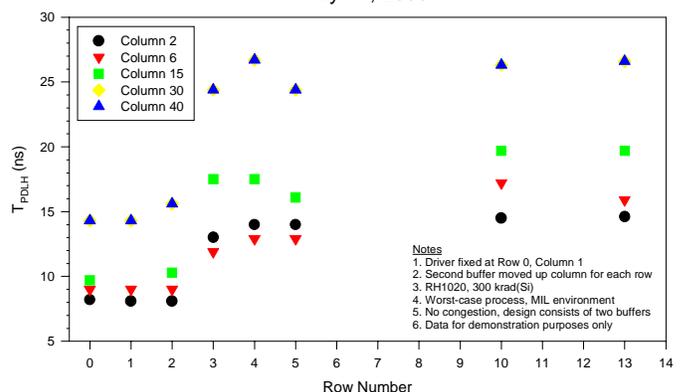


Next, the effects of placing a buffer in different rows was examined. That is, for a fixed column difference, how does the row selection effect propagation delay? Again, the buffer G1 was fixed at Row 0, Column 1. Individual sets of runs were made with the buffer G2 moving up Columns 2, 6, 15, 30, and 40. The results are shown in the chart below. The data for columns 30 and 40 were identical.

Again, we see that the data in general increases, although not monotonically for the points analyzed. The data also shows the sensitivity in moving the receiving buffer in the Y direction - increasing Row number. After two rows, there is a step increase in propagation delay. Beyond that, there is an increase in propagation delay although the curve appears "saturated." From corner to corner, we can see an increase in delay by approximately a factor of 4. Even for relatively small distances, the combination of Row and Column position can result in a doubling of the propagation delay.

The "wire" drawn on the schematic does not appear as a wire electrically, in this FPGA.

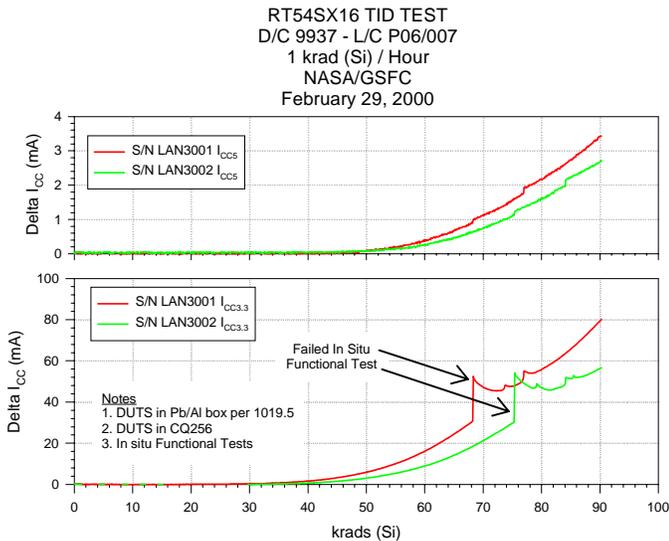
RH1020 P&R Analysis
Effect of Column Position on Prop Delay
May 17, 2000



In Situ Functional Testing

For many of the older FPGA technologies, *in situ* monitoring of device current was in general a good indicator of the device's state. With some of the more modern technologies, as was the case with the A500K050 discussed above, we saw that functional failure and parametric shifts could occur without a large increase in supply current. The RAMTRON FRAM parallel RAMs also exhibited this property.

The chart below shows data for two production RT54SX16's, L/C P006. We see that at moderate current levels, failure was detected by our *in situ* functional monitor. The coverage for this test was high. Functional tests were run every krad(Si) of exposure.



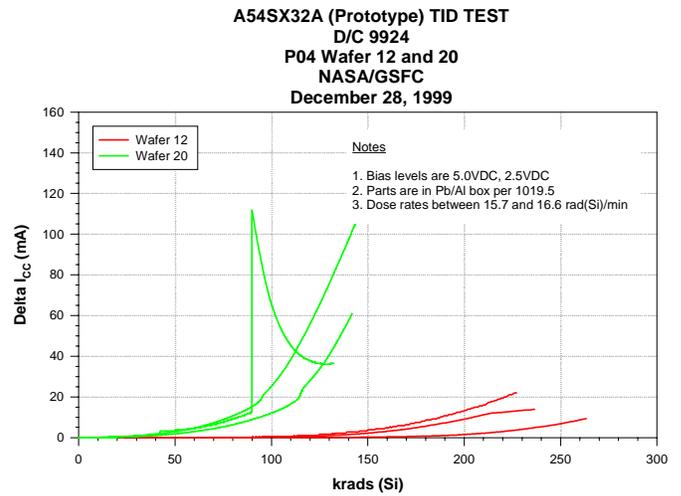
Clearly, one should never extrapolate the results of total dose radiation tests.

SX-A Technology

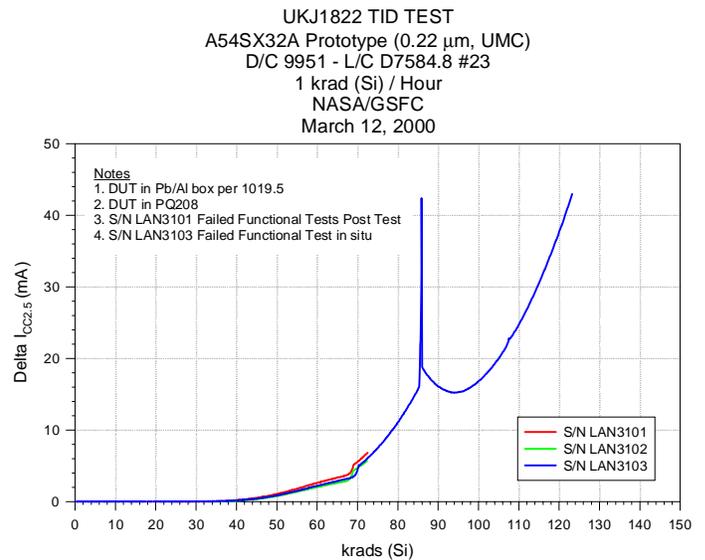
The SX technology consisted of "RT" parts produced at 0.6 μm at the MEC foundry and commercial grade parts fabricated at 0.35 μm technology at the Chartered Semiconductor foundry. The SX-A series devices are produced at 0.25 μm at MEC and at 0.22 μm at UMC. While the SX-series devices ran with a core voltage of 3.3 VDC, the SX-A-series devices run with a core voltage of 2.5 VDC. There are other electrical differences, such as in the I/O stage.

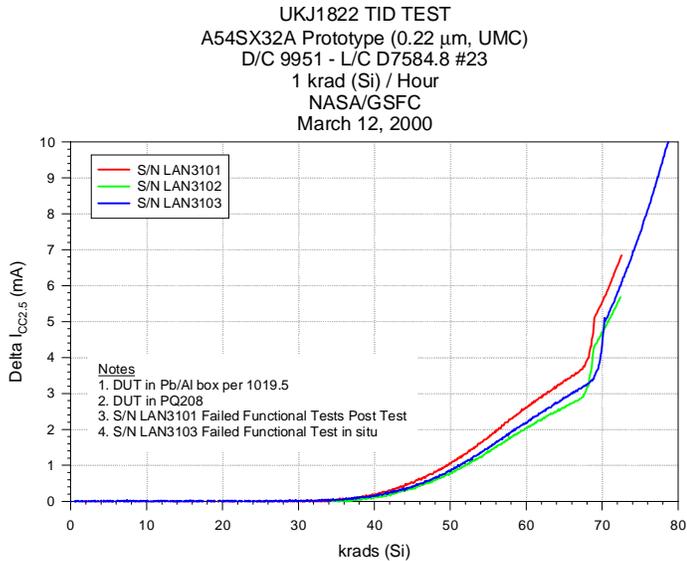
This note will review some of the total dose data from prototype MEC devices. An experiment was run on two wafers of A54SX32A (prototype) devices, produced at the MEC foundry. The two wafers were processed to see the effects on total dose performance. The bias voltages for this test consisted of 2.5 VDC for the array and 5.0 VDC for the I/O ring. Three parts from each of the two wafers were tested. Clearly, either of the two wafers would be considered

radiation-tolerant. Wafer 20 demonstrated performance levels greater than 200 krad(Si). The results are summarized in the chart below.



The next two charts summarize performance of 0.22 μm SX-A technology from the UMC fab. Again, with the use of *in situ* testing, it was shown that functional failure occurred with the small current jump seen in the strip chart. Note the low absolute level of the current when this failure was detected.





A42MX36 Heavy Ion Test

Previous heavy ion tests have shown that the A32200DX, with dual-port RAM, was highly susceptible to single event latchup (SEL). No SEL was detected in the A32140DX, which did not include the SRAM. The A42MX36 is the direct descendant of the A32200DX. These devices were tested at Brookhaven National Lab in September 1999. Bromine was used at normal incidence, for a LET = 38.1 MeV-cm²/mg. V_{CC} was set to a nominal 5.0 VDC. All runs resulted in the device latching, almost instantly. An attempt was made to find the latchup sensitive region by masking the part; this effort failed. Because of the low LET latchup, cross-section information and latchup threshold was not measured. A flux of approximately 1.2 x 10⁵ p/cm²/sec was used for all runs. Latchup currents, for some runs, exceeded two amps.

The devices were packaged in a PQFP208. The D/C was 9826 and the lot code was 2ACT14014.1.

More detailed information on this test is available at: http://rk.gsfc.nasa.gov/richcontent/fpga_content/MX_Series/42MX36_BNL0999/42MX36_BNL0999.htm.



National LVDS

LVDS DS90C031 Heavy Ion SEL Test
Brookhaven National Labs
September, 1999

Test Results Summary

Heavy ion tests were run on the National Semiconductor DS90C031 LVDS driver. These devices were modified to eliminate the latchup sensitivity they have shown in previous versions and heavy ion tests. The DUTs for this test were in flat packs and mounted on a controlled impedance (100 Ω) printed circuit board. Previous tests used SOIC and LCC packages. The dies are identified as DS90C031D by optical examination using a microscope.

No latchups were observed during these test runs. Three units were tested and all runs were at maximum voltage (5.5 VDC), worst-case for the single event latchup (SEL) test. Both data patterns (zeros and ones) were used. High fluences were used, typically 4 x 10⁷ ions/cm² per run, to ensure a thorough test of this modified device. No functional failures or damage was detected.

Some Single Event Transient (SET) data was obtained. A graph of SET Cross-section vs. LET was not made since the parts were not tested at either nominal or low voltage. Hence, the data is supplied only for reference. The circuit configuration may also underestimate the SET rate; the four driver receiver pairs per device are wired in series. The output of the last receiver (DS90C032) is monitored in two ways. The first simply goes to a relatively slow RS-422 driver, a DS26C31, which sends the signal down a long cable (50 to 100 feet twisted pair), into a DS26C32 RS-422 receiver, then into a counter implemented in

an Altera 5192. The final contents of this counter are listed in "Upsets Slow." We expected, and observed, that the slow interface would act as a filter. The clock input of a 74AC109 was used as a fast transient pulse detector. This data is shown in the column labeled "Upsets All" and is a better indicator of the SET rate. It will underestimate a bit as the 4 series connected driver-receiver pairs may act as a filter.

Beam time limitations during this trip prevented a full SET characterization as well as testing at lower LETs to find the SET threshold - the primary objective of this test was to verify the SEL design fix. Our next test will be to perform an SET characterization. Additionally, transient waveforms will be captured to determine pulse amplitudes and widths.

For additional information, tables, and plots, please see: http://rk.gsfc.nasa.gov/richcontent/Misc_Content/LVDS/LVDS_September_1999.htm

Long Term Anneal

To investigate the effects of processing on total dose performance, the UCL064 lot of A14100A (0.8 μm, MEC) was split several ways. Parts were selected from different wafers and exposed to 20 krad(Si) for this part of the test. The parts were then put on a long-term anneal; at the time of this writing, this has been 300 days. The two charts below summarize this information.

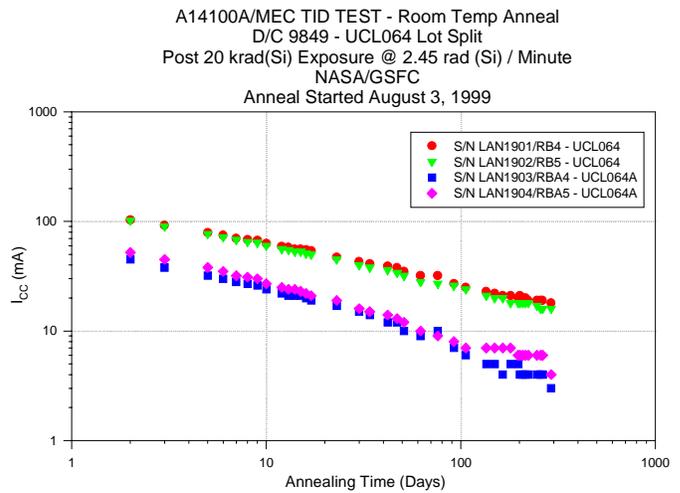
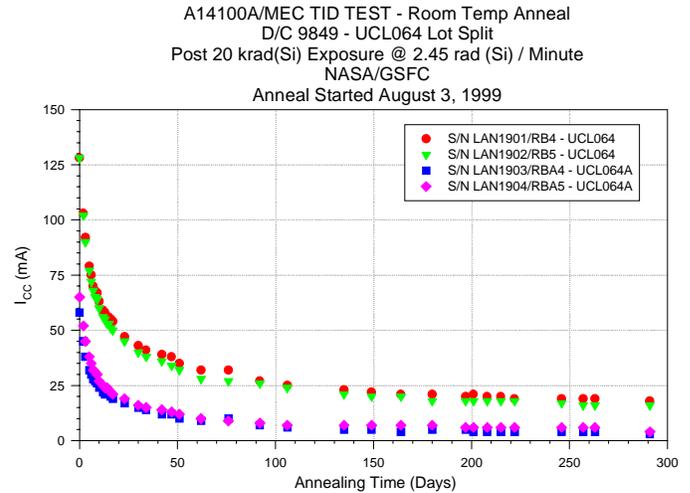
As can be seen, even at the modest level of 20 krad(Si), both sets of parts consumed relatively high levels of ICC, with significant differences between the lot splits. With regular processing, over 125 mA was consumed while that figure dropped to about 20 mA for the modified process.

For the anneal, we see the drop in ICC quickly tapering off, with the standard parts still consuming close to 20 mA and the modified parts consuming just a few mA.

The two charts are generated from the same data set. The top chart presents the information in the usual linear-linear graph. The bottom chart presents the data in a log-log format where there appears to be a linear relationship between log₁₀(ICC) and log₁₀(Time). It is tempting to be able to extrapolate results from future tests, as these long term tests are

time consuming, monopolize equipment, and are expensive. More data and analysis would be needed before extrapolation is possible.

Another set of long term annealing data is being taken on parts from the RT54SX series of devices.



KPP - A VHDL Pre-Processor

KPP is a pre-processor, similar to CPP, written for VHDL applications. It provides many standard functions such as #def, #undef, #ifdef, and #include that are often useful, but not supported by VHDL. Other features are also provided such as "for" loops. This software will run on Win '95, Win '98, and Win NT and was written by Ingrid Brill.

For more information and the software, please see: http://rk.gsfc.nasa.gov/richcontent/Software_Content/KPP.htm

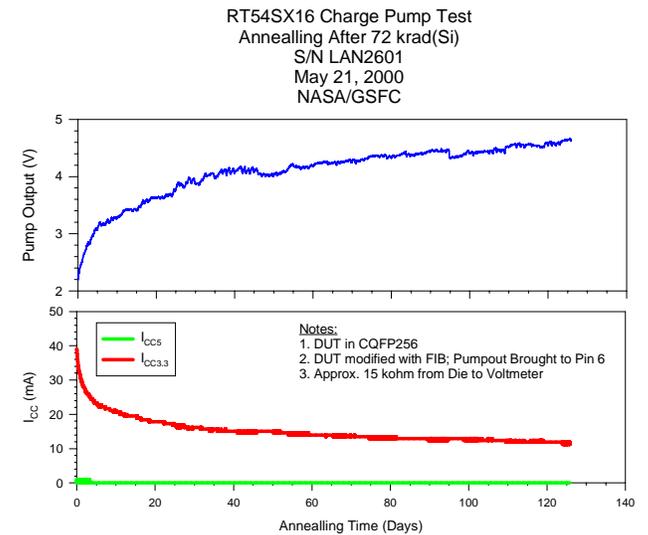
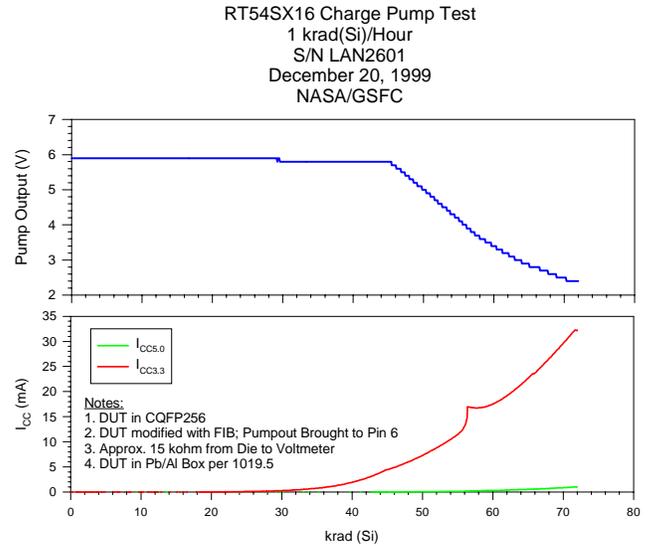
Some information from the included help file shows some of the features of KPP.

- **define <variable> {number}:** Causes the variable to be defined, or exist, in the program.
If number is included, the variable is defined as that number throughout the rest of the program.
- **#undef <variable>:** Causes the variable to be undefined, or not exist, in the program.
- **#include <filename>:** Replaces itself with the contents of the file filename (which are then also processed in the same fashion as the original code).
Nested #includes are allowed.
- **#ifdef <variable>:** Performs the code below if the variable is defined.
- **#ifndef <variable>:** Performs the code below if the variable is not defined.
- **#else:** Must always have either an #ifdef or #ifndef preceding it. Performs the code below if the preceding #ifdef or #ifndef statement was false.
- **#endif:** Needs to follow either an #ifdef, #ifndef, or an #else.
- **#for <variable> = x to y:** Loops through the code below, letting variable equal all the numbers between x and y, with an increment of 1.
- **#endfor:** Needs to follow a #for.

Charge Pump Measurements

It has been known for a considerable period of time that radiation effects on the charge pump circuitry have major effects on certain classes of programmable devices. Largely, this was inferred. Using RT54SX technology, direct measurements are now available.

The RT54SX16 (0.6 μm ., MEC) device was used for this test. Using a focused ion beam (FIB) the microcircuit was modified, bringing the charge pump's output to an unused I/O pin, where it was routed to our measurement system. In situ measurements were performed and the results are shown in the two charts below. Experience has shown that the small increase of ICC is associated with functional failure in this technology.

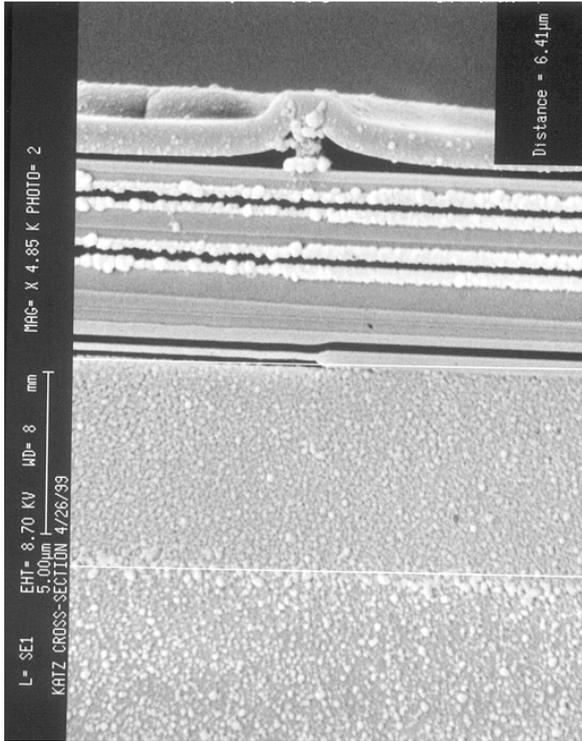


QL3025/EPI Experimental Devices

Heavy Ion Test

An experimental lot of QL3025's were fabricated, using an epitaxial layer of approximately 6.4 microns. Latchup tests were conducted at Brookhaven National Lab, using titanium at normal incidence, for an LET = 18.7 MeV-cm²/mg. Six devices were tested in total; three from each of two wafers. Nominal voltages for this part are VCCIO = 5.0 VDC (input bias) and VCC = 3.3VDC (majority of the part). Low voltage operation was also tested, attempting to find a latchup-free operating area. The results and current strip charts are shown on the www page referenced below. Because of the low LET latchup, cross-section information and latchup threshold was not measured http://rk.gsfc.nasa.gov/richcontent/fpga_content/

Quicklogic/QL3025EPI_BNL0499/QL3025EPI_BNL0499.htm.

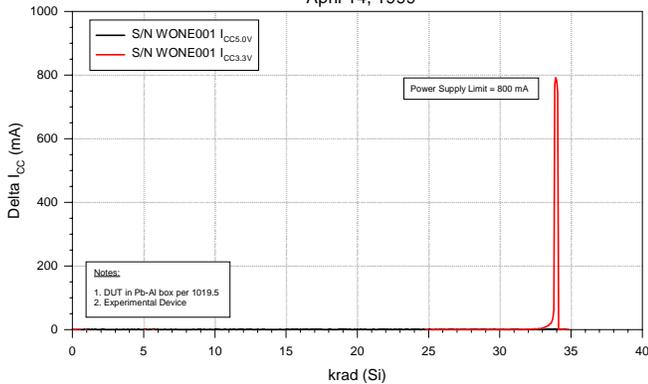


Total Dose Evaluation

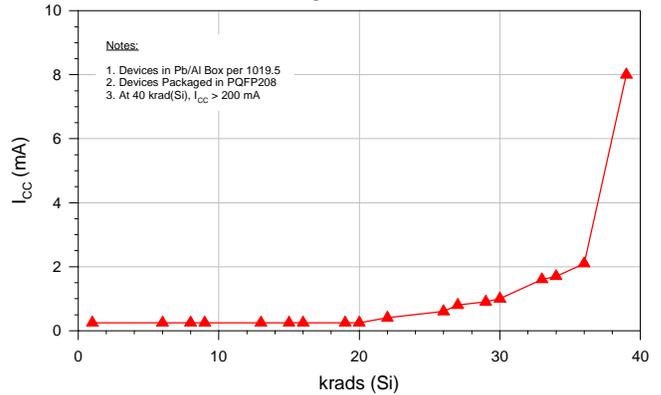
Two of the experimental QL3025/epi devices were evaluated in the NASA/GSFC total dose test facility. Dose rates of 18.6 krad(Si)/Day and 1 krad(Si)/Day were used. The results are summarized in the two charts below.

If we use the loss of control of the part as an estimate of the point of failure, we see a difference between the two dose rates of about 17%.

QL3025-2 ESPQ208R TID TEST
D/C 9913CA
18.6 krad (Si) / Day
NASA/GSFC
April 14, 1999



QL3025/Epi Low Dose Rate Test
1 krad(Si) / day
NASA/GSFC
August 5, 1999



Availability of Radiation Hard Space Quality Microcircuits

David M. Peters
Jet Propulsion Laboratory
818-354-7744
david.m.peters@jpl.nasa.gov

Radiation Hard Space Quality microcircuits, transistors, MOSFETs, diodes, & hybrids are available ~one week ARO. Contact Steve James (818) 354-0570, or visit <http://nppp.jpl.nasa.gov/data/sources.htm> for more information. Check the JPL "inventory page" which contains the current updated inventory of:

- Actel
- Data Devices Corporation Products
- Honeywell Solid State Electronics Center
- International Rectifier Corporation, Government and Space Products Group
- Intersil Corporation, Space and Defense
- Linear Technology Corporation
- Lockheed Martin, Space Electronics & Communications
- MicroSemi Corporation
- Micropac Industries, Inc.
- National Semiconductor Corporation Products
- TEMIC Semiconductors
- UTMC Microelectronic Systems, Inc.
- Xilinx, Inc.

ELECTRONIC PARTS STOCK AT DISTRIBUTORS

- Arrow/Zeus Electronics
- AVNET Electronics Marketing, Defense and Aerospace Product Business Unit
- Tecnologica

ELECTRONIC PARTS STOCK HELD BY THE USERS

The EPIMS-Web (<http://epims.gsfc.nasa.gov>) provides a link to "Parts Stock/Inventory" being held at NASA Goddard.

Contact Steve Waterbury (301) 286-7557 for more information and passwords.

The US Air Force maintains a www site for JAN S semiconductor and microcircuit stock held by DoD. Visit <http://ax.laafb.af.mil/cgi-bin/jansearch>.

Reliability Modeling of Micro-Electromechanical Systems Using Neural Networks

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281-483-5814

The following article summarizes ongoing research into the development of reliability models for Micro-Electromechanical Systems (MEMS) using neural networks. A detailed report describing the results will be available from the author in the next fiscal year.

Background

Revolutionary new devices are being fabricated at research institutions and commercial laboratories that may become one of the key defining technologies of the upcoming decade. These devices are known as Micro-Electromechanical Systems (MEMS) and are a class of semiconductor devices that utilize both mechanical and electrical systems at a microscopic scale. MEMS are essentially a hybrid of electrical and mechanical systems only visible using a microscope. In the MEMS environment, gravity and inertia are no longer controlling, but rather the effects of atomic forces and surface science dominate. MEMS devices are generally batch-fabricated, tens of thousands at a time, with economies of scale significantly reducing unit cost. In addition, the low/no touch fabrication

process of MEMS can create reliable systems with precision.

In the coming decade of this new millennium, the next step in the silicon revolution could be the widespread use of MEMS devices in many commercial and government applications. MEMS have become one of the most promising emerging technologies because of its potential to significantly alter many applications. MEMS are receiving substantial support for research and development throughout the world. MEMS will likely enable vast improvements in sensing and control in automotive, medical, space, military, telecommunication, computing, environmental, industrial, and recreational applications.

MEMS research and development is rapidly progressing in space applications -- where low-cost, high-reliability, small-size, low-power MEMS can have dramatic benefits. In addition by using MEMS technology, NASA will be able to embed many varying systems into one mission, thereby, gaining more science with the same investment.

Problem Description

An important part of any development process is being able to quantify the reliability of the device during conceptual design. At the conceptual design phase of a project, before the MEMS devices are actually built and tested, traditional methods of quantifying reliability are inadequate because the device is not in existence and cannot be tested to establish reliability distributions. A methodology for estimating MEMS reliability is required by design engineers.

In order to guide MEMS process development through reliability evaluations, quantification of MEMS reliability by evaluation and analysis of devices, test structures and materials must be made. Such a reliability estimate must be based on data available at the conceptual design phase of a project -- data about the fabrication process, design characteristics and physical attributes and performance expectations from the device including parameters related to the operating environment, and also packaging. The *reliability modeling techniques using neural networks* developed during this research may provide an ideal mechanism to translate these attributes into a predictive reliability tool.

In confronting the issues of MEMS reliability assurance, developers will certainly have different requirements. For example, a manned Mars mission will have a different set of requirements and specifications than an electronics device designed for home use, but there will be similar methodologies for assessing and quantifying the reliability of both. The neural network modeling techniques developed in this research are designed to utilize basic similarities in design requirements to provide a means of predicting MEMS reliability.

To quantify the reliability of a MEMS component, consideration must be given not only to the device itself, but also to the entire process surrounding the part, from conception, design, fabrication, testing, and packaging schemes, and ultimately to the environment in which the device will operate. This means that the development process must be qualified and effectively modeled including, the fabrication process, quality standards, and fabricator's experience. In addition, the design must be verified, and the packaging certified.

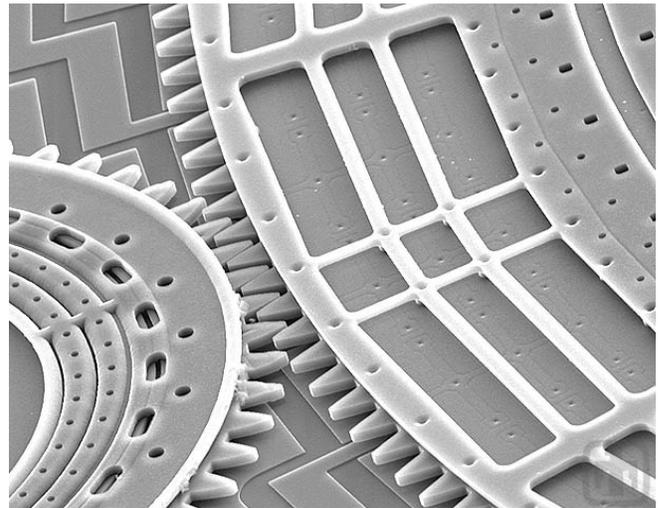
A Proposed Solution

The research performed by this author consists of developing reliability modeling techniques for MEMS devices at the conceptual design phase using *neural networks*. In addition, these neural networks can be used in the design process to optimize the overall reliability, since the networks can provide insight on what design, fabrication, operating and packaging attributes are significant determinants of overall reliability (can easily perform sensitivity analysis with the results of the modeling).

General Modeling Approach

A common obstacle to research of this type is the lack of readily available data, both quantity and quality, that are needed for adequate training of the neural networks. There is very little available data on MEMS reliability since most commercial manufacturers consider their reliability data proprietary. Most universities and research institutions do not have the quantity of similar data required to adequately produce models. However, Sandia National Laboratories in Albuquerque, New Mexico has been designing and manufacturing MEMS components for several years. Sandia is also emphasizing MEMS research because of

their characteristics: high reliability, low power consumption, small size and weight.



Precision MEMS Gears/ Courtesy of Sandia National Labs

Sandia has shown a lot of interest in the novel reliability modeling approach being developed in this effort. Sandia has graciously made all their reliability data for their MEMS microengine device available for this research (see photo example of MEMS gears). For more information on Sandia's microengine, contact Danelle Tanner at tannerdm@sandia.gov. Most of the reliability data are from the same basic MEMS design, with only minor design and operating environment parameters varied. Even though this is a limited test sample, it has provided an excellent basis to determine the feasibility of this modeling approach.

The general approach to developing neural networks to predict MEMS reliability consists of decomposing the system to its component level (gears, gyros, springs, etc...), then selecting which MEMS component attributes have a correlation to its component reliability. Next, data on the selected attributes and the overall component reliability are collected. The reliability data should be fit to a flexible distribution (e.g. Weibull). Whichever distribution is selected to fit the reliability data to, that distribution's parameters will become the output parameter of the model.

After all the input and output data is collected, the neural networks are trained with the inputs (attributes) and the outputs (shape parameters of the selected distribution, e.g. α , β for Weibull) from all the MEMS devices available. For this research, as men-

tioned earlier, the Sandia microengine was used because it was the only one available with sufficient data. However, before training, the attribute and reliability data is randomly partitioned into training data (the majority) and validation data (the remainder). A neural network is then applied to the training data (both attribute and reliability data is used to train the networks) -- the attributes eventually become the system inputs and reliability, the system output. As previously discussed, attribute data consist of any parameter that might have a correlation to overall reliability, i.e., fabrication process details, physical specifications, operating environment, property characteristics, packaging, etc. During the training process, the neural networks will find the actual correlation between the attributes and the reliability estimate. After the networks are trained, the validation data is used to verify that the neural networks provided accurate reliability estimates – independently validating that the neural network is accurately predicting reliability. Note that during testing with the validation data, only the input data is provided to the model. Then the output from the model (the reliability estimate) is compared to the real reliability value known from testing. If there is consistently good correlation between the estimates and the known values, the model can be used as a predictive tool for MEMS reliability. Now, reliability of a newly proposed MEMS device can be estimated by decomposition and utilization of the appropriate trained neural networks.

In contrast, insufficient correlation could be because the networks were not trained with enough data, or because not enough of the correct inputs were specified. Also possible, is that the data transformations or segmentation was inadequate.

Conclusion

To date extensive research into the development of reliability modeling techniques using neural networks has been performed. Use of true reliability data from Sandia National Laboratories has enabled this researcher to develop, test and quantifiably validate this reliability prediction methodology. The preliminary results of this research suggest that use of the techniques described herein may be used to accurately estimate the reliability of proposed MEMS devices during the concept phase before they even exist. Such tools may therefore be used to provide feedback into

the design and development of new MEMS devices to ensure that the ultimate end product has a higher likelihood of being robust and reliable. A final report on this exciting research will be produced during the next fiscal year.

Electronic Nose Technologies Advances in Engineering, Integrating and Commercializing Novel Sensor Technologies

October 26-27, 2000 • San Diego Hilton Resort
• San Diego, CA USA

(Knowledge Foundation)

Conference Chair:

Rajeshuni Ramesham, Ph.D., Applications Engineering Group, Quality Assurance (QA), Safety and Mission Assurance Directorate (SMAD), Jet Propulsion Laboratory; Tel:818 354 7190, Rajeshuni.Ramesham@jpl.nasa.gov

Significant advances are being made in the development of microfabricated microsensors and microsensor arrays for detecting gases and vapors. Producing practical and versatile instrumentation based on MEMS and monolithic IC sensor technologies will depend on ancillary components for sample collection, transfer, preconcentration and separation. The technical challenges are innumerable in designing, fabricating and interfacing with such components and optimizing their functional integration are topics of increasing importance. Also of critical interest are more efficient methods of data acquisition/management and analysis to coordinate system functions and interpret sensor responses for long-term reliability in terms of quality assurance and stability.

Major topics to be covered in-depth include:

- Science, Technology and Engineering Development of the Electronic Nose
- Electronics Packaging, Reliability, and Quality Assurance of E-Nose and Commercial Off-The-Shelf (COTS) Electronic Noses
- Current and New Applications for Existing E-Nose Technology

- Data Measurement and Management, Pattern Recognition and Electronic Neural Networks for E-Noses
- Market Opportunities for Electronic Noses

With a focus on exploring basic science, technology, engineering, and the integration and implementation of micro and macro analytical set-ups to identify gas species, this exciting new conference provides industry, government and academic investigators a unique opportunity to come up to speed and capitalize on electronic nose technologies.

Presentations have been arranged from the leading professionals from

National Science Foundation, Alpha-M.O.S, University of Wollongong (Australia), JPL/Caltech, Georgia Institute of Technology, MOTech (Germany), University of Brescia (Italy), Electronic Sensor Technology, Karlsruhe Research Center (Germany), NC State University, NIST, St. Croix Sensory, Inc., NRL, Agilent Technologies, MSU, Duke University Medical School, Cyrano Sciences, Illumina Inc.

One of the sessions will be chaired by Dr. Margaret Amy Ryan of JPL/Caltech (Section 346). The E-Nose task is funded for FY'01 by the NASA Electronic Parts and Packaging (NEPP) Program.

More details for this conference are provided at the following website:
<http://www.knowledgefoundation.com/enose2000.html>

The Aerospace Corporation's Manufacturing Problem Prevention Program (MP³) June 27-28, 2000

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From June 27-28, 2000 the Aerospace Corporation (support organization to the US Air Force Space and Missile Systems Center [USAF SMC]) hosted a conference entitled the Manufacturing Problem Prevention

Program (MP³). The MP³ provides a forum for spacecraft system manufacturers, hardware suppliers, and government agencies to share their lessons learned and experiences in building government contracted systems. The Program has focused on generating and distributing information that is intended to prevent problems, and minimize schedule and cost impacts due to unpredicted problems or anomalies. The MP³ has proven to be a valuable resource for both the Air Force and its contractors.

This MP³ meeting highlighted best commercial practice related issues and lessons learned in printed wiring board (PWB) procurement: an area of interest for cost reduction for many government contracted space systems. Topics included PWB fabrication, sub-contracted manufacturing, population & integration, Ball Grid Arrays (BGA) and Plastic Encapsulated Microcircuits (PEMs). Presentations were given by several major space contractors including TRW, Lockheed Martin, Boeing, Raytheon and Hughes as well as by the Aerospace Corporation and JPL.

Attendance to the MP³ conference is free and open to all U.S. Citizens. Visit the MP³ Homepage for future conference announcements. Copies of the proceedings may be obtained by contacting the conference sponsors at: mp3@aero.org

<http://www.aero.org/conferences/mp3/>

The following provides some highlights from the conference:

Manufacturing Problem Prevention Program Highlights

June 27-28, 2000

As a result of previous MP³ meetings the Aerospace Corporation has published eight "Strategies" over the years that address commonly occurring problems in spaceflight hardware/electronics assembly. The topics of these strategies are:

1. Honeycomb Sandwich Structures
2. Methyl ethyl Ketone
3. Tin Whiskers
4. Gold Embrittlement of Solder
5. Conformal Coating

6. Corrosion of Silver Plated Copper Wire: Red Plague
7. Conductive Epoxy Adhesives
8. High Strength Aluminum Alloys

Copies of these Strategies are available directly from the US Air Force SMC homepage:

<http://ax.laafb.af.mil/~gowerj/MP3strategies.doc>

This particular meeting of the MP³ focused on Lessons Learned in PWB procurement with some topics directly related to EEE parts issues. Some highlights from the conference included:

- Problem: Some "certified" labs improperly prepare PWB coupons for analysis. Improper preparation has led to falsely passing substandard flight boards. Problems were not uncovered until deep into integration and test resulting in major cost and schedule impacts.
Lesson: Know your coupon lab well. Oversight/direct involvement with the processing of coupons may be necessary. Some OEMs now closely monitor/coach their outside labs to ensure proper sample preparation. Subsequently, I have talked to GSFC experts in coupon analysis and found that they strongly agree that good coupon analysis is hard to come by.
- Problem: Improper design of PWB coupons. Some major contractors expressed concerns that the coupons for their flight boards did not adequately represent the flight board (i.e., not statistically significant # of samples of each hole size, coupons not selected from representative areas of the panel from which the flight boards were made).
Lesson: Some contractors design the coupons themselves rather than allow the PWB house to do it. In other cases OEMs are having one sacrificial flight board produced for each panel processed rather than having coupons built on the panels.
- Problem: Very few (if any) PWB suppliers make ALL types of PWBs well. Most presenters expressed that the majority of PWB manufacturers have some specific products they are experts in manufacturing, but may not be equipped to produce other types of PWBs. In addition, many

excellent PWB suppliers may not be responsive to low volume/high reliability customers for the simple reason of economics (i.e., getting a quality PWB does you no good if it does not meet your schedule).

Lesson: Know your PWB supplier, their capabilities and their primary customer base. Just because one PWB supplier can produce outstanding flex circuits does not mean they can make good rigid boards. In addition to obtaining quality PWBs, users must be concerned with the supplier's attentiveness to schedule. For low volume space procurements, it's important that you know your PWB supplier very well. Some houses will not give you proper support because of the low volume.

- Problem: Simple reliance on industry standards for space grade PWBs may not be wise. Some OEMs indicated that the IPC standards organization that maintains the PWB specs for industry may not have adequate representation from the space community to define proper requirements for hi rel/space needs.
Lesson: Some OEMs have tailored their own addendum/exceptions documents to go along with the IPC standards to address their high rel needs. GSFC has one (S312-P-003). PWB suppliers counter that there is a trade off in this approach because suppliers do standard practices best and may have difficulty when asked to do something special. Use industry standards when appropriate. Tailor only when really necessary.
- The Aerospace Corp. gave a presentation on the Status of COTS Insertion in Space. Issues such as PEMs, volatility of the manufacturer's design's/materials (change control), applicability of COTS to severe environments and obsolescence were addressed.
- One contractor shared their problem experiences regarding Stacked Ceramic Caps. They noted cracks in "as-received" parts due to designs that use a "tab" in the lead frame. Thermal stresses during the manufacturer's attachment of the lead frame to the stack of ceramic chip caps caused stress fractures in the ceramic chip originating at the lead frame tab to chip cap interface.

Information on Non-operating Reliability of Electronic Parts

Review Performed by Charles L. Gamble, Jr.

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The following information was obtained from reports on the Sense and Destroy Armor (SADARM) munition project for the U.S. Army. Most of the information below was obtained from reports published in 1985 and 1989.

There exist no accurate methods for determining a non-operating failure rate without observed failures.

Analysis of the collected data showed that the effect of long-term storage on the SADRAM electronic devices is a result of two major factors: parts design and environment.

Studies conducted for the Department of Defense (DoD) agencies have demonstrated that the ability of a system to withstand long-term storage conditions can be designed into the system. In general, design guidelines for the total life cycle for any system may be grounded into the following categories:

- Part Selection and Control
- Derating Practices
- Equipment/System Packaging
- Transportation and Handling
- Design Maintainability
- Design Testability
- Evaluation Methods for In-Plant and Field Evaluation
- Product Performance Agreements

Information collected during this study indicates that SADRAM electronic devices can be produced that will meet functional requirements after 10 years of dormant storage if the factors causing deterioration are known and eliminated or controlled. These factors include:

- Latent Manufacturing Defects
- Design Deficiencies
- Material Incompatibilities
- Residual Contaminants
- Environmental Contaminants
- Mechanical Stresses

Designing non-operating reliability into electronic devices requires the careful selection of discrete parts that comprise the devices. The objective of this part selection and control program is to obtain parts that will perform adequately and reliably after a minimum of ten years of dormant storage; a twenty-year dormant storage capability is desirable.

Summary of Review

The review of these reports revealed that the following types of electronic parts exhibited good reliability characteristics after long-term non-operating storage (10 years or more).

- Military grade fixed capacitors, except for electrolytic types
- Military grade integrated circuits (i.e., MIL-C-38510, Class S and Class B, or equivalents)
- Military grade DC/DC converters/Regulator electronics, if the same selection & application criteria used for integrated circuits is applied.
- Military grade film resistors and resistor networks.
- Military grade cables and connectors

The reports stated that the following electronic products were not recommended for long-term dormancy periods.

- Electrolytic Capacitors
- Variable Capacitors
- Inductive Devices (i.e., transformers, coils, etc.)
- Composition Resistors
- Wire-Wound Resistors
- Variable Resistors
- Plastic encapsulated devices

The reports also stated that environmental conditions must still be considered during long-term dormancy periods.

- Humidity/Moisture
- Ionic Contaminants
- Temperature
- Radiation
- Shock
- Vibration
- Other environmental conditions

There was no information in the reports on discrete semiconductor devices (i.e., diodes, transistors, and optocouplers).

The following are the details of the review:

DC to DC Converters/Regulator Electronics

Failure mechanisms for discrete semiconductors non-operating failure mechanisms are generally the direct result of deficiencies in materials and fabrication processes.

Bulk defects in silicon collect contaminants. These contaminants can cause thermal problems, gain failures, and leakage defects. Die and wire bonding failures are also very common.

Applying the same selection and application criteria used for microelectronic integrated circuits will assure that these components provide the required dormant storage reliability. Note that the reports indicated the MIL-C-38510, Class S and Class B integrated circuits exhibit good non-operating reliability characteristics.

Capacitors

The capacitors were subdivided by construction type as follows:

Fixed

Paper and/or Plastic
Mica or Glass
Ceramic
Electrolytic

Variable

Ceramic
Air

Generally, capacitors are stable devices in dormant applications, with the exception of variable and electrolytic types.

Variable capacitors are highly susceptible to environmental induced degradation; therefore, they are not recommended for dormant applications.

Electrolytic capacitors, both liquid and solid types experience definite dormancy induced degradation, and use of these devices in dormant applications should be controlled.

Electrolytic capacitors have experienced problems is storage.

- Electrolyte leakage in wet tantalum capacitors has been a major factor in long-term storage reliability.
- Impurities in the solid type electrolytic components have been the major cause of problems. A temperature cycling environment accelerates most of the failure mechanisms associated with these components.
- The self-healing properties of electrolytic devices will compensate for short dormancy periods (< 4 years). However, even during short non-operational periods, these devices require periodic monitoring to ensure reliable operation.

Fixed capacitors are generally very stable components in either dormant or operational environments. The only exceptions are the electrolytic types.

- Fixed capacitors with paper, paper/plastic, or plastic dielectric, as a group, have high insulation resistance, good stability, low dielectric absorption and low loss factor over a wide temperature ranges.
- Metallized paper capacitors have low insulation resistance and are prone to dielectric breakdown.
- Capacitors with plastic dielectric, which is nonabsorbent, have superior moisture characteristics, but should be hermetically sealed since small amounts of moisture increase the rate of chemical reactions with the capacitor materials.
- Fixed glass and mica dielectric capacitors have non-flexible dielectric materials. These components have excellent long-term stability, a low

temperature coefficient and a history of good reliability.

- Fixed ceramic capacitors are available in tubular, flat disc, or flat plate design configurations. In dormant applications, wax impregnated conformal coatings will collect dust and other contaminants and the insulation resistance will decrease under prolonged high humidity conditions. These components also have a good history of reliability in both operational and dormant modes.

For most fixed capacitor types, dormancy is not a significant degradation factor; however, dormant capacitors may degrade due to environmental factors experienced during the dormant period.

- Temperature and moisture are the primary degrading environments for capacitors.
- Low temperature can result in significant capacitance changes for capacitors, whether they are operating or dormant.
- Capacitors are susceptible to moisture induced degradation. Even in hermetically sealed units, moisture present during manufacture can lead to deterioration of insulation or dielectric materials. This can be a more serious consideration in certain lower grade devices.
- Moisture in the capacitor dielectric will decrease the dielectric strength, life, and insulation resistance, and increase the power factor of the capacitor. In general, capacitors that operate in high humidity environments should be hermetically sealed. The effect of moisture on pressure contacts, which are not gas tight, may result in a high resistance or open contact.

Inductive Devices

Inductive devices are susceptible to environmental conditions that accelerate dormant failure rates. Temperature, humidity, and mechanical stresses are the primary contributors to dormant failures. Also, inadequate manufacturing processes and improper handling can cause damage contributing to the vulnerability of the components in the storage environment.

For non-operating applications, the selection of standard military inductive devices manufactured with

MIL-SPEC quality components, where possible, is highly recommended.

The primary failure mechanisms in inductive devices in the dormant mode are short and open circuits. They are typically accelerated in storage by moisture and heat, which cause insulation breakdown.

The following is a summation of the effects of dormant storage on transformers:

- Temperature: reduced dielectric; opens; shorts; hot spots (i.e., affects the thermal stability of the magnet wire used); malformation
- Humidity: corrosion; fungus; shorts; opens
- Storage: deterioration of potting and dielectric

The following is a summation of the effects of dormant storage on coils:

- Temperature: warping; melting; instability; change in dielectric properties
- Humidity: electrolysis; corrosion

Resistors

Because of their stability, fixed film type resistors are generally recommended for dormant applications.

However, degradation may occur due to environmental stresses during the non-operating period. The effects of environmental stresses appear to be independent of resistance value, but very dependent upon construction type and quality level.

Humidity is the most significant environmental factor relative to potential degradation of dormant resistors. Long storage periods in a high humidity environment can cause significant changes to resistance values. Open circuits and short circuits are less frequent types of dormancy failures. In operation, resistors tend to minimize the effects of humidity due to heat dissipation; however in storage they tend to absorb moisture. The moisture will not typically cause a failure until after the component is in operation.

The adequacy of the case to preclude the effects of humidity is critical and case failures tend to be the result of processing errors; thus, emphasis is on the selection of higher quality level (i.e., MIL-SPEC, or better) items. Also, circuits should be designed to preclude moisture and dirt traps.

Variable resistors

Variable resistors experience significant environmental degradation in the dormant mode.

Variable resistors are generally considered highly unstable in the dormant mode and are not recommended for dormant applications. In addition to the effects of moisture, shock and vibration are significant environmental factors relative to potential degradation of variable resistors.

Vulnerability to moisture, temperature, shock, vibration, and contamination make variable resistors a poor choice for almost all applications, except where adequate environmental protection is certain.

Fixed resistors are classified by the following construction types: 1) composition, 2) film, and 3) wire-wound. Also, a special type of resistor class gaining wide use is the fixed film network.

Composition Resistors

Composition resistors include those that are formed from a mixture of a resistive material and a binder, and molded into a specific shape and resistance value. Wire leads are imbedded in the resistance element and an insulating case is molded around the resistor, thus forming an enclosure to support the leads and provide a moisture seal.

The case material is normally phenolic and is not completely impervious to moisture. Moisture may cause degradation in the dormant mode by absorption into the element (increased resistance) or the formation of leakage paths (decreased resistance) in surface moisture.

Open and short circuit failure modes seldom occur.

This class of resistor is generally the least stable type in dormant applications, but may be satisfactory if adequate environment protection is expected.

Fixed Film Resistors

Fixed film resistors are formed by depositing resistive material (carbon or metal) on the inside or outside of glass or refractory tubes, and spirally cutting the film to obtain the desired resistance value. Leads and various types of end caps provide electrical connec-

tions and a molded plastic case provides physical strength and moisture protection.

The properties of the materials used to make the resistive film can be selected to provide excellent protection against the effects of temperature cycling and humidity.

Manufacturing defects are credited as being the primary cause of failure in the dormant mode. Tighter screening and process control can be effective in reducing potential dormant failures.

Film resistors are more stable under extreme environmental conditions than composition resistors and approach the characteristics of wire-wound resistors. Because of this stability, film type resistors are generally recommended for dormant applications.

Wire-Wound Resistors

Wire-wound resistors are made by winding appropriately selective resistive wire around a ceramic form. Molded cases provide protection in high humidity environments. Precision resistors of this type provide closer tolerance and stability than the other types.

Failure modes due to humidity include leakage between resistive wiring turns and/or layers and open conditions caused by corrosion and electrolytic action between wire and end cap termination.

Wire-wound resistors are more vulnerable to vibration and shock largely due to type of construction, size and weight. This is the most stable type of fixed resistor under extreme environmental conditions; however, it is not likely to be an acceptable component for dormant applications because of size and weight constraints and vulnerability to shock and vibration.

Fixed Film Network Resistors

Fixed film network resistors consist of multiple deposited resistive film elements packaged in flat pack, single-in-line package (SIP), or dual-in-line package (DIP).

Network resistors offer good stability, long life, and accuracy and are desirable where miniaturization is important and/or where the circuit design calls for multiple resistors of the same value.

Network resistors have essentially the same vulnerability to dormant environment condition as fixed film resistors; however, use of the single package in lieu of separate components reduces potential moisture and contaminant traps.

General Purpose Integrated Circuits (IC's)

Storage failure rates of microcircuits are time-related and environment dependent. For the most part, these failure rates are independent of the device function; however, increased complexity slightly increases expected non-operating failures.

Expected non-operating failures are very dependent on the microcircuit package type. Most package failures are caused by process-related failures. Improper sealing procedures are a major contributor to contamination defects and influence a variety of other non-operating failure mechanisms. Device quality, therefore, is a critical consideration for predicting non-operating failures.

The primary environmental factors that accelerate in storage are temperature, moisture, and mechanical stresses. The most significant failure mechanisms during dormancy are related to manufacturing defects, corrosion processes, and mechanical failures. Although the environments are quite different, most failures that occur during dormancy are the same basic kind as those found in the operating mode, resulting in the further degradation of latent manufacturing defects which were not detected during device screening. The major contributors to non-operating failures are wire bond, oxide, and metallization failures.

The primary concern for long-term dormant reliability for IC devices is the influence of chemical contaminants introduced either from the environment or during fabrication. Moisture, in particular, is very critical because of the corrosion processes it induces directly and because the presence of moisture activates contaminants such as residual chlorine ions. Very minute amounts of water can cause degradation of materials within a device package. All possible steps should be taken to eliminate it within micro-electronic devices. Therefore, the use of hermetically sealed devices is highly recommended. Plastic encap-

sulated devices are non-hermetic and, as a general rule, should not be used for dormant designs.

General-purpose integrated circuits can be expected to have excellent long-term, non-operating storage characteristics if properly fabricated and screened. For long-term non-operating storage applications, it is recommended that the packaging materials of IC's be carefully selected and that the highest quality screening level practical be implemented (e.g., MIL-C-38510, Classes S and B, or equivalents).

Flexible Cables

Cable and wiring configurations include single conductors (shielded and unshielded) wire, twisted single conductor cables (shielded and unshielded), coaxial cables, and multiple-conductor cables (round and flat).

The dominant failure mechanisms for dormant cables are insulation degradation and conductor/connector corrosion and breakage. High moisture and temperature variations are the primary storage environment factors contributing to these failures.

The primary design selection factors for connectors include insert materials, contact current, number of active contacts, mate/unmate cycling (if there is an active maintenance program), and storage environment become critical considerations.

Contact pin corrosion or surface films resulting from adverse environmental conditions are the next major contributors to dormant failure rates. High temperatures can cause insulation breakdown. Low temperatures tend to create fatigue in metallic components due to brittleness and can also cause separation and consequent seal failures between connectors and insulating materials due to shrinkage and different coefficients of expansion between the materials. Moisture and environmental contaminants create connector corrosion.

Insulating materials in cables will fail in the dormant mode generally in the same manner as insulating materials in connectors. The primary contributors to cabling failures are high/low temperatures, moisture and mechanical stresses.

Development of Theoretical Models for Non-operating Failure Rates:

In general, the theoretical model development consisted of evaluation of the hypothetical effect on nonoperating failure rate of the following factors.

- Function
- Technology
 - Fabrication Techniques
 - Fabrication Process Maturity
 - Failure Mode/Mechanism Experience
- Complexity
- Packaging Techniques
- Effectiveness of Process Controls
- Effectiveness of Screening and Test Techniques
- Nonoperating Environment and Temperature
- Frequency of Equipment Power Cycle

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- Effect of Long-Term Storage on Electronic Devices.** This is Contractor Report ARFSD-CR-95008, dated November 1995, from the U.S. Army Armament Research, Development and Engineering Center.
- Long-Term Non-Operating Reliability of Electronic Products.** This is a book written by Judy and Michael Pecht. The book was published in 1995, by CRC Press, Inc. The International Standard Book Number (ISBN) is 0-8493-9621-2.
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