Copyright © 2006 IEEE. Reprinted from Radiation Effects Data Workshop

This material is posted here with permission of the IEEE. Such permission of the IEEE does not in any way imply IEEE endorsement of any of Jet Propulsion Laboratory's products or services. Internal or personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution must be obtained from the IEEE by writing to pubs-permissions@ieee.org.

By choosing to view this document, you agree to all provisions of the copyright laws protecting it.

Radiation Tests on 2Gb NAND Flash Memories

D.N. Nguyen, S. M. Guertin, and J. D. Patterson

Abstract – **We report on SEE and TID tests of highly scaled Samsung 2Gbits flash memories. Both in-situ and biased interval irradiations were used to characterize the response of the total accumulated dose failures. The radiation-induced failures can be categorized as followings: single event upset (SEU) read errors in biased and unbiased modes, write errors, and single-event-functional-interrupt (SEFI) failures.**

Index Terms—**Flash, In-situ, SEE, TID**

I. Introduction

As non-volatile memories have been scaled down to improve its density, NAND flash devices are used widely in commercial as well as space applications. Flash memories are attractive choices for the massive data recorder requirements for space missions. Previous solid-state recorders were designed around reliable, robust and radiation-hardened dynamic random access memories (DRAM) but current and future recorders for space missions are being built with commercial-off-the-shelf flash memory devices.

The NAND structure is more compact since it does not provide contacts to individual source and drain regions. Memory cells in the NAND structure require reading and writing through the other cells in the stack (the current Samsung 9F2G08UOM has 32 cells in the stack plus 2 select cells), an architecture that results in inherently slower cell access as shown in Figure 1. The basic storage element consists of a control gate stacked over an isolated polysilicon gate in the gate oxide known as a floating gate, a source, and a drain. Data can be interpreted as "0" when charges (electrons) are placed in the floating gate. When electrons are removed from the floating gate, data become "1". The configuration is known as single level or one-bit-per-cell storage since the read-out data can be identified either as "1" or "0". In terms of cell threshold voltage, sense-amp circuitry recognizes "1" optimally at the level of 2.7 volts and "0" at 5.7 volts. In order to obtain higher density, flash memory structures have been scaled down in size. But the scaling process reached its limitation at cell size of 55nm [1]. Another limitation is the operating voltage range, the Fowler-Nordheim tunnel devices (NAND structure) need 18 to 20V for program and erase due to the inability of the shorter channel length to withstand the required programming voltage [2]. This paper presents the results of SEE and TID tests and the latent damage on programming capability of NAND flash devices.

D. N. Nguyen is with the Jet Propulsion Lab, Pasadena, CA 91109 USA (phone: 818-354-8554; e-mail: duc.n.nguyen@jpl.nasa.gov)
S. M. Guertin is with the Jet Propulsion Lab, Pasadena, CA 91109 USA (e-mail: steven.m.guertin@jpl.nasa.gov)
J. D. Patterson is with FHCRC in Seattle, WA (e-mail: jpatters@fhcrc.org)

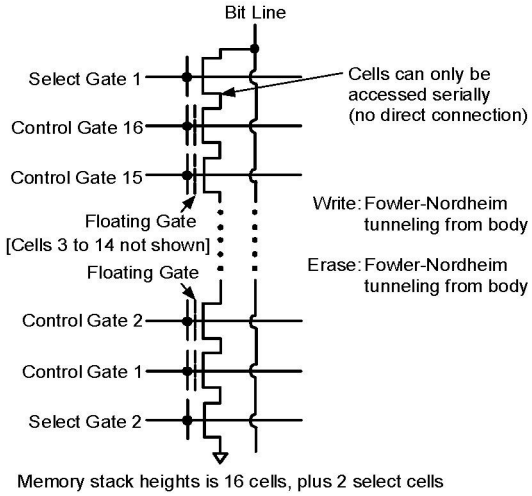

Fig. 1: NAND cell structure, only 16 cells in the memory stack are shown.

II. Device Descriptions

The NAND-based Samsung 2Gigabit flash parts are organized as 2112 bytes x 64 pages by 2048 blocks. Programming and read data are transferred between the 2112-byte static register and the memory cell array in 2112-byte increments. During program and read mode, the page can be separated into three sections by the use of an internal pointer. The erase operation is implemented in block increments. The serial read cycle is 30ns and the access time of cell array to register is 25 microsecond. Samsung devices were built on a 90nm process technology.

The flash memory technology has internal charge pump generators to provide higher voltages than their external operating supplies, for the programming and erase operations. The Samsung flash devices typically require 5 seconds to erase the whole part. The Samsung devices operate with lower currents in all modes, up to 30mA.

Ten de-lidded parts were used for SEE testing and ten other devices were used for TID tests. The date codes are as follows: Samsung K9F2G08UOM with D/C 0240, 0516, and 0616.

1-4244-0638-2/06/$20.00 ©2006 IEEE.

Authorized licensed use limited to: IEEE Xplore. Downloaded on March 17, 2009 at 13:45 from IEEE Xplore. Restrictions apply.

III. Test Set-up

SEE testing was done at the Texas A&M cyclotron and the Brookhaven National Lab Tandem Van de Graaff accelerator. All tests were performed at 25 degree C. The test equipment is comprised of two laptop computers, a power supply, and an FPGA-development system. One laptop controls a HP6629A power supply. This allows precision voltage control and latch-up detection and protection since the computer has millisecond control over the operation of the power supply. A second laptop controls the test circuit board designed specifically to read errors and write commands/test patterns to the (device under test) DUTs. Parts are programmed with all zero. All zero pattern forces all floating gates in the device to be filled with electrons, and consequently creates a worst-case leakage test.

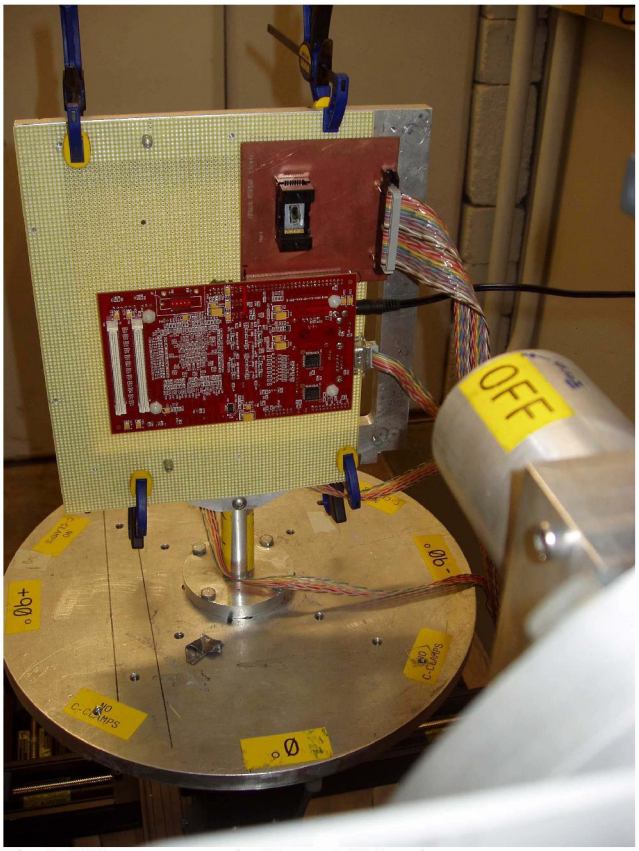

Fig. 2 SEE test setup at the Texas A&M cyclotron

Tests were done with normal incident beam in air at Texas A&M, while at Brookhaven Laboratory they were exposed in the vacuum chamber.

TABLE I
IONS BEAMS USED AT BOTH TEXAS AND BNL FACILITIES

Ion	Energy(MeV)/ LET(MeV-cm^2/mg)	Range(μm)/Facility
Ne	25/2	762/ Texas
Ar	944/6	457/Texas
Kr	1914/20	296/Texas
Cl	212/11	64/ BNL
Ni	270/28	45/BNL
Br	287/41	38/BNL

Total dose tests were done using the JPL cobalt-60 facility at a dose rate of 25 rad(Si) per second with a series of 2 or 4 krad(Si) steps and at 25 degrees C. The devices under test (DUT) were tested with two modes: static-biased read and in-situ mode.

Static biased read-only mode tests consisted of the following sequences:

1. Erase, write, and read to validate checkerboard pattern
2. Irradiate
3. Read pattern to ensure data retention
4. Repeat step 1 with inverse checkerboard data
5. Irradiate
6. Repeat 1 to 5

Fig. 3 TID test setup at the JPL Cobalt-60 facility

IV. Radiation Induced Failures

Flash memories are relatively sensitive to radiation. The overall operation of NAND flash memories requires

Authorized licensed use limited to: IEEE Xplore. Downloaded on March 17, 2009 at 13:45 from IEEE Xplore. Restrictions apply.

many clock cycles and commands just like the operation of most microprocessors because of the complex architectures, such as internal state machine, write buffer, and registers. Single bit upset errors can be caused by a single ion hit on the cell, or in the readout buffer. Soft errors were detected during subsequent reads. Write errors are confirmed when memory cell contents are opposite of expected data during post-irradiation reads. Failure to erase can be defined as an unsuccessful removal of electrons from floating gates after a number of passes, or a failure of device's ready signal to inform the status register after a specified elapsed time. Single event upsets occur in the state machine and registers (address, data, control). They are very difficult to categorize and interpret because of the many interconnected sub-elements inside the functional block. These upsets will mostly interrupt the intended operation and lock it into an undefined function mode. New generations of shrinking cell area in flash memory complicated the distinction between single event upsets and single-event-functional-interrupt (SEFI). [3][4].

V. See Test Results

Six Samsung parts were tested with negligible variation among them. The testing approaches were designed to characterize four single events mechanisms:

1. Upsets occurring during a read
2. Upsets occurring during a write
3. SEFIs occurring during a read or write
4. Loss of charge occurring in an unbiased irradiation. Ionizing particles strike DUTs in a power off configuration. Post read upsets were analyzed to study the future utilization of these devices in a sleep mode during a space flight.

The upset names were defined as follows:

a. Read Upsets (0 to 1): reading a "1" when should have read a "0".
b. Read Upsets (1 to 0): reading a "0" when should have read a "1".
c. Write Upsets (0 to 1): writing a "1" when should have written a "0"
d. Write Upsets (1 to 0): writing a "0" when should have written a "1".

The identification and analysis of SEFI events were more time consuming than for single event bit upsets. SEFIs typically affected large contiguous blocks of compromised data. The definition of what constituted large and contiguous was changed as the architecture of device's control circuitry evolved. When SEFIs were first discovered, their signature usually was a lockup of the device's operation with a high current surge. This is no longer true with today's devices. SEFI events on the Samsung flash devices usually occurred while reading or writing to random addresses in the page, and not at the beginning or the end of the page. Some events would only affect one or a few surrounding pages before returning to normal operation without a power recycle.

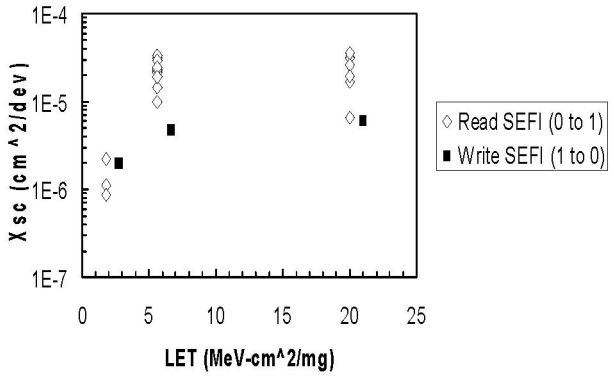

Fig. 4 Cross-section of SEFI upsets of both Read all 0s and Write all 1s.

. Figure 4 shows the SEFI upset cross sections for the devices while reading 0s or writing 1s. Data were sequentially read, one byte at a time. The spread of data was due to the methods used to identify and count the total number of SEFIs. To count all SEFI events, each run must be distinguished from SEU events so that the resulting upsets needed to be subtracted from SEUs. Depending on the beam's LET and flux, it was difficult to separate out a single SEFI event affecting multiple pages or multiple SEFIs creating a smaller number of neighboring pages.

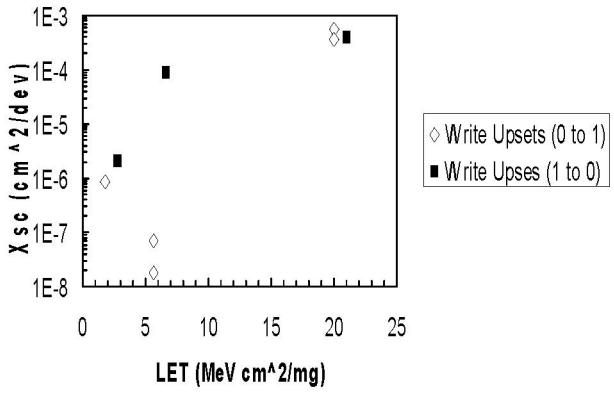

Fig. 5 Cross-section of write operations.

Figure 5 shows the write upset cross sections while the devices were either writing 0s or erasing during beam. Post irradiation verification detected errors during programming and erase operations.

Authorized licensed use limited to: IEEE Xplore. Downloaded on March 17, 2009 at 13:45 from IEEE Xplore. Restrictions apply.

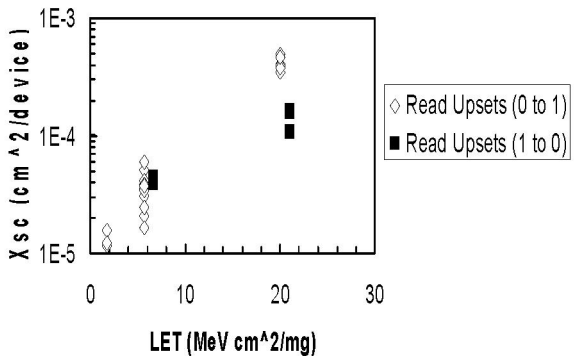

Fig. 6 Cross-section of read-upsets (biased during beam): more upsets of expected zeros than upsets of expected ones.

The devices were read and exposed to beam. More errors were observed with charges being leaked out of the floating gates (read upsets of expected zeros) as seen in Fig. 6.

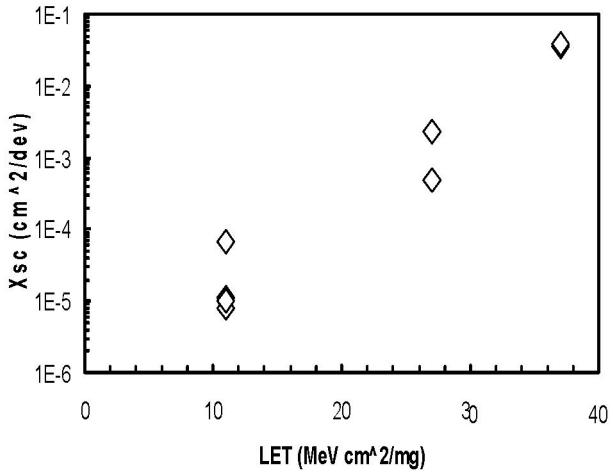

Fig. 7 Cross-section of read upset (unbiased) as indicators of degrading cell retention characteristics.

The parts were tested at BNL with the Tandem Van de Graaff accelerator. DUTs were programmed with all zeros and were unbiased during beam. Due to the sensitivity of charge pump circuitry [5], space applications of flash memories have been advised to power off their devices during flight.

VI. TID TEST RESULTS

In-situ mode tests ran continuously with Erase/Write/Read operation while the parts were exposed to cobalt-60 source. The in-situ setup was used to verify the radiation effects in floating gate memories [6].

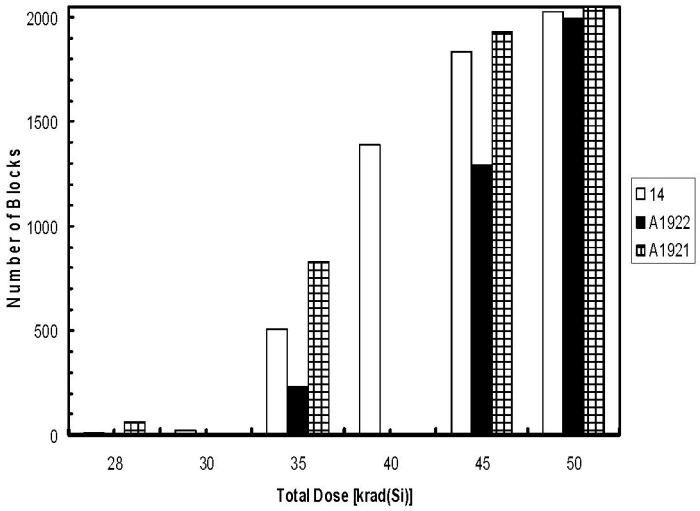

Fig. 8 In-situ irradiation: programming failures with elapsed time of 34 minutes.

Figure 8 shows the gradual increase of bad programmed blocks at 28 krads(Si) and the sudden change starting after 30 krads(Si). The in-situ TID data had shown that the Samsung parts had a small number of bad programmed blocks even at the high accumulated dose at the very start, but after 30 minutes elapsed or at 42 krads(Si), the number of bad programmed blocks increased to almost two thousand. In comparison with the static irradiations as shown in Fig. 9, at 30 krads(Si), the number of bad programmed blocks is already in the thousands.

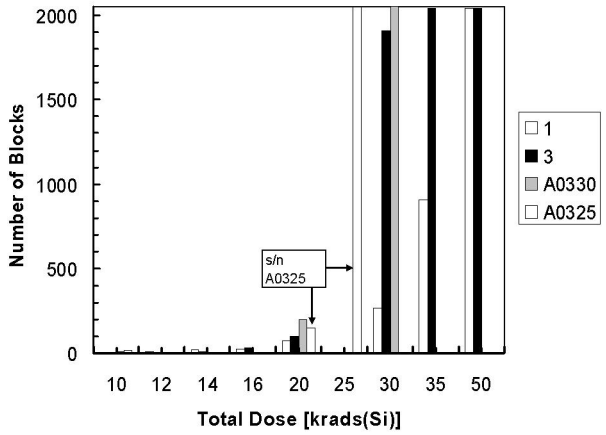

Fig. 9 Programming failures under static biased: except s/n 1, others had a pause of 30-40 minutes between irradiations.

Serial number 1 was electrically tested 30 minutes prior to serial number 3 after each irradiation. Data points

Authorized licensed use limited to: IEEE Xplore. Downloaded on March 17, 2009 at 13:45 from IEEE Xplore. Restrictions apply.

of other two parts s/n A0325 and A0330, were collected 30-40 minutes after the irradiation took place at the following intervals: 10krad(Si), 20krad(Si), 25krad(Si), 30krad(Si), and 35krad(Si). Almost all blocks of devices A0325 were bad after 25krad(Si), A0330 at 30krad(Si), and both sn1, sn3 at 50krad(Si) as shown in Figure 7. Static bias of DUTs and delaying electrical tests between irradiation intervals produce more degradation than the in-situ configuration. After 500 hours unbiased, 120 blocks of serial number A0325 could be programmed again.

VII. CONCLUSIONS

High density flash memory devices are sensitive to SEFI that may add power surge to critical loads due to the power recycling. The devices are improved as far as TID since only few blocks cannot be programmed at 20 krads(Si) compared to earlier flash devices which failed at about 7krad(Si). Worst cases are static biased during irradiation and delay electrical tests between intervals. As the cells are scaled down further, heavy ions reduce the retention capability of the floating gate from keeping charge being drained out. Heavy ions also can damage the charge pump circuitry to stop devices from erase and/or program.

Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not constitute or imply its endorsement by the United States Government or the Jet Propulsion Laboratory, California Institute of Technology

The work described in this paper was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under the contract with the National Aeronautics and Space Administration

REFERENCES

[1] S. Lai, "Tunnel oxide and ETOX flash scaling limitation," *International Non-Volatile Memory Technology Conference,* p6, June 1998

[2] G. Atwood, "Future Directions and Challenges for ETox Flash Memory," *IEEE Transactions on Device and Materials Reliability,* vol. 4, no. 3, pp. 301-305, September 2004.

[3] R. Koga, S.H. Penzin, K.B. Crawford, and W.R. Crain," Single event functional interrupt (SEFI) sensitivity in microcircuits," *Proceedings of RADECS97,* 311-318, 1997.

[4] R. Koga, P. Yu, K.B. Crawford, S.H. Crain, and V.T. Tran," Permanent single event functional interrupt (SEFI) in 128- and 256-megabit synchronous dynamic random access memories (SDRAMs)," *2001 IEEE Radiation Effects Data Workshop Record,* p6.

[5] D.N. Nguyen, S.M. Guertin, G.M. Swift, and A.H. Johnston," Radiation Effects on advanced flash memories," *IEEE Trans. Nucl. Sci.,* vol. 46, no. 6, pp. 1744-1750, Dec 1999.

[6] G.Cellere, A. Paccagnella, A. Visconti, B. Bonanomi, P. Caprara, and S. Lora," A Model for TID Effects on Floating Gate Memory Cells", *IEEE Trans. Nucl. Sci.,* vol.51, no. 6, pp.3753-3758, Dec. 2004

Authorized licensed use limited to: IEEE Xplore. Downloaded on March 17, 2009 at 13:45 from IEEE Xplore. Restrictions apply.