National Aeronautics and Space Administration

BOK– Mechanical Methods for Array Package Assembly

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Objectives and Products

Commercial-off-the-shelf area array package (COTS AAP) technologies in high-reliability versions are now being considered for use in a number of National Aeronautics and Space Administration (NASA) electronic systems. These packages are prone to early failure due to the severe mechanical shock and vibration of launch, as well as other less severe conditions, such as mechanical loading during descent, rough terrain mobility, handling, and ground tests. As the density of these packages increases and the size of ball interconnections decrease, susceptibility to mechanical loading and cycling fatigue grows even more. Information and applicable restrictions on package assembly for NASA's stringent mechanical loading requirements is extremely limited.

This report presents a summary of the body of knowledge (BOK) specifically developed for the evaluation of area array packages and is based on surveys of literature from industry and academia. For high-reliability applications, extremely limited data exists that covers mechanical shock and random vibration; those data will be presented. Most of the data from industry deals with mechanical fatigue caused by four-point bend tests, as well as from drop tests for hand-held electronics; the most recent data will be presented, along with a brief background description of prior literature. Given NASA's severe mechanical loading and fatigue requirements, understanding the key design guidelines and failure mechanisms from past tests is critical to developing an approach that will minimize future failures. Further additional specific tailored testing enable low-risk insertion of these advanced electronic packages.

Key Words: Solder joint reliability, mechanical fatigue, drop, vibration, FCBGA, CGA, CSP, FPGA, flip chip ball grid array, flip-chip column grid array

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1. Executive Summary

Shock and vibration testing at the package, assembly, and system levels has played an integral part in evaluating microelectronics for use in high-reliability applications. Figure 1, which was adapted from a recent presentation by the co-managers of the NASA Electronics Parts and Packaging (NEPP) program, includes mechanical shock and vibration and other key aspects of technology being investigated by the NEPP team.

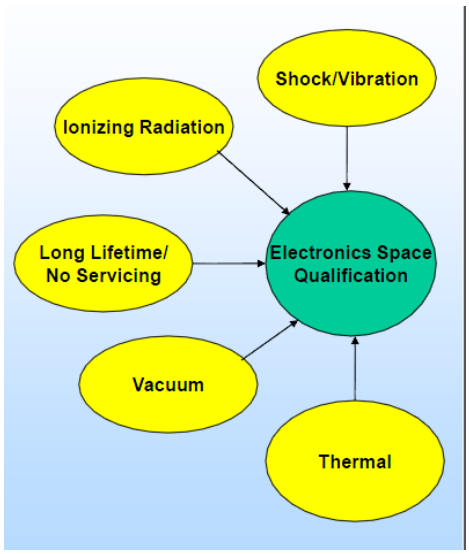

Figure 1. Mechanical shock and vibrations are one of the key concerns for high-reliability applications (courtesy of K, LaBel/Mike Sampson, see reference 1).

NASA has numerous specifications that address evaluating resistance to mechanical loading for conventional packages, such as leaded components. In addition, workmanship requirements to meet harsher mechanical environments are in place. For example, one of the workmanship requirements during inspection is to verify that "adhesive bonding/staking materials has been applied…for parts in excess of 7 grams (0.25 oz.) per lead." Testing applicability or similar workmanship requirements need to be defined for advanced area array electronics, both single and stack packaging technologies. An example of a ceramic quad-flat package (CQFP) failure due to lack of sufficient mechanical support is illustrated in Figure 2, which was taken from the NEPP website.

Figure 3 shows key reliability parameters under thermal and mechanical loading; it specifically shows details of failure mechanisms under mechanical loading for an area array package and assembly. Reliability investigation of array assemblies' behavior under mechanical loading becomes extremely important with the emergence of advanced field programmable gate arrays (FPGA) and their use in high-reliability applications. The high input/output (I/O) versions of these microelectronic devices are now available as a non-hermetic underfilled flip-chip ball grid array (FCBGA) or flip-chip column grid array (CGA). Exposure of brittle die and fragile columns are two aspects that further necessitate the characterization of these types of packages under mechanical loading in

addition to conventional thermal cycling. Since commercial industries are leading these technologies, especially those that are used in portable electronics, extensive data are available. The mechanical data generated from industry specifications generally uses fatigue bending and drop testing rather than under shock and vibration testing, as commonly performed for high-reliability applications.

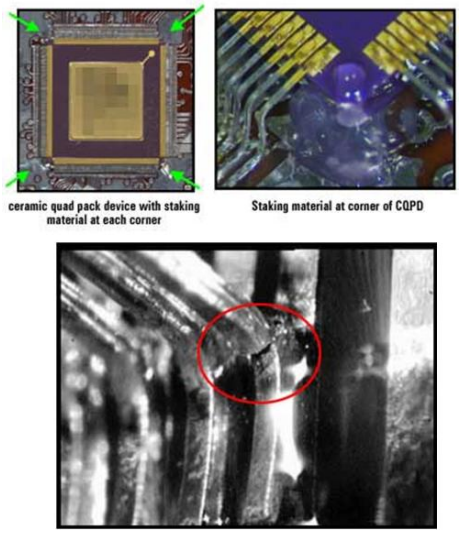

Figure 2. Lead failure for a CQFP under vibration loading due insufficient corner staking materials. (NASA Workmanship 8739.1, paragraph 4.4-3b].

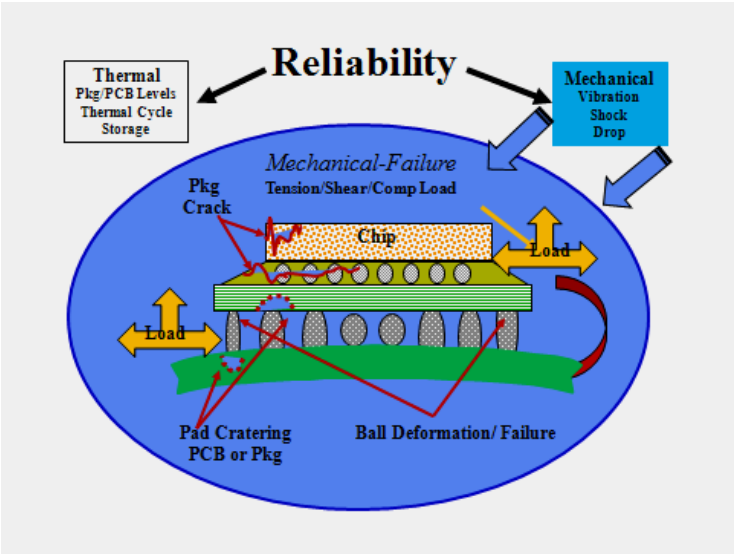

Figure 3. Thermal and mechanical reliability parameters, specifically showing failure mechanisms of advanced area array package assembly under mechanical loading, including shock and vibration.

This report presents a summary of the body of knowledge (BOK) on area array package evaluation, and is based on both current industry practice and a survey of the literature. Limited data, specifically generated for high-reliability applications covering shock and vibration and generated by a NASA-DoD industry team, is also presented. Key findings are.

- Most advanced electronic packages are plastic, rather than the ceramic version typically considered for high-reliability applications. Package-on-package becomes a popular choice for industry.
- Numerous specifications are developed by industry (IPC and JEDEC) to address mechanical reliability issues associated with use of advanced electronic packages, especially for mobile applications. These specifications are summarized and presented.
- Underfill, underfilm underfill, and edge-bond have been shown to improve resistance to mechanical drop tests by a number of authors.
- Vibration behavior of package assemblies are less studied and understood. Investigators agree that the fatigue life data from the traditional superposition approach (Minor's Rule) are not valid and generally overpredict projected fatigue life. For example, it was shown that the sequence of thermal cycle followed by vibration was harsher than vibration followed by thermal cycle.
- NASA-DOD test data regarding the mechanical shock and vibration performance of package assemblies with Pb-free and tin lead solder alloys were compared. In general, tin-lead performed better than Pb-free solder assemblies.

Given NASA's severe mechanical loading and fatigue requirements, understanding the key design guidelines acquired from the literature survey, test data, and failure mechanisms, in conjunction with complementary future test data, is critical to minimizing future failures. Such knowledge base allows in preparation for low-risk insertion of these advanced electronic packages.

2. Electronics Packaging Trend

Unlike early microelectronic technologies that aimed mostly at meeting high-reliability applications, consumer electronics is now driving the trends for electronic packaging and assembly. With that being the primary driver, materials and processes are transitioning to Pb-free solder alloy in order to enforcing restrictions on hazardous substances (ROHS) for electronics systems. While there is a drive to develop new low-k dielectrics and advanced organic substrate materials, the higher melting temperature of these solder alloys is pushing the limits of their reliability. High-reliability industry now uses specialty electronics, along with either adapted consumer electronics or their own tailored versions.

In the past, high-reliability applications always utilized ceramic versions of plastic packages, such as the plastic ball-grid-array (PBGA) or its analogous ceramic ball-grid-array (and column-grid-array) (CBGA and CGA). Today, there are fewer ceramic versions and they are generally lagging in technology compared to plastic ones. In fact, under thermal stresses, even though ceramic packages are individually more reliable compared to plastic BGA versions, they may not always be the most reliable choice when assembled onto polymeric board. This is due to a much larger coefficient of thermal mismatch. Solder joint reliability evaluation using a thermal cycling approach is well-established [2-6]. New specifications have recently been generated by industry to address robustness under thermal stress due to the expansion of portable electronics and insufficient mechanical resistance reliability ROHS solder alloys. Both thermal and mechanical reliability approaches are an integral part of the microelectronic packaging equation for overall system reliability, especially those to be considered for high-reliability applications [7].

Due to the breadth of work being performed in the area of microelectronics packaging, only a few key aspects of technologies are discussed. A number of technologies are first briefly reviewed; then, specific area array packaging trends (with an emphasis on high-reliability applications) are discussed in detail. In the brief description provided in this section, each technology and trend is illustrated using the associated package photos, meant to convey the complex multidirectional trends in technologies (Fig. 4). The x-axis of the graph represents time (from current to future) and the y-axis indicates technical capability. The technical capability embodies a combination of a number of factors, including the complexity and maturity of each technology. An arrow starting from the lower left corner and extending to the top right corner was added to indicate the movement from current low capability towards future high technical capability. Colored arrows with numbered labels represent different technology categories above. The numbers, from 1 to 4, suggest the status of development and/or availability, as follows: 1 = Development, 2 = Samples are available for evaluation, 3 = Low Production Volume and 4 = High Production Volume.

2.1 Single Chip Area Array Packages

The trend in single packaging technology is illustrated in Figure 4. Single chip packages such as BGAs and CSPs (chip scale package) are now widely used for many electronic applications, including portable and telecommunication products. The BGA version is now being considered for high-reliability applications with generally much harsher thermal and mechanical cycling requirements than those for commercial use. Technical challenges for

BGA/CSP packages, such as the behavior of solder joints under thermal and mechanical loading, have become a 'moving target' to meet development requirements in higher density die with its associated continuous increase in pin count (I/O), decrease in pitches, and newly introduced packaging styles.

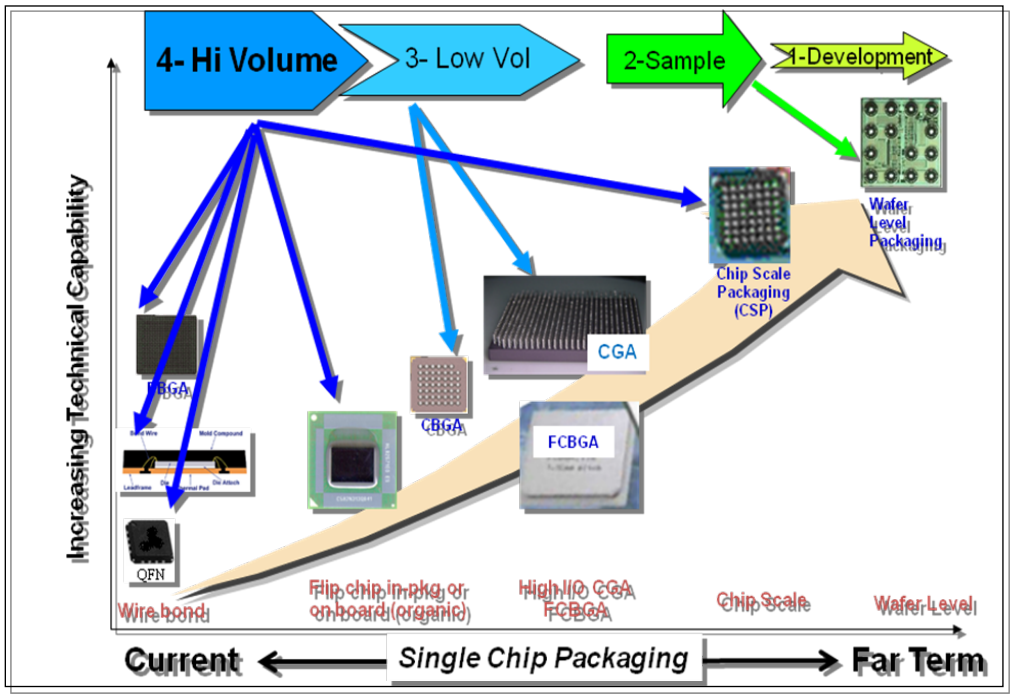

Figure 4. Microelectronic trends for single packaging technologies.

For high-reliability applications, there is a continuous need to understand behavior under mechanical and thermal stresses, because the I/O of CGA packages increases and becomes more complex using non-hermetic flip-chip die and added passives. Thermal stress due to column attachment for LGA and/or reworked CGA packages affects reliability. Assembly of LGA directly onto board using conductive adhesive may become a viable option in the near future, possibly using adhesives with nano-particulates (or other approaches) in order to improve resistance to mechanical loading and fatigue cycling. Thermal and mechanical characterizations of early versions of high I/O PBGAs with wire bond, as well as advanced higher I/O versions with flip chip die, are critical for certain harsh environmental applications. Evaluation of CSPs, including wafer-level CSP (WLCSP), should be selective since packaging technologies do not yet show the thermal and mechanical resistance robustness required for high-reliability applications. With a majority of commercial industry already implementing Pb-free solders in their products, there is now added complexity and challenge for high-reliability applications. The options for users of tin-lead solders are (a) continue to use tin-lead solder with Pb-free columns/solder balls (backward compatibility), (b) replace Pb-free balls/columns with tin-lead, or (c) accommodate Pb-free in the near future with an understanding of the associated risks, while continuing to develop mitigation approaches.

2.2 3D Packaging Technologies

The trend for 3D packaging technology is illustrated in Figure 5. For high-density packaging, the migration to 3D has become mainstream. Currently, 3D packaging consists of stacking packaged devices, called package-on-package (PoP), stacking die within a package called package-in-package (PiP), or stacking wire bonded die (primarily memory). Both technologies are used today with the promise of stacking die (without wire bonds) using through-silicon-via (TSV) technology. The technical issues for the 3D packages are both internal to package and external when these packages are assembled onto board, such as PoP.

For high-reliability applications, there is a need to narrow selection of PoP and PiP packages for harsh environmental applications based on thermal resistance robustness. Such focused evaluations should include 3D wire bond stack package technology, but also monitor the progress of TSV being developed for high-density and high-frequency applications. PoPs require new process development, so key implementation issues shall be identified and optimized for high-reliability applications.

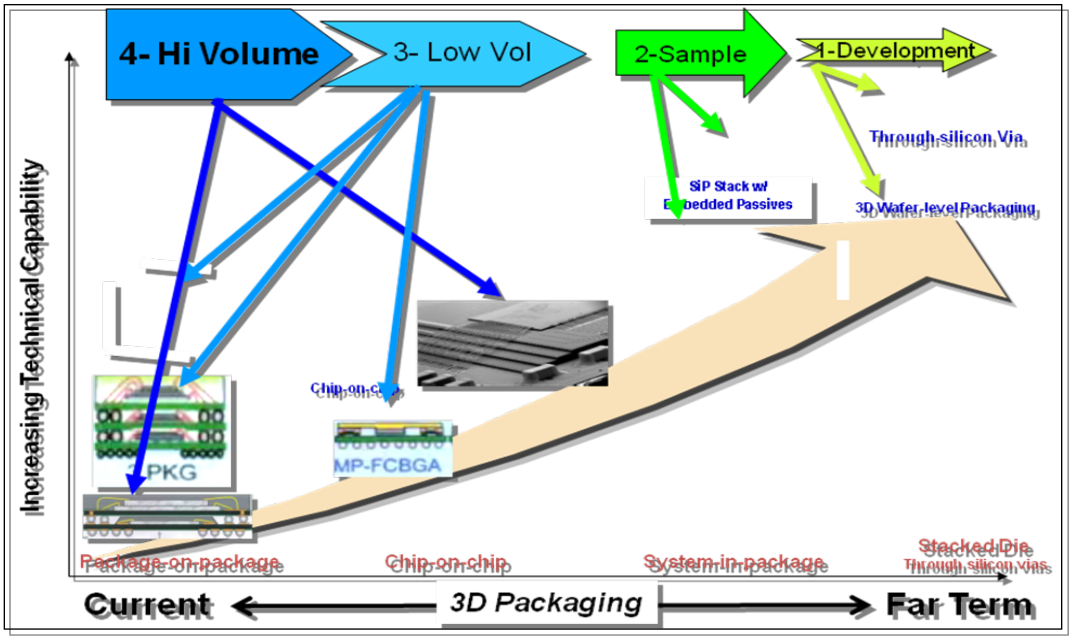

Figure 5. Microelectronic trends for 3D packaging technologies.

3. Reliability under Mechanical Testing

3.1 Introduction

Reliability is the ability of a system (here microelectronics) to function as anticipated under the expected operating conditions for an expected time without exceeding the expected failure levels. However, reliability is threatened by infant mortality due to workmanship defects and the lack of sound manufacturing and reliability design. Designs for manufacturability (DfM), design for assembly (DfA), design for testability (DfT), and so on,

are prerequisite to assure the reliability of the product. Only a design for reliability (DfR) can assure that manufactured to quality will be reliable. The elements of system reliability are the device/package/PCB and their interconnections, consideration of design for reliability prior to assembly and subsequent manufacturing, and quality assurance implementation (Fig. 6).

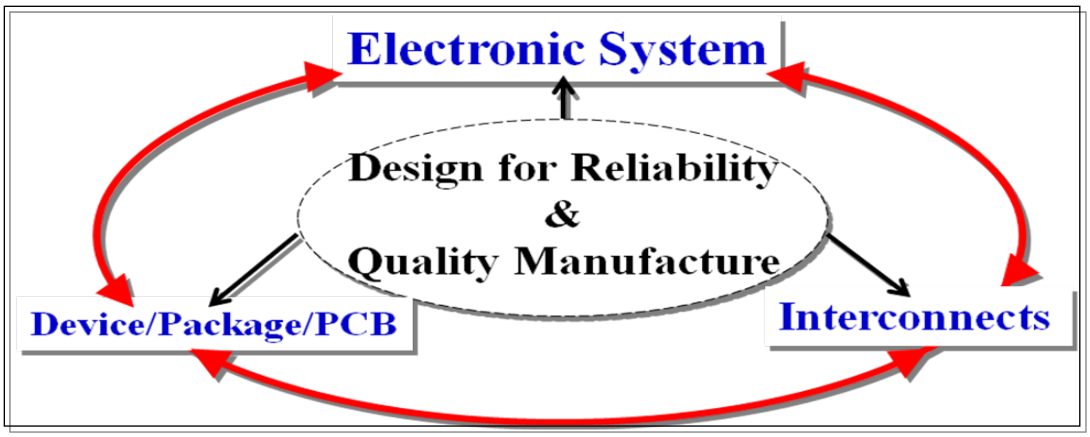

Figure 6. System reliability achieved through design for reliability (DfR), sound manufacturing, and quality, including packaging/device/PCB and interconnections.

Stresses are induced at various steps of manufacturing, testing, and environmental exposures, and during application can cause failures due to overloading or wear out the mechanism by fatigue cycles. Stress induced during the packing process could cause cracking of the die and package or interconnection failure due to overloading. On the other hand, lower loading could cause fatigue failures due to repeated thermal cycling or mechanical loading exposures. Physics-of-failure for each case is different and in some cases may contradict each other; compromised optimization may be required to accurately assess their effectiveness. Figure 7 presents key parameters affecting reliability under thermal and mechanical loading, with an emphasis on mechanical loading and failures.

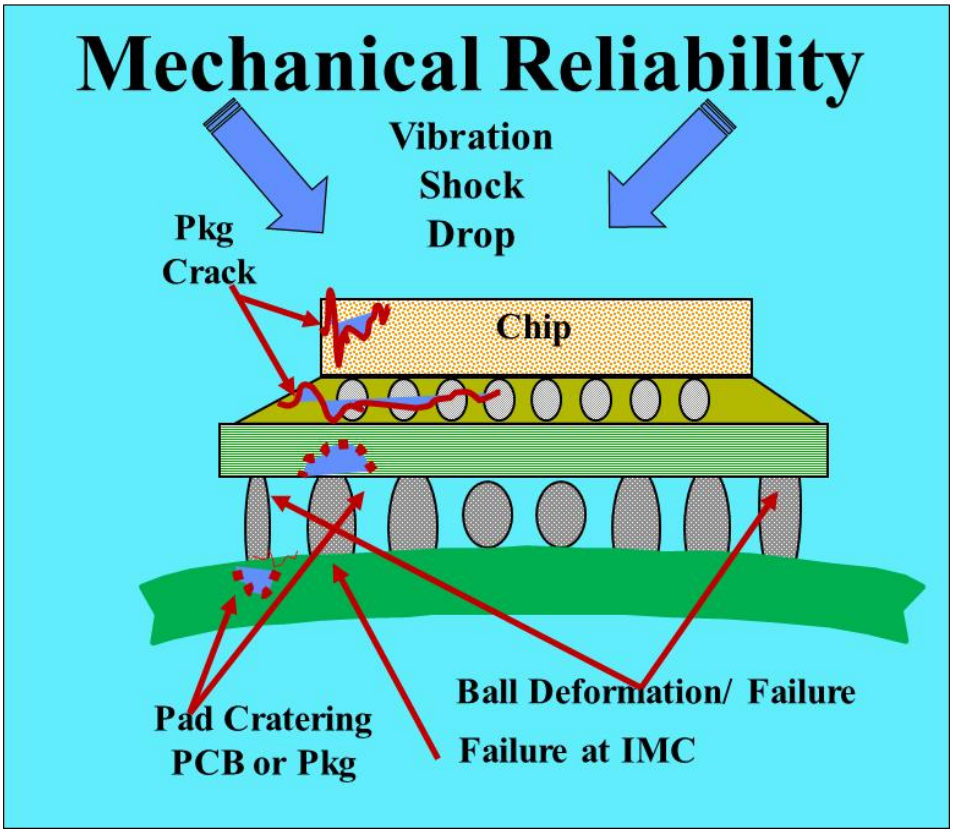

Figure 7. Typical mechanical reliability test methods and failure mechanisms for area array package and assembly.

Solders in surface mounts are unique since they provide both electrical interconnection and mechanical load-bearing elements for attachment of package on PCB [8]. A solder joint in isolation is neither reliable nor unreliable; reliability has meaning only in the context of interconnections, either within the package or outside of the package on PCB. Solder joints are a key interface element for FBGA package and assembly on PCB. Three elements play key roles in defining reliability for FPBGA/FCBGA: global, local, and solder alloy. In FBGA, solder balls also act as a load-carrying element between package and boards, similar to metallic leads (e.g., QFP). The characteristics of these three elements—package (e.g., die, substrate, solder joint, underfill), PCB (e.g., polymer, Cu, plated through hole, microvia), interconnections (e.g., solder joints, via, balls, underfill)—together with the use conditions, the design life, and acceptance failure probability for the electronic assembly determine the reliability of FBGA/FCBGA assemblies.

Area array packages, in general, and flip-chip dies and FPBGA specifically, lack thermal and mechanical resistance generally observed for PTH and leaded package assemblies soldered with $Sn_{37}Pb$ alloys. Lack of reliability resistance is further aggravated with the use of lead-free solder alloys, especially under harsh thermal cycling and dynamic loading such as drop and vibration. Mechanical stress condition may induce additional failure to those induced by thermal cycling, including solder joint brittle fracture and PCB/Package pad interfacial failures. For these reasons, new specifications are being generated by industry to

better characterize SMT materials properties (package, PCB) and strain limitation (PCB, solder), as well as methods of defining mechanical resistance to repeated mechanical loading such as drops. Key specifications will be discussed first, followed by test data on reliability of various package assemblies subjected to various types of mechanical loading.

3.2 Specification on Mechanical Testing

Figure 8 lists a number of specifications generated in recent years by commercial industry, particularly for IPC [9] and JEDEC [10] in response to increasing demands on area array packages and their miniaturized versions and stack technologies. It also includes the key military specification [11] that was recently updated (in 2008).

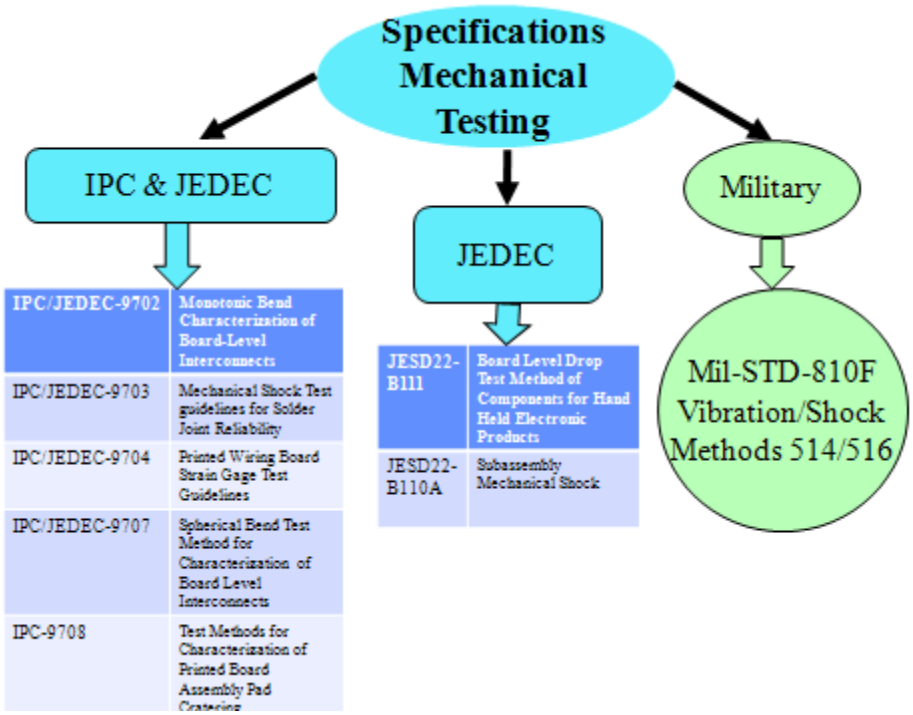

Figure 8. Key Commercial and military specifications for mechanical testing, including those that define bending, drop, vibration, and shock behavior of microelectronics, advanced area array packages and 3D packaging technologies.

The key specifications that are relevant to this BOK are as follows.

- IPC/JEDEC 9702 covers basic mechanical bend testing characterization and strain to failure using four points, a bend test method commonly used by industry. Specific strain gage attachment is delineated in IPC/JEDEC-9704.
- IPC/JEDEC 9707 covers a new test method that is more applicable for area array packages, using spherical loading at points rather than loading through cylindrical rod as used in four point bend testing defined in 9702. This standard supplements existing standards for mechanical shock during shipping, handling, or field

operation, as well as filling the gap for IPC/JEDEC 9702 to better characterize maximum strain levels. The two specifications provide a common method of establishing the fracture resistance of board-level package interconnects to flextural/point loading during PCB assembly and test operations. No pass/fail qualification requirements are provided, since each package/assembly is considered unique.

- IPC 9703 covers generic guidelines for mechanical drop and shock testing, because the requirement for each industry is different. The scope of document includes 1) methods for defining mechanical shock use conditions, 2) methods to define system level and system board level component testing that correlates to the use conditions, and 3) guidance on the use of experimental metrologies for mechanical shock tests.
- IPC 9708 is generated in response to newly observed board failures (pad cratering) resulting from the move to implement Pb-free solder alloys. Pb-free solders are generally stiffer than tin-lead solders; they can transfer more of the applied global strain to the assembly. The Pb-free approach requires higher reflow temperatures that induce higher residual stress/strains in the assembly. Pb-free is typically assembled with phenolic-cured PCB materials that are more brittle than conventional dicy-cured FR4 materials. These strains could eventually relax over time, but if mechanical strain is applied shortly after reflow, pad cratering could occur at lower mechanical strain levels.
- JEDEC JESD-B111 was developed for portable electronics in response to the need to define resistance to repeated drops, which is required for mobile applications. Shock pulse requirement to PCB assembly is defined based on JESD22-B110 condition B Table 1 (or JESD22-B104-B Table 1) with 1500 Gs, 0.5 millisecond duration, and half-sine pulse. This specification is widely used by industry and data are of valuable for high-reliability applications. JESD-B210A defines resistance to mechanical shock.
- Mil-STD-810F covers many aspects of environmental testing, including mechanical vibration and shock, and is well established for conventional microelectronics for high-reliability applications.

BOK on test data gathered by industry using these specifications is presented in the following section.

4. Test Data on Reliability

4.1 Monotonic Bend Test Data

Specification IPC/JEDEC 9702, Appendix A, documents allowable PCB strains during board assembly and test operations in order to eliminate brittle fracture in production. A series of linear plots of strains vs. strain rates provided guidelines to understand the limitation on strains considered to be "acceptable" in the lower regions; in other words, strains that would not be expected to result in solder joint failure. Later, these plots were better defined by expanded availability of test data and the use of projection by finite element analysis.

Figure 9 show a recent plot of strains vs. strain rates presented in literature [12], but yet to be included in the specification IPC 9702. Strain values are based on the lower limit of the fracture strength distribution of test data (approx. Average X-3 sigma), not the average number of failures (63%) generally reported for cycles-to-failure. The author cautions that fitted plots are primarily based on empirical data, are not fundamentally a physics-based model, and are therefore limited to specific test conditions. Extrapolation to any other conditions need to be verified since allowable levels are based on PCB deformation, not solder interconnection due to difficulty of strain gage attachment to solder. The strain rate induced during monotonic bend test conditions, as defined in IPC/JEDEC 9702, represents the rates (1,000–30,000 $\mu\varepsilon$/s) associated during typical PCB board assembly, handling, and test conditions. This range; however, is 1 to 2 orders of magnitude lower than strain rates associated with a drop impact condition. One example of monotonic strain measurement is given below, before discussing a new approach of measurement by acoustic emission.

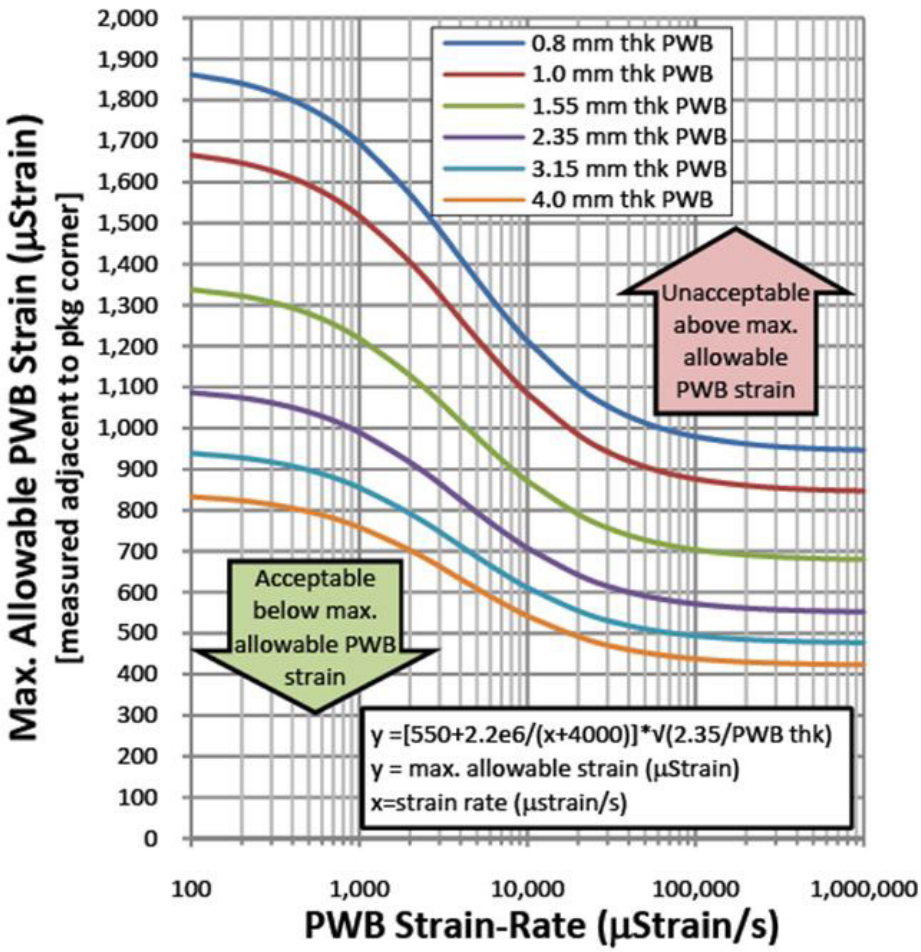

Figure 9. Maximum allowable PCB strain versus PCB strain rate (Courtesy Keith Newman, reference, see IPC 9704, Appendix A).

Strain measurement techniques and monotonic bend tests per IPC/JEDEC 9702 were carried out to determine board-level solder joint reliability for two large CBGA and PBGA packages [13]. CBGA2400 I/O, 51 × 51 mm, had 0.7 mm-SAC387 balls and the PBGA1517, 40 × 40 mm, had 0.6 mm-SAC305 balls, both assembled with SAC305 solder paste onto 90 × 250 mm flexural board with 6 layers of 2.35 mm thickness. Via in pad was used for CBGA and conventional NSMD dog-bone via for PBGA. Effect of edge-bonding on corner of package was also evaluated. Evaluation performed from plots of data gathered during testing by monitoring continuity in package daisy chain, by changes in monotonic microstrains (με) from strain gages at corner and away from BGAs, and interruption in micro strain rates from the nominal of 5000 με/s. Table 1 summarizes test results taken from various plots given in the papers.

Table 1. Monotonic bend test results (based on IPC 9702) showing bending forces and maximum strains to failures for large ceramic/plastic BGA (CBGA/PBGA) package assemblies, with and without edge-bond epoxy.

Package Type	Bending Force Newton	με Daisy Chain
CBGA 2400 I/O	930	~ 3000
CBGA-100% Edge-Bond	1303	~ 5000
PBGA 1517 I/O	1187	~6000
PBGA-100% Edge-Bond	1498	~7000

Author was able to show a correlation between strain rate plots for PCB strain gage values and the interruption in daisy chain packages monitored during flexural testing. Plots revealed consistent results between strain rate interruptions and daisy chain discontinuity for packages without edge bond. However, for edge-bonded packages, only the onset of failure epoxy fractures clearly could be identified, not daisy-chain failure. The author concluded that strain-rate plot is a "useful-indicator" for failure projection of different packages, with and without edge bonding adhesives.

A new monitoring approach based on acoustic emission (AE) was found to be effective in detecting early initiation of pad crating (fine cohesive cracks under BGA) using IPC/JEDEC 9702, the monotonic bend testing method [14]. The IPC 9708 specification provides qualitative testing that characterizes the integrity and failure behavior of PCB pads by pull testing; therefore, ranking PCB's propensity to pad cratering before use. Pad cratering cracks initiated during assembly and testing are not detectable by electrical testing or non-destructive inspection methods. Pad cratering pose a long-term reliability risk since the cracks generated under the PCB pad may propagate under subsequent testing and application.

The IPC 6–10d team, during its annual meeting at IPC APEX2012, invited the principal author of the AE paper, "Investigation Pad Cratering in Large Flip-Chip BGA using Acoustic Emission," [14] to present his findings to the team for review. The AE evaluation was performed using a 40 × 40 mm FCBGA 1521 I/O package with Pb-free SAC305 solder balls and 1-mm pitch, assembled onto 8-layer PCB with 93-mil thickness. AE sensors were attached to four-point bend test vehicles to detect the onset of either pad cratering or brittle IMCC failure. The investigation included the effects of other parameters including normal or diagonal package attach and strain, NSMD or SMD PCB pads, and single or multiple reflow cycles. Table 2 summarizes the effects of key parameters on microstrain measurement by electrical and acoustic emission failure criteria. The microstrain values are always lower from AE compared to electrical measurements. Based on plotting the data, the authors

conclude that for pad cratering, the maximum strain is estimated to be 1250 με, but for the IMC brittle fracture this value is lower, estimated to be about 860 με.

Based on favorable test results with AE methods, the 6–10d team decided to have follow-up teleconferences on this topic to better define the details of this technique. Information was released either with standard test methods or as a guideline document supplementing the strain gage method. The IPC website can be reviewed for updated and progress on this activity.

Table 2. Monotonic bend failure test results performed on IPC 9702 using daisy-chain electrical methods and a new approach by acoustic mission (AE).

FCBGA 1517 I/Os SAC 305 Balls	µStrain Electrical	µStrain Acoustic
0°, NSMD, 3x reflow	~2800	~ 2000
45°, NSMD, 3x reflow	~ 3250	~ 1800
45°, SMD, 3x reflow	~ 2250	~2100
45°, NSMD, 1x reflow	~3500	~2000

4.2 Bend Fatigue Test Data

The four-point bend fatigue test simulates the key strokes in mobile electronics applications, where repeated strokes could result in considerable flexure of printed circuit board and package assembly. In earlier evaluations, the tin-lead behavior of FPBGAs and CSPs was characterized. For example, in reference 15, the behavior of a chip-scale package with 0.8 mm pitch subjected to a four-point cycling bend test, was evaluated after initial optimization of the span and assurance of uniformity of strain within the span. The initial strain gage evaluation indicated that the number of components on the board has a negligible impact on the board strains when the components are at least 10 mm apart. Board-to-board variation in strain data was attributed to board initial warpage or twist, board residual stresses, or board hysteresis. It is recommended that multiple boards should be tested to account for the board variation. The effect of board (1 mm thick) deflection (1.5 to 4 mm) was investigated first, followed by the effect of loading frequency, 1–5 Hz, for a constant deflection value of 2 mm. For lower deflection levels, the failures are dominated by solder joint mechanical fatigue failure. However, at large deflection levels, the failure mode changes to board failure, demonstrated by trace breaking and pad rip-off. Reading the plot, it is estimated that board με is about 300 times greater than board deflection in mm, e.g., a deflection of 2 mm of PCB is equivalent to strain of 600 με for PCB. FEA was used to estimate the total strain energy for solder joints. It was determined that the maximum strain locations were at the outermost

rows of solder balls with depopulations. For tin-lead eutectic solder, relationship between number of cycles to failure by four point bend test and strain energy at solder joint is given by: $N= C(\Delta W_{Total})^{-1.8}$.

With wider use of lead-free, authors started initially to compare behavior of tin-lead solder with Pb-free, late only evaluation of Pb-free. For example [16], four-point bend test was used to compare fatigue for tin-lead (63Sn37Pb) and Pb-free solder (95.5Sn4.0Ag0.5Cu, SAC405). A single PBGA256, 1.27 mm pitch, was assembled onto 1 mm thick PCB for testing under loading from 25 to 60N. No deflection information was give. Results indicate relative fatigue trend changes for tin-lead and Pb-free solder alloys depending on loading cycle. At higher loading, tin-lead solder performed better than Pb-free. This was reversed for lower loading or higher number of cycles to failure. For example, for 60 N loading, tin-lead performed 1.66 times better—9400 versus 5600 for SAC405. At 25 N, tin-lead failed at 220,000 and SAC405 at higher values of 240,000. Relationships between cycles to failure and inelastic energy dissipate in solder were determined by FEA. For tin-lead this was $N= 12152(\Delta W_{in})^{-1.1}$ and for SAC405 was $N= 54094(\Delta W_{in})^{-0.84}$.

4.3 Drop Test Data

JESD22-B111 for board drop test is a test intended for portable application; it is useful solder joint fracture for packages smaller than 15 mm. JESD22-B110A is more suitable for larger packages and use conditions using the appropriate machine type, i.e., with acceleration shock profile conditions under half-pulse loading.

Extensive work has been carried out by various investigators to address the weaknesses of area array packages under mechanical loading and to propose improvements that can be achieved by underfilling and edge-bond bonding. Only a few aspects of the investigation are discussed here to shed some light on the effects of key parameters that affect drop reliability. In the early stage of portable electronics, thermal cycle reliability was shown to meet many consumer application requirements. [17]. However, fine pitch BGA and CSPs have difficulty with mechanical shock and substrate flexing tests for portable electronics applications. A test vehicle with 4 FPBA having 108 balls and 0.8 pitch, 10 × 10 mm package with 5 × 5 mm die was assembled on thin board (.039 inches) without underfill, fast cure, or reworkable underfills. The vehicle experienced a total of ten drops from a height of 6 feet. Repeated flexure testing was also performed at twice the radius size that caused failure of the board during monotonic bending (17.5 and 8.76 inches).

Test conditions and results are summarized in Table 3. Even though test results for thermal shock did not show a clear trend, significant improvement in mechanical performance was achieved with both the reworkable and non-reworkable underfills. The reworked process improved mechanical performance. Use of underfill did not alter thermal shock performance and was thought to be the result of voids due to residual flux. Void content decreased with a nitrogen reflow atmosphere.

Table 3. Summary of test results for FPBGA with and without underfill.

FPBGA 108 I/Os 0.8 mm Pitch	TS Failure (–40/125°C)	10 Drops (6 feet)	Flex (1/2 Max Deflection)
No Underfill	~1000	100%	113
Underfill A (3566)-Fast Flow	~1000 (voids)	No Failure	>1250
Underfill B (3567) Reworkable	>3000	30%	>1250
Underfill B Reworked	NA	10%	> 5000

In a later investigation [18], the number of drops to failure was investigated for a tape-array CSP package, 8-mm, 0.5 mm pitch, with 132 I/O. At 10 percent failure, no underfilled crossed the failure line at 2 drops, corner bond at 5 drops, and full capillary underfill at 10 drops. The authors concluded that corner bond underfill provides a 3- to4-fold improvement compared to no underfill. Corner bond underfill is a viable, cost-effective approach for many portable product applications.

Drop testing was carried out to assess the resistance of MAPBGA with and without underfilm underfill [19]. A number of test vehicles assembled with 338 I/O 11x11 mm MAPBGA and 0.5 mm pitch using Pb-free SAC305 and preformed underfilm were subjected to thermal cycling (0 to 100C) and drop testing at 1,500 g with 0.5-millisecond duration per JEDEC. There were no failure of assemblies to 3000 cycles and 100 drops. Later, the drop g level increased to 3,500 g in order to induce failures. Based on all test results, the author concludes that 8-fold or higher improvement in drop resistance is achieved when underfilm material is used at the 3,500 g level. Underfilm had no degradation in thermal cycling performance.

Conventional drop towers typically have a limit of 5,000 g, which is sufficient for mobile applications. However, testing at very high g-loads may be required for high-reliability applications. To facilitate the need for higher g-levels, an added fixture called dual mass shock amplifier (DMSA) has been developed, enabling testing up to the 100,000 g level. A DSMA fixture was used to subject daisy-chain PCB package assemblies to low-to-high g levels to characterize damage initiation and progression in interconnects [20]. Peak shock pulse magnitudes ranged from 1,500 g to 50,000 g. Only shock drop data and failures for CGA400 package assemblies were presented. Peak strains (at the PCB bottom, center) at 3,000 g and 50,000 g levels were empirically measured and reported to be 3,331 με and 7,251 με, respectively.

No failure of two CGA assemblies was observed at 3,000 g for 120 drops. At much higher g levels, failures did occur and the number of drops-to-failure decreased with increasing g levels. The mean number of drops for 30,000, 40,000, and 50,000 g level tests were 7.2, 5.4, and 4.2, respectively. Failure analysis by high-power microscope revealed their failure occurrence at the corner interconnects, either at solder fillet or close to the center of columns. Necking of the failed solder columns is an indication that failure has been caused by axial pulling of the solder column. Authors used a global local modeling approach by finite element model and found a good correlation with experimental strain, displacement, and failure modes.

4.4 Shock

Recently, shock testing of PBGA and other electronic assemblies with tin-lead and Pb-free solder was performed based on MIL-STD-810F, Method 515.5 with modification [21, 22]. The purpose was to determine the resistance of solder alloys to the stresses associated with the high-intensity shocks representative of high-reliability applications. A step stress shock test was performed to maximize the number of failures generated, which allowed comparisons of solder reliability. Modifications allowed testing to continue until a majority (approximately 63 percent) of components failed. The electrical continuity of the solder joints was continuously monitored during the test.

The overall results of the mechanical shock testing are summarized in Table 4. If a solder alloy/component finish combination performed as well or better than the SnPb control, it was assigned the number "1" and the color "green". Solders that performed worse than the SnPb control were assigned a "2" and the color "yellow". For those cases where both the SnPb controls and a Pb-free solder had few or no failures after 900 shock pulses, they were not ranked.

Table 4. Comparison of tin-lead and Pb-free solder joint reliability based on repeated and increasing shock levels [courtesy NASA-DOD Project, Reference 21].

Component	Sn37Pb/Sn37Pb	SAC305/SAC405	Sn37Pb/SAC405	SAC305/Sn37Pb	Rwk Flux Only /Sn37Pb	Rwk Flux Only /SAC405	Rwk Sn37Pb/SAC405 (SnPb Profile)	Rwk Sn37Pb/SAC405 (Pb-Free Profile)		
BGA-225	1	1	2	1	1	1	2	1		
Component	**Sn37Pb/Sn37Pb**	**SAC305/SAC305**	**Sn37Pb/SAC305**	**SAC305/Sn37Pb**						
CLCC-20	1	2	2	2						
Component	**Sn37Pb/Sn37Pb**	**SAC305/SAC105**	**Sn37Pb/SAC105**	**SAC305/Sn37Pb**	**Rwk Flux Only /Sn37Pb**	**Rwk Flux Only /SAC105**	**Rwk Sn37Pb/SAC105 (SnPb Profile)**	**Rwk Sn37Pb/SAC105 (Pb-Free Profile)**		
CSP-100	1	1	2	1	2	1	2	2		
Component	**Sn37Pb/SnPb**	**SN100C/Sn**	**Sn37Pb/NiPdAu**	**Rwk Sn37Pb/Sn**	**Rwk SN100C/Sn**					
PDIP-20	1	1	1	2	2					
Component	**Sn37Pb/Sn37Pb**	**SAC305/Sn**	**Sn37Pb/Sn**	**SAC305/Sn37Pb**						
QFN-20	Not enough failures to rank	Not enough failures to rank	Not enough failures to rank	Not enough failures to rank						
Component	**Sn37Pb/Sn**	**SAC305/Sn**	**Sn37Pb/NiPdAu**	**SAC305/NiPdAu**	**Sn37Pb /Sn37Pb Dip**	**SAC305 /SAC305 Dip**				
TQFP-144	1	1	1	1	1	2				
Component	**Sn37Pb/SnPb**	**Sn37Pb/Sn**	**Sn37Pb/SnBi**	**SAC305/Sn**	**SAC305/SnBi**	**SAC305/SnPb**	**Rwk Sn37Pb/SnPb**	**Rwk Sn37Pb/Sn (SnPb Profile)**	**Rwk Sn37Pb/Sn (Pb-Free Profile)**	**Rwk SAC305/SnBi**
TSOP-50	Not enough failures to rank	Not enough failures to rank	Not enough failures to rank	Not enough failures to rank	Not enough failures to rank	Not enough failures to rank	2	2	2	2

The rankings in the table are somewhat subjective since the data for some component types contained a lot of scatter while other component types had few failures, which complicated the ranking process. In addition, if some of the component/solder combinations had only a few early failures, these failures did not count in the ranking process. In general, the pure Pb-free systems (SAC305/SAC405 balls, SAC305/SAC105 balls, SAC305/Sn, and SN100C/Sn) performed as well or better than the SnPb controls (SnPb/SnPb or SnPb/Sn). For mixed technologies, SnPb solder balls combined with SAC305 paste (and reflowed with a Pb-free profile) performed as well as the SnPb controls on both the BGAs and the CSPs. In contrast, SnPb solder paste combined with either SAC405 or SAC105 balls (and reflowed with a SnPb thermal profile) underperformed the SnPb/SnPb controls.

Rework operations on the PDIPs and TSOPs reduced the reliability of both the SnPb and the Pb-free solders when compared to the unreworked SnPb/SnPb controls. In contrast, rework of SnPb and SAC405 BGAs and SAC105 CSPs using flux only gave equivalent performance to the unreworked SnPb/SnPb controls. Pb-free BGAs reworked with SnPb paste and SAC405 balls (and a Pb-free thermal profile) were equivalent to the SnPb controls.

4.5 Harmonic and Random Vibration at Room and High Temperatures

In reference 23, authors state that a literature search reveals that even though four point and three point testing have been performed by researchers at room temperature (RT), there is no research at higher temperatures. Bending tests carried out both at RT and 125°C for a very thin quad flat no-lead (VQFN), 48 solder pin, assembled on board with OSP and Ni/Au surface finishes using Sn-Ag-Cu Pb-free solder. Using FEA and test results at RT and 125°C, the relationship between averaged life and plastic strain energy density was established. These relationships for RT (25°C) and 125°C are: $N_{(25°C)} = 6.414\ (\Delta W_P)^{-0.935}$ and $N_{(125°C)} = 0.032(\Delta W_P)^{-1.92}$ where (ΔW_P) is plastic strain energy density accumulation per cycle. The power law exponent of the high-temperature bending fatigue model (1.92) is about twice the exponent of the room temperature bending fatigue model (0.935), which indicates that the acceleration factor of cycle to failure is larger in high-temperature bending fatigue than in room temperature bending fatigue.

For high-reliability applications, use of vibration as one of the environmental requirements is common and well established. However, there is less data on characterization of advanced electronic package assemblies under vibration, since they are yet to be fully utilized for high-reliability applications. There has been limited research by universities because it is difficult to interpret complex vibration loading, especially with random vibration and inclusion of other environmental exposures, such isothermal aging and thermal cycling. In reference [24], there is a review of investigations in the area of vibration for electronic packages, irrespective of types of packages. The investigation was divided into four categories.

1. Those using an empirical model to estimate package life under vibration—the formulas have little or no correlation to the underlying physics or dynamics of the problems.
2. Those using analytic models that are based on the physics and dynamics of the problem, but generally involve simplifying the assumptions,

3. Those relying primarily on finite element modeling.
4. Those relying primarily on experimental approaches, correlating with FEA analysis.

For combined sequential or combined thermal cycling and vibration, test data indicates that a simple linear superposition of damage (Minor's rule) is not applicable. For example, in reference [25], the authors investigated inelastic behavior of solder joints under concurrent vibration and thermal cycling. They reported observations from a series of concurrent thermal cycling and vibration tests on 63Sn/37Pb solder joints of an actual ball grid array (BGA) package and compared them with pure thermal cycling test results. They observed that although thermal deformation is the dominant feature of solder joint behavior, vibration significantly modifies the total behavior of solder joints under concurrent stresses.

In another reference [26], the authors developed a nonlinear damage model to account for non-linearity of thermal cycle and vibration. Figure 10, taken from this reference, shows the effect of sequential vibration and thermal cycling (vibration/thermal cycle alone, or one before the other one) in comparison to test data. It is apparent that the T-V sequence (thermal cycling followed by vibration loading) was a harsher sequence than the V-T sequence (vibration loading followed by thermal cycling). The difference was attributed to the severe deformation and microstructural changes that occur in thermal cycling, which initiate cracks quickly and quicken the subsequent vibration loading. A nonlinear cumulative damage model was developed to account for the sequence effect. This was done to predict remaining fatigue life for this type of package assembly after it has experienced some level of damage from a prior environment, such as transportation or preconditioning. Authors go on to state that the methodology, developed in this work, has the potential for application for other electronic packages and environments.

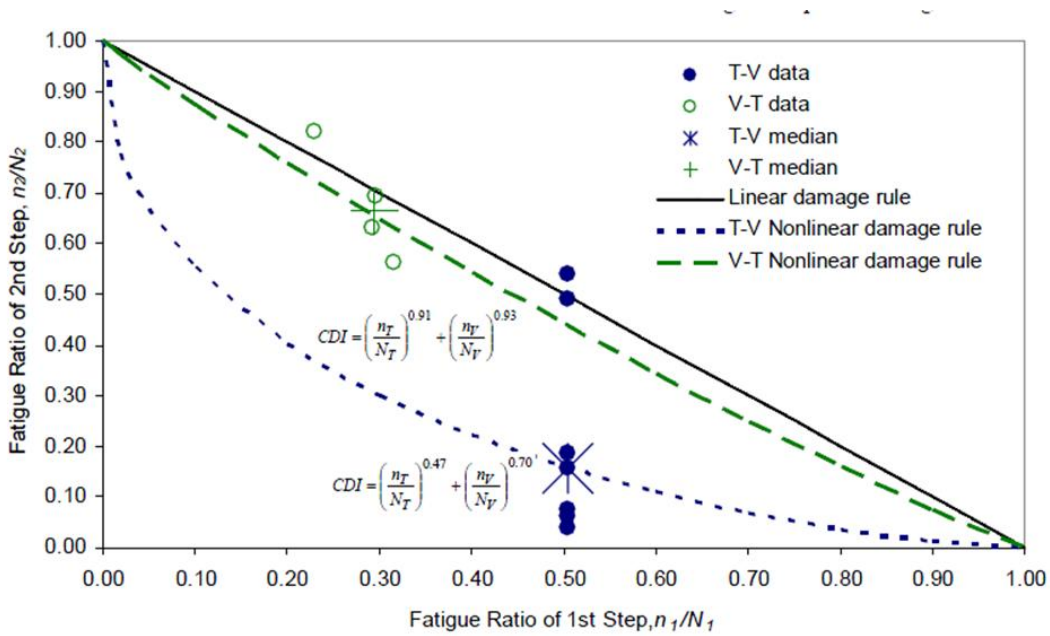

Figure 10. Plot of n_1/N_1 vs. n_2/N_2 for sequential loadings T-V (thermal cycle followed by vibration) and V-T (vibration followed by thermal cycle), along with linear and nonlinear damage models (courtesy IEEE, Perkin).

In reference [27], the authors found that characterizing the fatigue life by the traditional linear superposition approach was over-predicted, compared with the effectiveness of either linear damage superposition or incremental damage superposition approach. In their study, the solder interconnect reliability of PBGA assemblies was examined through test and simulation under multiple environmental loading conditions: temperature cycling alone, vibration loading alone, and combined thermal cycling and vibration loading. The results showed that the PBGA interconnect failed sooner under the combined application of random vibration and temperature cycling than with either separate vibration loading or temperature cycling. Therefore, they concluded that the incremental damage superposition approach, which considers the temperature-imposed load state on vibration damage, more accurately estimates the life expectancy of the critical PBGA solder joint under combined temperature cycle and random vibration, as opposed to the linear superposition approach.

In a recent paper in 2012 [28], several investigators reviewed studies on vibration, with a focus on combined environmental approaches. An earlier joint paper by the same author asserted that an incremental superposition approach (ISDA) takes into consideration the nonlinear interaction between vibration stresses and thermomechanical stresses. Test results showed that the fatigue damage was more vulnerable to vibration stresses alone than with combined stresses. The most recent investigation performed to determine the effect of temperature on vibration durability of SAC305 PCB assemblies of a chip scale thin core ball grid array (CTBGA) was also presented. Three different temperatures tested included room temperature (25°C), high temperature (125°C), and cold temperature (–40°C). Figure 11 shows test results only for RT and high temperature, since at lower temperature the fixture and table excitation spectrums did significantly change, contrary to the condition for RT and high temperature. At high temperature, vibration durability has much shorter than durability at RT due to changes in solder fatigue properties and the strain-rate effect of modal frequency. The author stated that vibration durability at lower temperature will be gathered in the future even though the post processing of durability data at lower temperature will be much more complex—the fixture and table excitation spectrums change significantly from room temperature to low temperature.

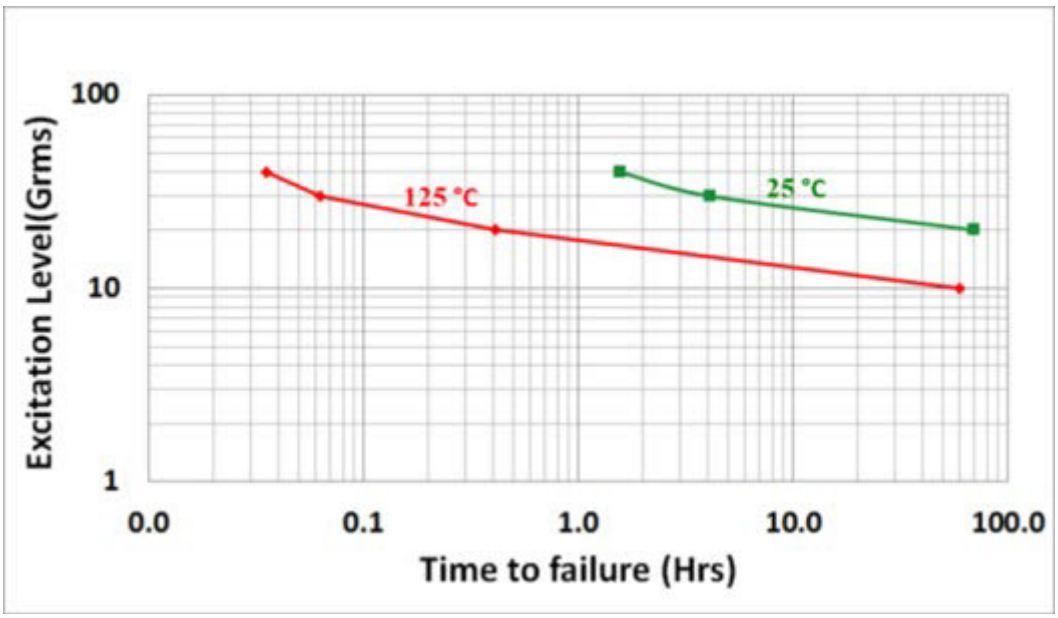

Figure 11. Vibration fatigue, g level versus hours to failure, at two RT and 125°C.

In another paper presented at the IEEE Itherm 2012 [19], authors discuss the criticality of electronic components mounted on automotive systems that are exposed simultaneously to high temperature and dynamic loads. Both high temperature and vibrations contribute to failures in such systems. The author states that most of the research covers the reliability of electronic systems subjected to either vibrations or thermal cycling independently. Relatively few researchers have studied reliability in the environment of simultaneous thermal cycling and vibration. There is a lack of fundamental understanding of reliability of electronic systems subjected to extended periods of vibrations at elevated temperatures. The authors presented their studies on the reliability of Pb-free alloys under similar combined environments.

Two test vehicles, one with various package styles and one with a single BGA package, were assembled with SAC305. The vehicles were subjected to out-of-plane harmonic vibration at their first natural frequency inside of an isothermal chamber. Full field displacement and deformation gradient on PCB was measured by digital image co-relation (DIC). Even though photograph and ID of package used was given, but from plots of cycles to failure with temperature variation (25°C, 85°C, and 125°C), the package type for each plot is still not clear. An accurate interpretation of the fail data was not possible because the cycles-to-failure is different for each package. This is due to the associated strains being different for different locations. Typical failure modes observed were:

- Quad flat packages (QFPs) are copper lead deformation and lead cracking.
- Thin small outline packages ($TSOP_S$), with more rigid leads have failed at the solder joints without significant lead cracking, though some lead deformation is observed in the corner leads.
- Plastic ball grid arrays (PBGAs) showed solder ball cracking at copper traces, revealed by cross-sectioning.

Recently, a NASA-DoD team [21] presented vibration test data based on the general requirements of MIL-STD-810F, Method 514.5, both for Pb-free and tin-lead solder alloys. The limits identified in the vibration testing were used to compare performance differences in the Pb-free test alloys, as well as mixed solder joints vs. the baseline standard SnPb (63/37) alloy. The following procedures were considered:

- Place the PCBs into a test fixture in random order and mount the test fixture onto an electrodynamic shaker.
- Conduct a step stress test in the Z-axis only (i.e., perpendicular to the plane of the circuit board). Most failures will occur with displacements applied in the Z-axis, which will result in maximum board bending for each of the major modes.
- Run the test using the stress steps shown in Figure 12. Subject the test vehicles to 8.0 g_{rms} for one hour. Then increase the Z-axis vibration level in 2.0 g_{rms} increments, shaking for one hour per step until the 20.0 g_{rms} level is completed. Then subject the test vehicles to a final one hour of vibration at 28.0 g_{rms}.
- Continuously monitor the electrical continuity of the solder joints during the test using event detectors with shielded cables. All wires used for monitoring were soldered directly to the test vehicles and then glued to the test vehicles (with stress relief) to minimize wire fatigue during the test.

A step stress test is required, since a test conducted at a constant 8.0 g_{rms} level (Step 1) would take thousands of hours to fail the same number of components as a step stress test. This is because some locations on a circuit assembly experience very low stresses and severe vibration is required in order to fail components at these locations. The shape of the PSD (Power Spectral Density) curve for each step stress level was designed so that all of the major resonances of the test vehicles would be excited by the random vibration input. The PSD curves presented in MIL-STD-810F were used as guides for the creation of this step stress test but were not directly duplicated.

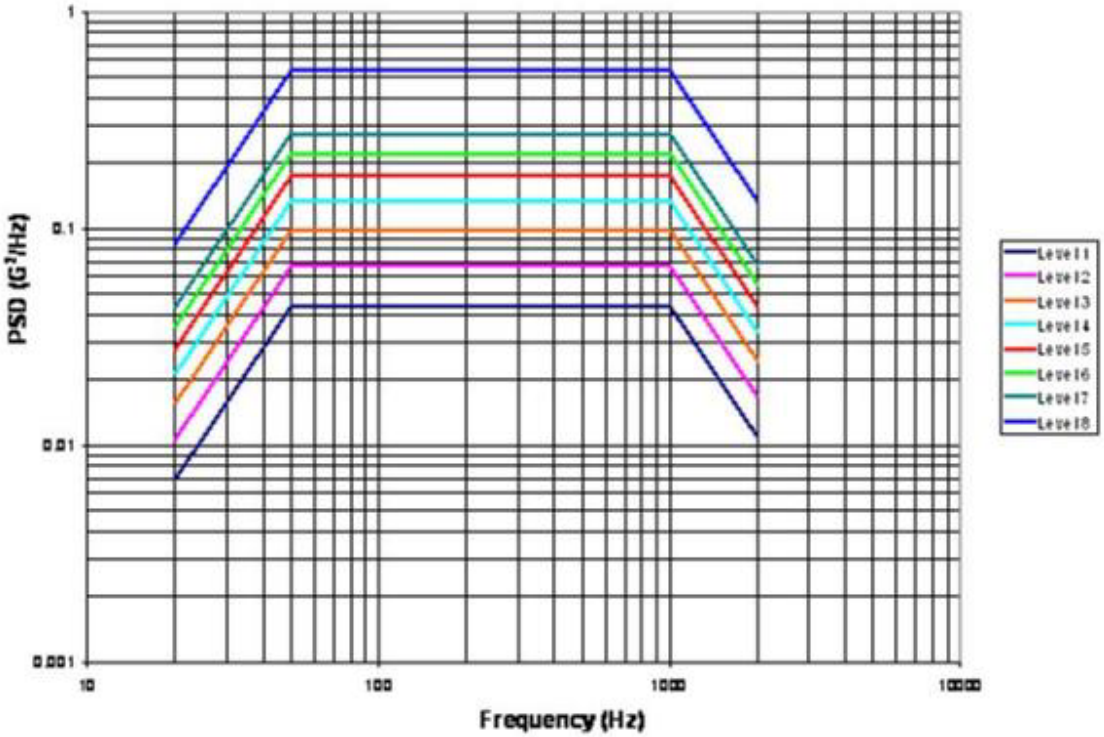

Figure 12. Vibration spectrum with increasing g levels to enforce sufficient failures during short period testing.

Twenty-seven test vehicles consisted of 5 SnPb "Manufactured" test vehicles; 6 Pb-free "Manufactured" test vehicles assembled with SAC305 paste; 5 Pb-free "Manufactured" test vehicles assembled with SN100C paste; 6 SnPb "Rework" test vehicles; and 5 Pb-free "Rework" test vehicles. Most of the test vehicles had an immersion silver PWB finish, except for one SAC305 "Manufactured" test vehicle (Test Vehicle 96) with ENIG PWB finish and one SnPb "Rework" test vehicle (Test Vehicle 157) with ENIG PWB finish.

Table 5 shows the percent of each component type that failed on both the "Manufactured" and the "Rework" test vehicles at the end of the test. Notice that the QFN-20's were resistant to failure due to vibration.

Table 5. Percentage of packages failed (includes mixed solders) [courtesy NASA-DoD Consortium].

	% of Components Failed During Vibration Testing				
	"Manufactured" Test Vehicles			"Rework" Test Vehicles	
	SnPb Paste	SAC305 Paste	SN100C Paste	SnPb Paste	Pb-Free Paste
Component					
BGA-225	84	98	100	100	100
CLCC-20	32	43	90	35	68
CSP-100	62	73	70	62	80
PDIP-20	98	92	100	88	96
QFN-20	0	21	20	8	10
TQFP-144	60	63	64	70	70
TSOP-50	62	73	86	77	80

The overall results of the vibration testing are summarized in Table 6. If a solder alloy/component finish combination performed as well or better than the SnPb control, it was assigned the number “1” and the color “green”. Solders that performed worse than the SnPb control were assigned a “2” and the color “yellow”. Solders that performed much worse than the SnPb control were assigned a “3” and the color “red”.

The rankings in Table 6 are somewhat subjective due to the scatter in the data for some component types. The TSOP data was difficult to interpret since the orientation of the TSOP on the test vehicle appeared to influence how the solder/component finish combinations performed relative to the Sn37Pb/SnPb controls. Weibull plots were not used since the test conditions were changed during the test (i.e., the PSD was increased every 60 minutes), which renders the Weibull parameters meaningless.

Table 6. Comparison of tin-lead and Pb-free solder joint reliability based on repeated and increasing vibration levels [courtesy NASA-DoD Consortium].

	Relative Ranking (Solder Alloy / Component Finish)											
BGA-225	Sn37Pb/ Sn37Pb	SAC305/ SAC405	Sn37Pb/ SAC405	SAC305/ Sn37Pb	Rwk Flux Only/ Sn37Pb	Rwk Flux Only/ SAC405	Rwk Sn37Pb/SAC405 (SnPb Profile)	Rwk Sn37Pb/SAC405 (Pb-Free Profile)	SN100C/ SAC405			
	1	3	3	3	3	3	3	3	3			
CLCC-20	Sn37Pb/ Sn37Pb	SAC305/ SAC305	Sn37Pb/ SAC305	SAC305/ Sn37Pb	SN100C/ SAC305							
	1	3	2	3	3							
CSP-100	Sn37Pb/ Sn37Pb	SAC305/ SAC105	Sn37Pb/ SAC105	SAC305/ Sn37Pb	Rwk Flux Only/ Sn37Pb	Rwk Flux Only/ SAC105	Rwk Sn37Pb/SAC105 (SnPb Profile)	Rwk Sn37Pb/SAC105 (Pb-Free Profile)	SN100C/ SAC105			
	1	1	1	2	1	2	1	3	1			
PDIP-20	Sn37Pb/ SnPb	SN100C/ Sn	Sn37Pb/ NiPdAu	Rwk Sn37Pb/ Sn	Rwk Sn100C/ Sn	SN100C/ NiPdAu						
	1	3	2	3	3	3						
QFN-20	Sn37Pb/ Sn37Pb	SAC305/ Sn	Sn37Pb/ Sn	SAC305/ Sn37Pb	SN100C/ Sn							
	1	2	1	1	2							
TQFP-144	Sn37Pb/ Sn	SAC305/ Sn	Sn37Pb/ NiPdAu	SAC305/ NiPdAu	Sn37Pb/ Sn37Pb Dip	SAC305/ SAC305 Dip	SN100C/ Sn					
	1	1	1	2	1	2	1					
TSOP-50	Sn37Pb/ SnPb	Sn37Pb/ Sn	Sn37Pb/ SnBi	SAC305/ Sn	SAC305/ SnBi	SAC305/ SnPb	Rwk Sn37Pb/ SnPb	Rwk Sn37Pb/Sn (SnPb Profile)	Rwk Sn37Pb/Sn (Pb-free Profile)	Rwk SAC305/ SnBi	SN100C/ Sn	SN100C/ SnBi
	1	2*	2*	2*	2*	2	2	2*	2*	2	2	2

*Performance relative to Sn37Pb control may depend on orientation of the TSOP

1 = as good as or better than Sn37Pb control

2 = worse than Sn37Pb control

3 = much worse than Sn37Pb control

5. Conclusions

NASA has stringent reliability requirements; some coincide with other high-reliability applications and others are unique for the space environment. For example, mechanical methods such as shock and vibration at the package, assembly, and system levels have been an integral part of evaluation for use of microelectronics in high-reliability applications. Indeed, NASA has numerous specifications that address approaches on evaluating resistance to mechanical loading at various levels for conventional packages, such as leaded components. In addition, workmanship requirements to meet harsher mechanical environments are in place. This is not, however, applicable for advanced electronics packages. The requirements for advanced electronics packages, mostly developed and used by commercial industry, need to be reviewed, and their applicability and use for high reliability needs to be identified. This BOK survey identified numerous specifications and investigations on mechanical performance of advanced electronic packaging that could be explored further for high-reliability applications. Key findings are as follows.

- Most advanced electronic packages come in plastic versions rather than the ceramic that is typically considered for high-reliability applications.
- Package-on-package has become a popular choice for commercial industry.
- Numerous specifications are developed by industry (IPC and JEDEC) to address mechanical reliability issues associated with use of advanced electronic packages, especially for mobile applications. These specifications were summarized and presented.
- Industry further enhanced use of mechanical evaluation due to poorer mechanical performance of most Pb-free solder alloy interconnections. Whenever data were available, behavior of both tin-lead and Pb-solder interconnections were presented for comparison.
- The most recent plot of allowable strains for PCB under monotonic bend test based on IPC/JEDEC 9702 was presented. Allowable microstrains decrease for higher strain loading applications.
- An acoustic emission monitoring test method procedure that detects earlier signs of pad cratering is being developed by IPC as a guideline.
- Correlation between the number of cycles to failure during bend testing and the change in solder joint energy is generally non-linear.
- Most area array packages have low resistance to repeated drops.
- Underfill, underfilm underfill, and edge-bond have been shown to improve resistance to mechanical drop tests by a number of authors.
- Vibration behavior of package assemblies are less studied and understood. Investigators agree that data on the fatigue life given by the traditional superposition approach (Minor's Rule) are not valid and generally overpredict life projections. For example, it was shown that the sequence of thermal cycles followed by vibration was a harsher sequence than vibration followed by thermal cycle.
- At higher temperature, vibration durability is much shorter than at RT due to changes in solder fatigue properties and the strain-rate effect of model frequency.

- Failure under vibration for package assemblies are different. QFPs fails by copper lead deformation/cracking, TSOPs fails at solder joints, and PBGAs fails by solder ball cracking at copper traces.
- NASA-DoD test data generated regarding mechanical shock and vibration performance of package assemblies with Pb-free and tin lead solder alloys were compared. In general, tin-lead performed better than Pb-free solder assemblies.

Understanding of the key design guidelines from the literature survey, test data, and failure mechanisms, considered in conjunction with complementary future test data, is critical to developing an approach to minimize failures for NASA's severe mechanical loading and fatigue requirements. Such knowledge base allow in preparation for low-risk insertion of these advanced electronic packages.

6. Acronyms and Abbreviations

BGA	ball grid array
CBGA	ceramic ball grid array
CCGA	ceramic column grid array
CGA	column grid array
COTS	commercial-off-the-shelf
CQFP	ceramic quad flat pack
CSP	chip scale (size) package
CTE	coefficient of thermal expansion
Cu	copper
DOE	design of experiment
EDX/EDS	energy dispersive x-ray
FPGA	field programmable gate array
FCBGA	flip-chip ball grid array
HASL	hot-air solder leveling
HDI	high density interconnect
I/O	input/output
JPL	Jet Propulsion Laboratory
LGA	land grid array
MIP	mandatory inspection point
NASA	National Aeronautics and Space Administration
NEPP	NASA Electronic Parts and Packaging
NSMD	non solder mask defined
PBGA	plastic ball grid array
PCB	printed circuit board
PWB	printed wiring board
QA	quality assurance
QFP	quad flat pack
RMA	rosin mildly activated
SEM	scanning electron microscopy
SMC	surface mount components
SMD	solder mask defined
SMT	surface mount
Tg	glass transition temperature
TV	test vehicle

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