National Aeronautics and Space Administration

Reliability of CGA/LGA/HDI Package Board/Assembly

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Reliability of CGA/LGA/HDI Package Board/Assembly (Revision A)

NASA Electronic Parts and Packaging (NEPP) Program
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OBJECTIVES AND PRODUCTS

Commercial-off-the-shelf column grid array (COTS CGA) packaging technologies in high-reliability versions are now being considered for use in a number of National Aeronautics and Space Administration (NASA) electronic systems. Understanding the process and quality assurance (QA) indicators for reliability are important for low-risk insertion of these advanced electronic packages.

The previous report on this subject presented test data and assembly information for CGA packages with 1752 and 1272 inputs/outputs (I/Os) and 1-mm pitch. Also presented were test results for a number of land grid arrays (LGAs) with 1517 I/Os that were converted to CGAs and subjected to column pull testing—first, as attached and, subsequently, at intervals during isothermal aging at 125°C. These CGAs were also successfully assembled onto PCBs for subsequent environmental reliability testing.

This follow-up report presents reliability test results conducted by thermal cycling of five CGA assemblies evaluated under two extreme cycle profiles, representative of use for high-reliability applications. The thermal cycles ranged from a low temperature of –55°C to maximum temperatures of either 100°C or 125°C with slow ramp-up rate (3°C/min) and dwell times of about 15 minutes at the two extremes. Optical photomicrographs that illustrate key inspection findings of up to 200 thermal cycles are presented. Other information presented include an evaluation of the integrity of capacitors on CGA substrate after thermal cycling as well as process evaluation for direct assembly of an LGA onto PCB. The qualification guidelines, which are based on the test results for CGA/LGA/HDI packages and board assemblies, will facilitate NASA projects' use of very dense and newly available FPGA area array packages with known reliably and mitigation risks, allowing greater processing power in a smaller board footprint and lower system weight.

Key Words: CGA, CCGA, LGA, BME Capacitor, solder joint reliability, thermal cycle, column grid array, 2nd level reliability

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1.0 EXECUTIVE SUMMARY

The overall objectives and approaches of the reliability evaluation of CGA/LGA/HDI package/board/assembly are summarized in Figure 1. Topics marked with smiley faces are investigated and either presented previously [1] or will be covered in this or follow-on reports when sufficient data become available. The overall goal is to develop qualification guidelines for advanced high input/output (I/O) column/land grid array (CGA/LGA) assembled onto both conventional and high density interconnect (HDI) printed circuit/wiring boards (PCB/PWB). This report will briefly address results for package evaluation and assembly optimization as well as detail results of thermal cycle testing and failure analyses.

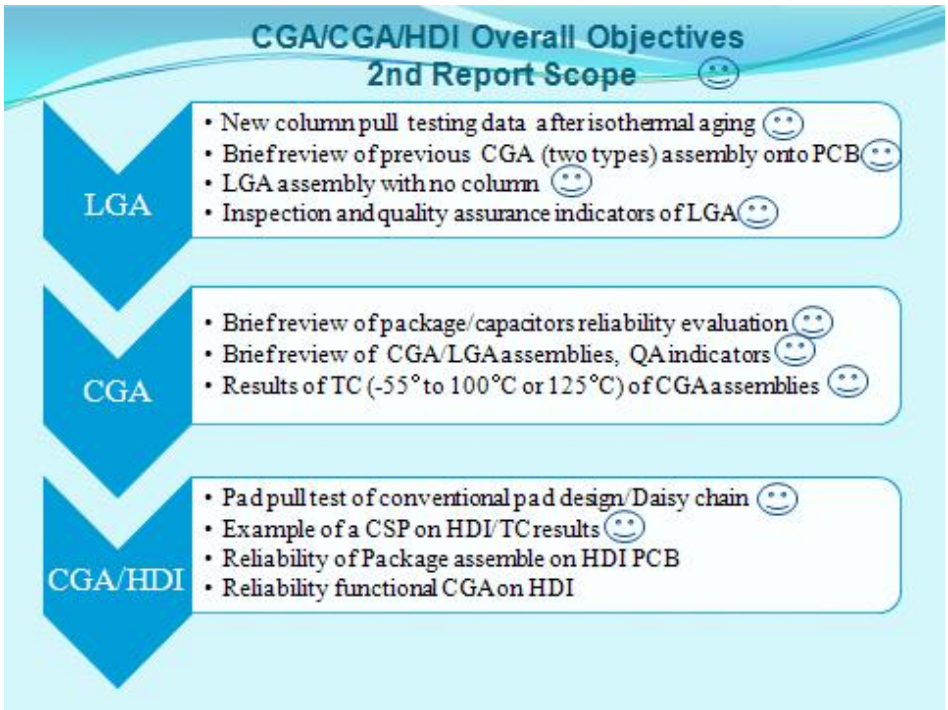

Figure 1. Test matrix for CGA/CCGA/HDI package/board/assembly program with identification of the key areas of investigation.

Two CGA packages with 1752 and 1272 I/Os and two column styles were evaluated, one with a pure solder column and the other with a copper-wrapped solder column. The scope of evaluation also included a ceramic array package with 1517 I/Os that came as land grid array (LGA) with no column attachment. LGAs were converted into CGA by performing two styles of column attachment at two facilities. One style had copper wrapped onto a solder column with a diameter slightly lower than standard value; the other style had a microspring coil with no solder column, but a standard diameter. Figure 2 shows photomicrographs of four CGA packages and their column configurations. Integrity of the Cu-wrapped column was established with isothermal aging at 125°C for up to 1000 hours of aging.

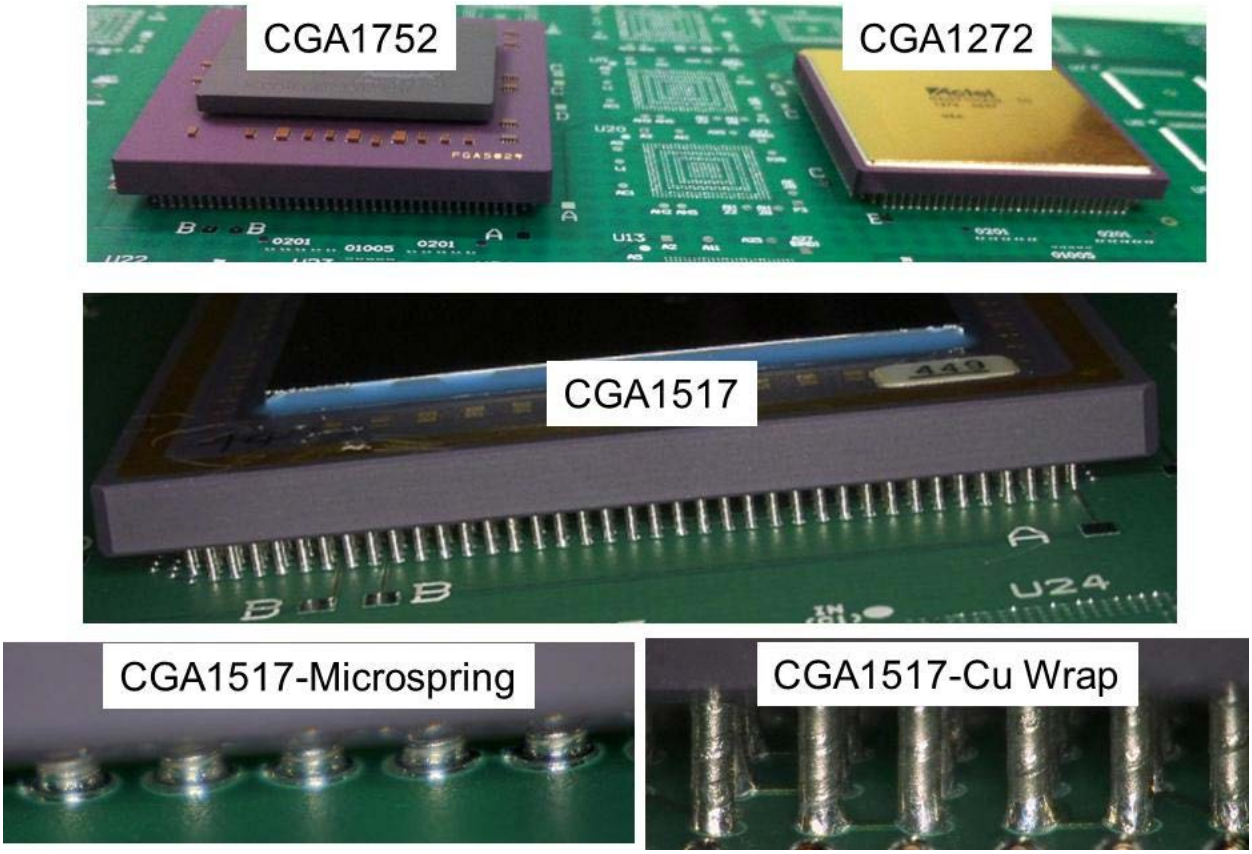

Figure 2. Four CGA types: CGA1752 with pure solder column (top-left) and CGA1272 with copper-wrapped solder column (top-right), CGA1517 with microspring column (bottom-right), CGA1517 with Cu Wrapped column (bottom-left).

Previously, visual, SEM, and thermal cycle (–55° to 130°C) evaluations were performed on the CGA1752 package alone to determine the integrity of column attachment and the chip capacitors on the package substrate. In addition, multilayer capacitors, on-package assembly after thermal cycling, were evaluated for microstructural integrity by X-sectioning and material construction by elemental analysis using scanning electron microscopy (SEM) analysis tools.

Four CGA packages (CGA1272, CGA1509, CGA1517, CGA1752) with three column types (pure solder, copper-wrapped, and microspring columns) were assembled onto conventional printed circuit boards using three types of tin-lead solder paste alloys. The inspection results of the peripheral columns after assembly revealed that the quality of solder joints to be acceptable (see Figure 3). X-ray photomicrographs, showing the quality of solder joint assemblies and applicable workmanship defects, revealed no shorts or significant solder balling. Four types CGA assemblies were subjected to thermal cycling for evaluation of solder joints as well as capacitor and internal flip-chip die on package. Assemblies were subjected to two extreme profiles representative of use for high reliability applications. The thermal cycles ranged from a low temperature of –55°C to maximum temperatures of either 100°C or 125°C with slow ramp-up rate of 3°C/min) and dwell times of about 15 minutes at the two extremes. Optical, SEM, and X-ray inspection of assemblies were performed prior to thermal cycling to evaluate solder joint quality and workmanship defects and subsequent inspections during thermal cycling exposures established solder damage and progress with cycling. Photomicrographs illustrate key inspection findings after up to 200 thermal cycles are presented. Figure 3 provides examples of such

photomicrographs taken at 200 thermal cycles (–55°/125°C). An LGA package was also directly assembled onto PCB to determine generic processing issues.

In summary, it was demonstrated that LGA could be successfully converted into CGA packages using either of the two column styles. Furthermore, these types of CGA packages could be successfully assembled onto conventional PCBs if the PCB pad design and other processing parameters were appropriately optimized for the column styles and package sizes. A number of extremely large/thick CGA packages with 1272, 1509, 1517, and 1752 I/Os were successfully assembled onto PCBs. One LGA package with no-columns also assembled onto PCB with some success. Reliability is a key issue that was addressed for chip capacitors on packages for the non-hermetic CGA1752 package. Thermal cycle behavior of 2nd-level reliability of four CGA packages with four styles of columns/sizes were evaluated for solder damage progress with thermal cycling (–55°/100°C or –55°/125°C) established by optical, X-ray, and SEM inspection evaluation technique. Representative optical photomicrographs for all CGA assemblies after up to 200 thermal cycles presented.

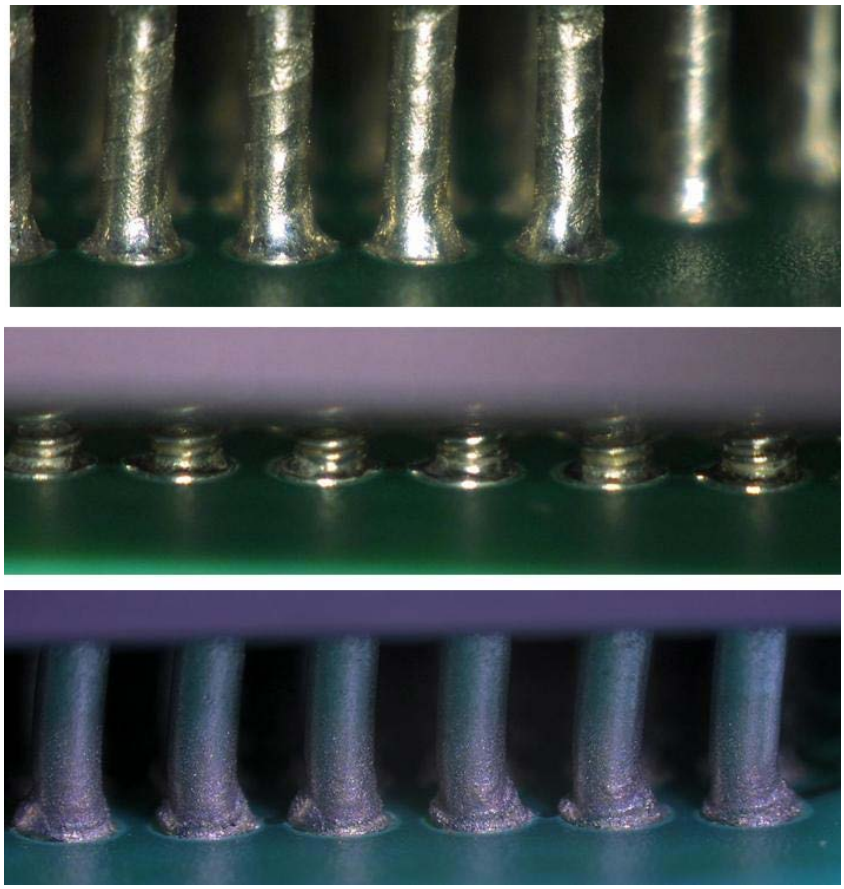

Figure 3. Representative photomicrographs of three solder columns solder joint quality after 200 thermal cycles (–55°/125°C) for CGA package assemblies.

2.0 GAS AND EVALUATION APPROACHES

2.1 Column Grid Array Packaging Technology Trend

For high reliability applications, lower I/O CGAs with a 1.27-mm pitch (the distance between adjacent column centers) are replacing surface-mount leaded packages, such as ceramic quad flat packs (CQFPs). There are no comparable ceramic leaded packages for higher I/O CGAs. The advanced CGA packages, those with more than 1000 I/Os, generally come in 1-mm pitch and use flip-chip die rather than wire bond internal to the package. Replacement to CGA is especially appropriate for packages with higher than 300 I/O counts where CQFP pitches become much finer (0.3–0.4 mm), making them extremely difficult to handle and assemble. In addition to size reduction, CGAs also provide improved electrical and thermal performance and are the package choice for field programmable gate arrays (FPGAs). However; their solder columns are prone to damage, it is challenging to assemble them onto PCB, and it is almost impossible to rework defective solder joints.

Rework, re-attachment of columns, and reassembly prior to final assembly may be required to address solder defects due to processing or column damage due to shipping and mishandling. The CGA packages are in the form of LGA during initial die attachment and underfilling; later columns are attached under another processing step. This report will address several pertinent issues: the integrity of LGAs after column attachment process; the integrity of CGA packages with chip capacitors; and the solder joint reliability of both LGAs and CGAs after they are assembled onto PCBs.

CGA packages are preferred to CBGA (see Figure 4) since they show better thermal solder joint reliability than their CBGA counterparts. For most high reliability applications, CGAs show acceptable solder joint reliability for larger packages and higher than 300 I/Os (when resistance to thermal cycling is significantly reduced for CBGAs with increasing package size and I/Os). To limit the growth of package size, most ceramic packages with more than about 1,000 I/Os come in the CGA style with 1-mm pitch or lower.

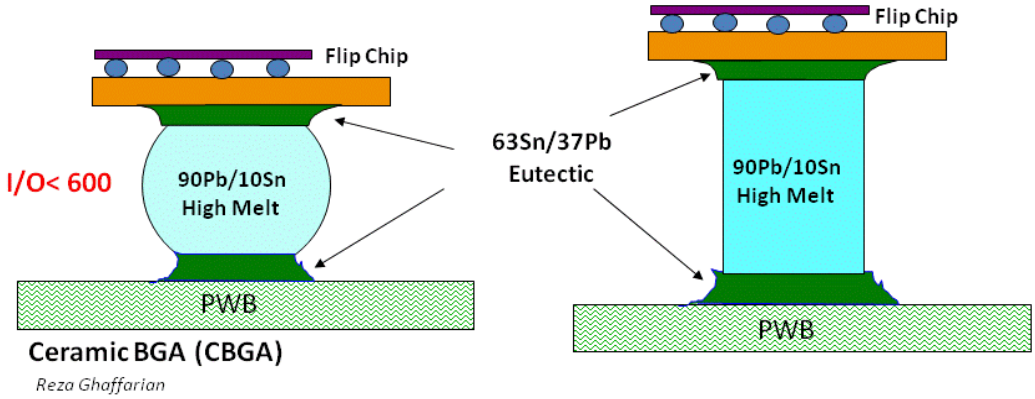

Figure 4. Examples of ceramic column grid array (CCGA or CGA) and ceramic ball grid array (CBGA) package configurations.

The key drawback of CGAs remains the same: individual column re-workability is impossible and inspection capability for interconnection integrity is poor (e.g., cannot detect cracks or cold solder). Implementation of process controls is critical in achieving quality solder joints, which consequently achieves optimum assembly reliability. Visual inspection of peripheral columns, when they are not blocked, can be performed by optical microscopy to ensure solder quality as another process indicator. Although progress has been made in improving the resolution of X-ray for better inspection, the issue of inspection for specific defects, such as cold solder joints and microcracks, remains unresolved.

Even though CGAs are commercial-off-the-shelf (COTS) packages, their high reliability versions go through a much more stringent screening, which adds significant cost and longer delivery times. The issues with CGA COTS packages are essentially the same as other COTS issues and include package die source and lot-to-lot materials variations, availability of packages with radiation-hard die, outgassing for materials including underfill, etc. A number of these issues is addressed for high reliability versions. Assembly, inspection, and lack of individual solder reworkability issues are additional key aspects of such implementation. Assembly reliability behaviors of such area array packages, including CGAs, are addressed in a number of previous investigations [2]–[7].

2.2 Purpose of This 2nd Interim Report

This 2nd interim report presents test data for CGA packages with 1752 and 1272 I/Os and 1-mm pitch. It summarizes the previous results of visual, SEM, and thermal cycle evaluations performed on the CGA1752 packages to determine the integrity of the chip capacitors on package followed by test result of failure analysis of them after thermal cycling. The CGA packages were successfully assembled onto conventional printed circuit boards using standard tin-lead solder paste alloys. Prior to thermal cycling, inspection was performed to determine quality of solder joints for solder paste types with different solder particulate sizes. Results are also presented for inspections performed on two packages with different dimensions and column types. X-ray photomicrographs show the quality of solder joint assembly and workmanship defects.

Evaluation also included a ceramic array package with 1517 I/Os that was originally an LGA. A number of LGAs were transformed into CGA by performing column attachment using two different column styles. The integrity of column attachment for these was established by subjecting them to pull testing; first, as attached and, subsequently, at intervals during isothermal aging at 125°C. The pull test results are shown.

3.0 EXPERIMENTAL APPROACHES FOR CGA PACKAGES

3.1 CCGA Package Types

The evaluations covered in this report deal with several aspects of advanced area array packaging and high density printed circuit boards. One was to characterize the reliability of CGA packages with 1752 and 1272 I/Os and 1-mm pitch, assembled onto conventional PCBs. Figure 5 shows photomicrographs of the two CGAs and their sizes. These daisy-chain CGA packages were built by two different manufacturers and had two different column styles. Since CGA daisy-chain packages are typically 50 to 300 times more expensive than PBGA daisy-chain versions, only a very limited number were used. This section reviews test results for packages and assembly optimization.

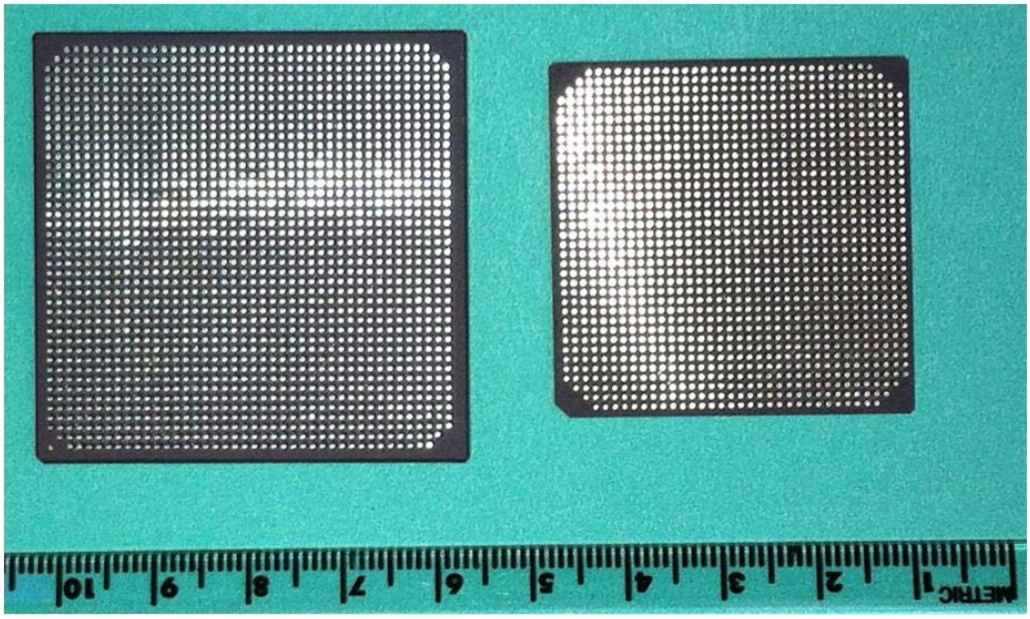

Figure 5. The two column grid array (CGA) packages; 1752 I/Os (left) and 1272 I/Os (right). Note that in both cases corner columns are removed by the manufacturer.

3.2 CGA Package Receiving, Inspection, and Evaluation

The two CGA package types were inspected by microscope to detect any workmanship defect anomalies, such as bent columns, and to verify the quality and uniformity of solder joints for column attachments. (see Figure 6, for representative photomicrographs of the two packages.) The 1752 package has pure tin-lead solid solder with high lead concentration (90Pb/10Sn); the 1272 CGA package has slightly lower lead solder content (80Pb/20Sn), but solder columns are wrapped with copper helical spring. Copper-wrapped columns are also tin-lead coated and therefore do not have the appearance of copper except for the exposed flat area on top.

The CGA1272 is hermetically sealed with no additional chip capacitor parts. The CGA1752 is non-hermetic, has an additional chip capacitor on top of the ceramic substrate, and is exposed. Figure 6 shows a generic construction of this package provided by the manufacturer along with a photo of the package from the top. Inspection of chip capacitor solder joints for a package received in December 2010 revealed a number of unacceptable solder joints, based on NASA workmanship standards. For this reason, the solder joints for these chip capacitors were further characterized by SEM and subjected to a limited number of thermal shock cycles. The results of inspection and environmental evaluation are discussed in the following sections.

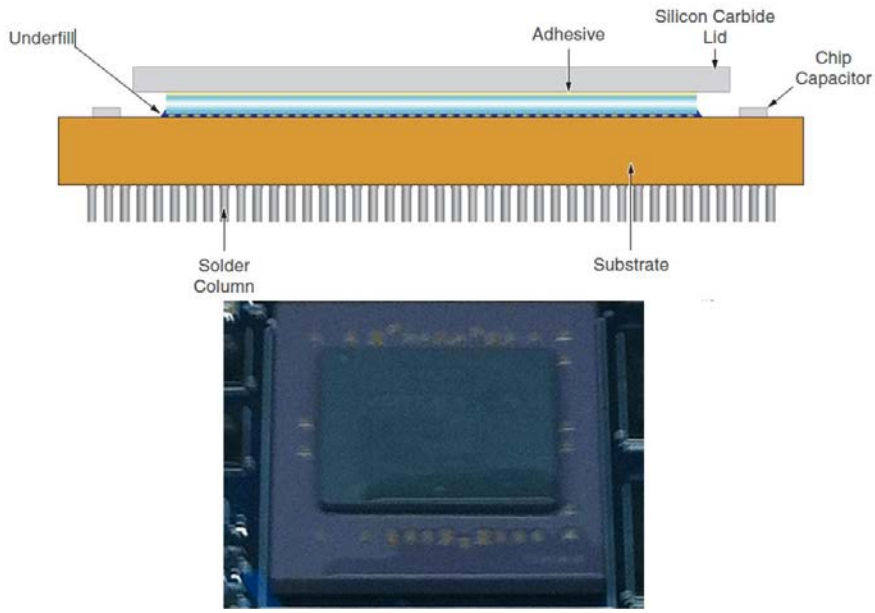

Figure 6. Construction of CGA 1752 I/O package (top) and photo of package showing the exposed chip capacitors.

3.2.1 CGA Package Characterization by X-ray

A real-time 2D X-ray system was used to determine the integrity of column solder joint attachment, among other features of these packages. Figure 7 shows representative X-ray photomicrographs of CGA1752 and CGA1272.

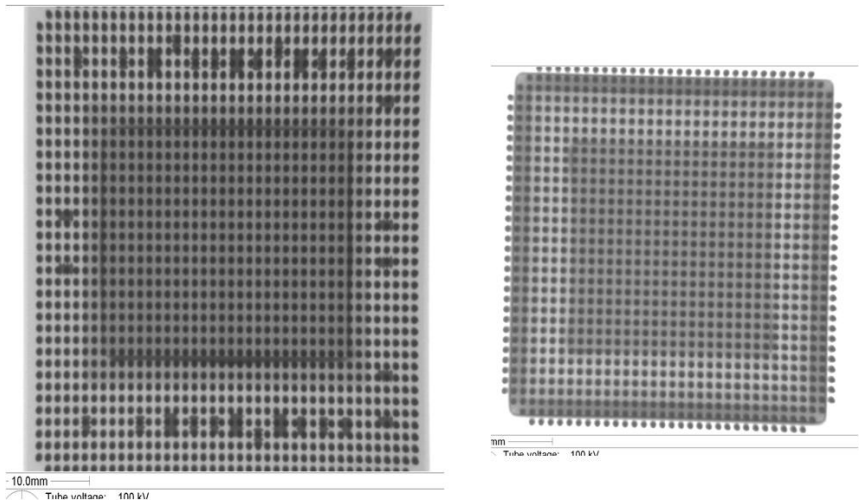

Figure 7. X-ray photomicrographs of CGA 1752 I/Os (left) and CGA 1272 I/Os (right); the darker areas are where chip capacitors are located.

3.2.2 Chip Capacitor Characterization

The first set of daisy-chain package samples was received late in December of 2010. The second set of daisy-chain package samples was received late in May 2011. For the second set, inspection revealed better workmanship of the solder joints for the chip capacitors surface mounted on CGA substrate. Chip capacitor solder joints are formed into the side metallization rather than conventional two-end solder

joints. Figure 8 and 9 show optical photomicrographs of representative solder joints, acceptable/unacceptable quality, based on NASA workmanship requirements.

There are six (6) 0805 and twenty-five (25) 0603 capacitors, making a total of 248 solder joints. Note that these are daisy-chain packages and may not be representative of a functional package. Functional packages should be inspected for such workmanship anomalies before committing to an expensive assembly process and extremely difficult rework process. Inspection plan should be implemented at receiving to assure adequate quality of solder joints if chip capacitors are not hidden and could be inspection. However, recent application note indicates that heat sink sizes are increased to cover the package substrate; therefore, such implementation will hinder visual inspection of chip capacitors for solder joint quality.

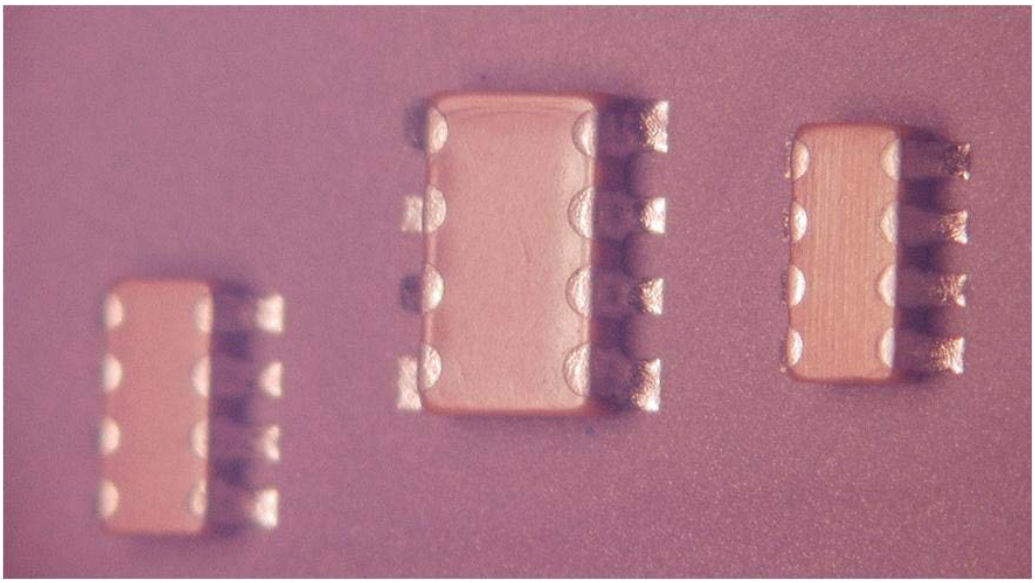

Figure 8. Chip capacitors showing better solder joint quality in the May 2011 set.

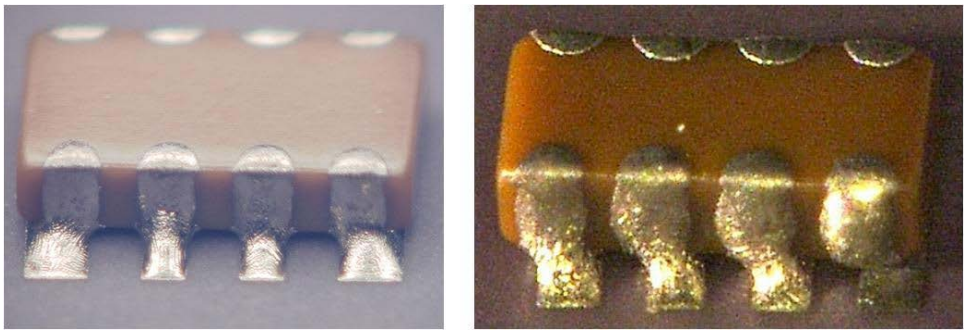

Figure 9. Chip capacitors showing inconsistency in solder joint quality; the far right solder is clearly unacceptable.

Further characterizations were performed using SEM to better define microstructure. Figure 10 shows a representative example of solder joint quality at a higher magnification. In addition, elemental analysis was performed using dispersive X-ray spectroscopy (EDX/EDS) to obtain semi-quantitative elemental results for the solder joints. The results showed that indeed they are high lead tin-lead solder (90Pb/10Sn), similar to the column solder alloy. The melting point of these solder alloys is higher than the tin-lead commonly used to attach columns onto PCB. High lead solders generally show a lack of shininess and

poor flow. This is due to their alloy pasty regime during solidification when they are compared to eutectic tin-lead solder, with no pasty regime during melting.

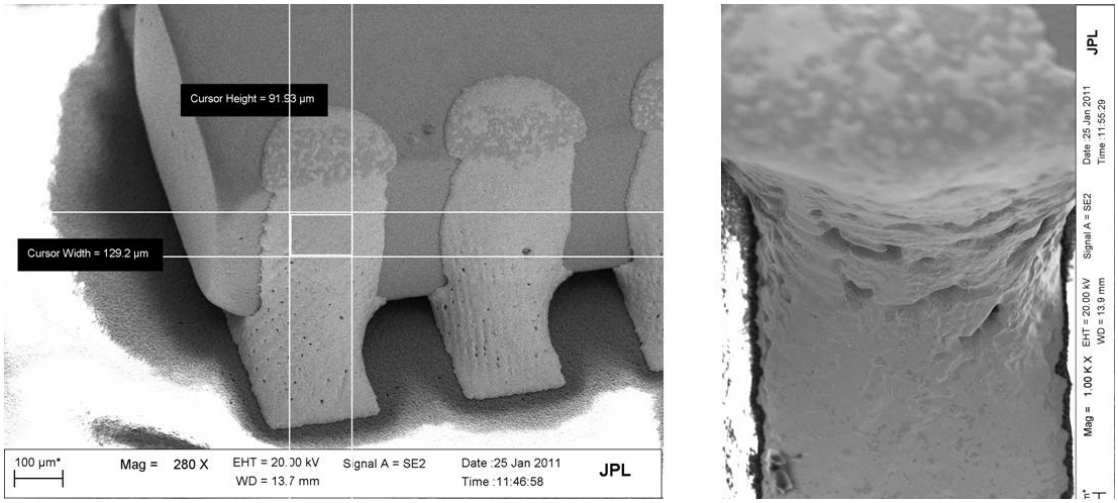

Figure 10. SEM photomicrographs showing the nature of solder joints at much higher magnification.

3.2.3 Chip Capacitor Characterization after Thermal Shock Cycles of Unattached CGA

CGA1752 and CGA1272 packages with different column styles were subjected to thermal shock cycles to specifically establish resistance of chip capacitor solder joints (for CGA1752) and to inspect the integrity of solder column attachments. To establish behavior of high lead solder joints under thermal cycling and subsequent reflow during assembly, the thoroughly inspected package was subjected to thermal shock cycles. This was accomplished by using two chamber cells and cycling between –55° to 130°C, with 10 minutes dwell times at the two extreme temperatures. Samples were removed after 50 cycle intervals and inspected for signs of damage and degradation due to thermal shock cycles.

Figure 11 shows representative solder joints after 200 thermal shock cycles. No evidence of significant damage or crack initiation was observed. Resistance of solder joint to thermal shock is attributed to good coefficient of thermal expansion (CTE) match of ceramic chip capacitors to ceramic CGA substrate. The higher melting temperature of high lead (tin-lead alloy) solder also contributed to its high resistance to thermal shock cycle.

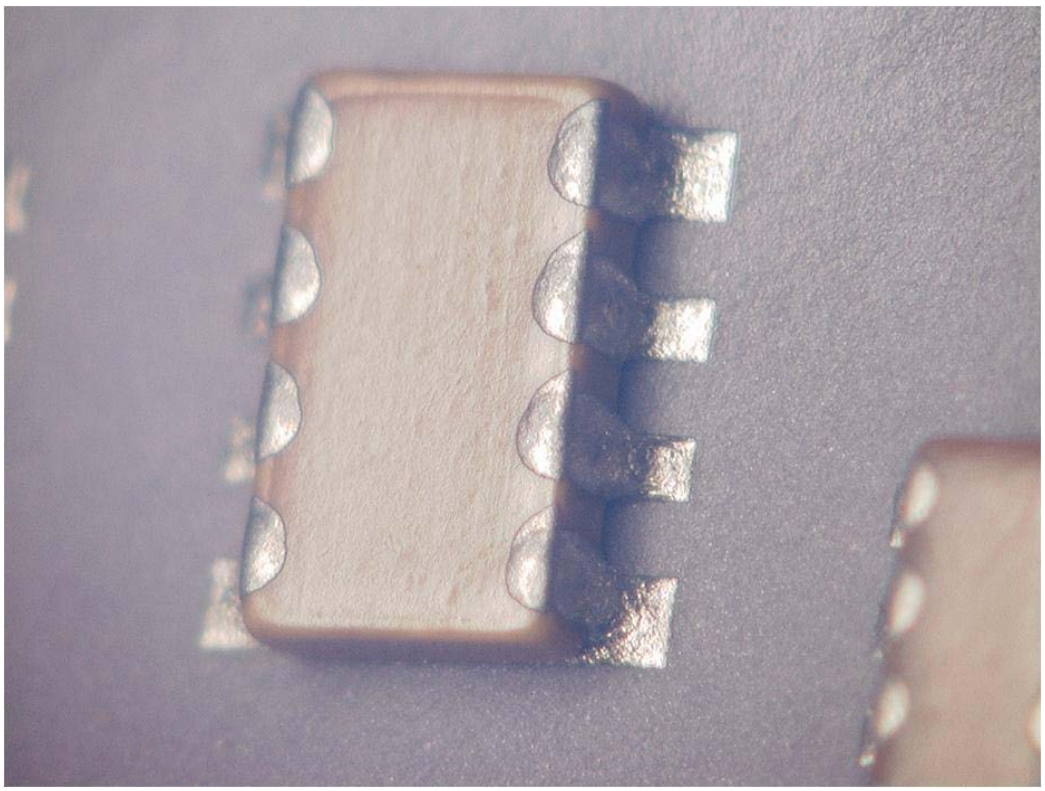

Figure 11. Chip-capacitor solder joint quality after 200 thermal shocks (–55° to 130°C) showing no signs of cracks.

3.2.4 Chip Capacitor Failure Analysis after Thermal Shock Cycles of CGA Assembly

The unassembled CGA1752 package after thermal exposure was also assembled onto PCB along with the other unexposed packages using eutectic tin-lead solder joint. This and other package assemblies were subjected to thermal cycling using two profiles. The chip capacitors with pre-cycling condition were inspected while on the subtracted using optical and SEM. Damage condition of a representative chip capacitor after CGA assembly thermal cycling prior to removal and locations of their removal for subsequent evaluation is shown in Figure 12. The history of thermal cycle condition of these chip capacitors is as follows:

- Package subjected to thermal shock (–55/130°C);
- Reflow for Assembly (218°C); and
- Additional TCs of CGA package assembly on board.

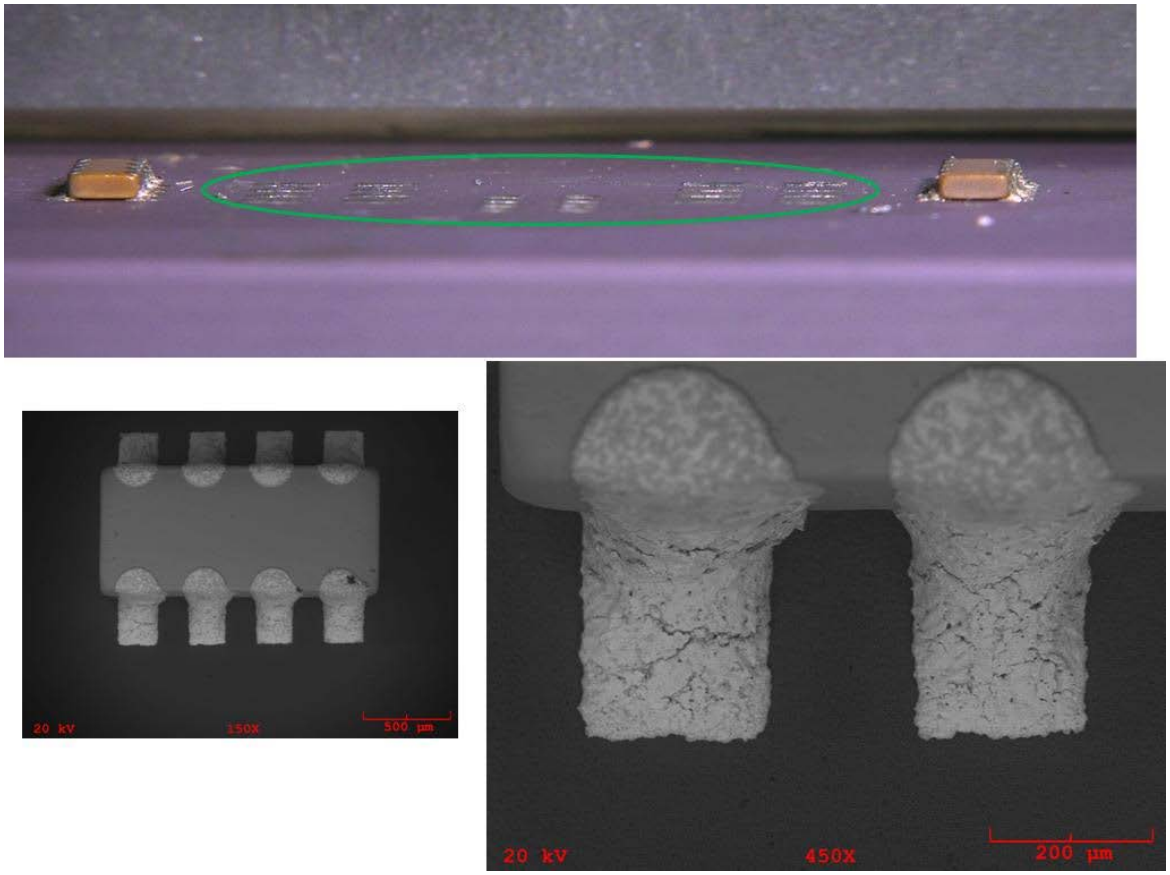

Figure 12. SEM photomicrographs of chip-capacitor solder joint quality after an assembly reflow cycle (RT-218°C) and thermal cycles (–55° to 125°C) and removal locations.

SEM features of a removed capacitor shows signs of large number of microcracks and gross microstructural features. Cross-sections (see Figure 13) of chip capacitor showed no internal failures even though one showed cracking through section possibly due to methods of removal of chip from substrate by mechanical means. Option of de-soldering of solders for capacitor removal was not considered since it is thought that such thermal shock could cause formation of internal microcracks or failure, which would have been difficult to distinguish from the induced environmental thermal shock or thermal cycle testing.

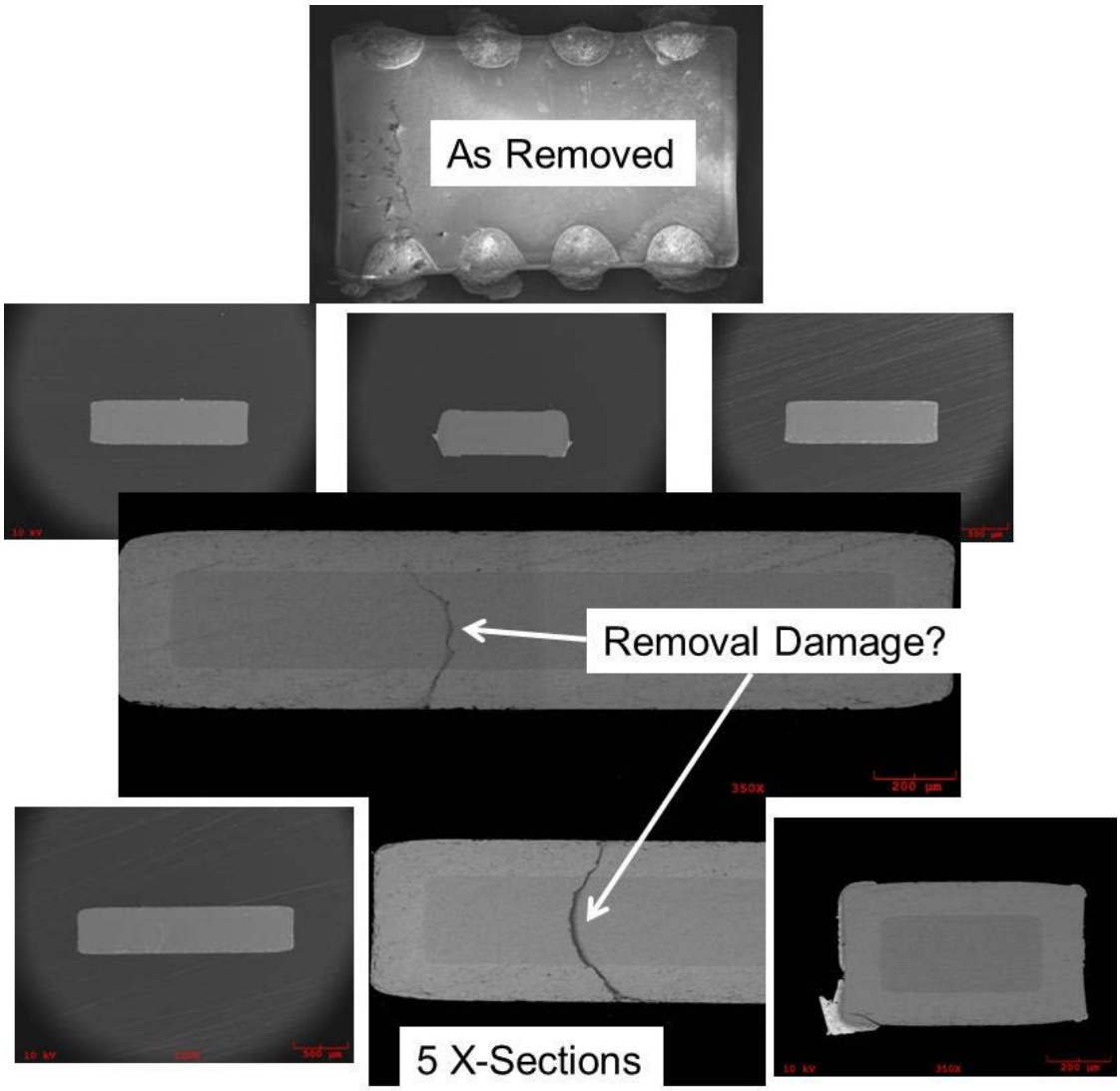

Figure 13. SEM photomicrographs of five chip-capacitor before (top) and after cross-sectioning (five) subjected an assembly reflow cycle (RT-218°C) and thermal cycles (–55° to 125°C).

SEM EDS elemental analysis and mapping for capacitor's interlayer chemical distribution are shown in Figure 14. Capacitor was identified as $BaTiO_3$ dielectric with Ni electrodes. $BaTiO_3$ capacitor is part of category of capacitors that are known as base metal electrode (BME) which were developed to meet the needs of microelectronic industry for reduction in cost, demand in increasing capacitance, and move towards shrinking in size.

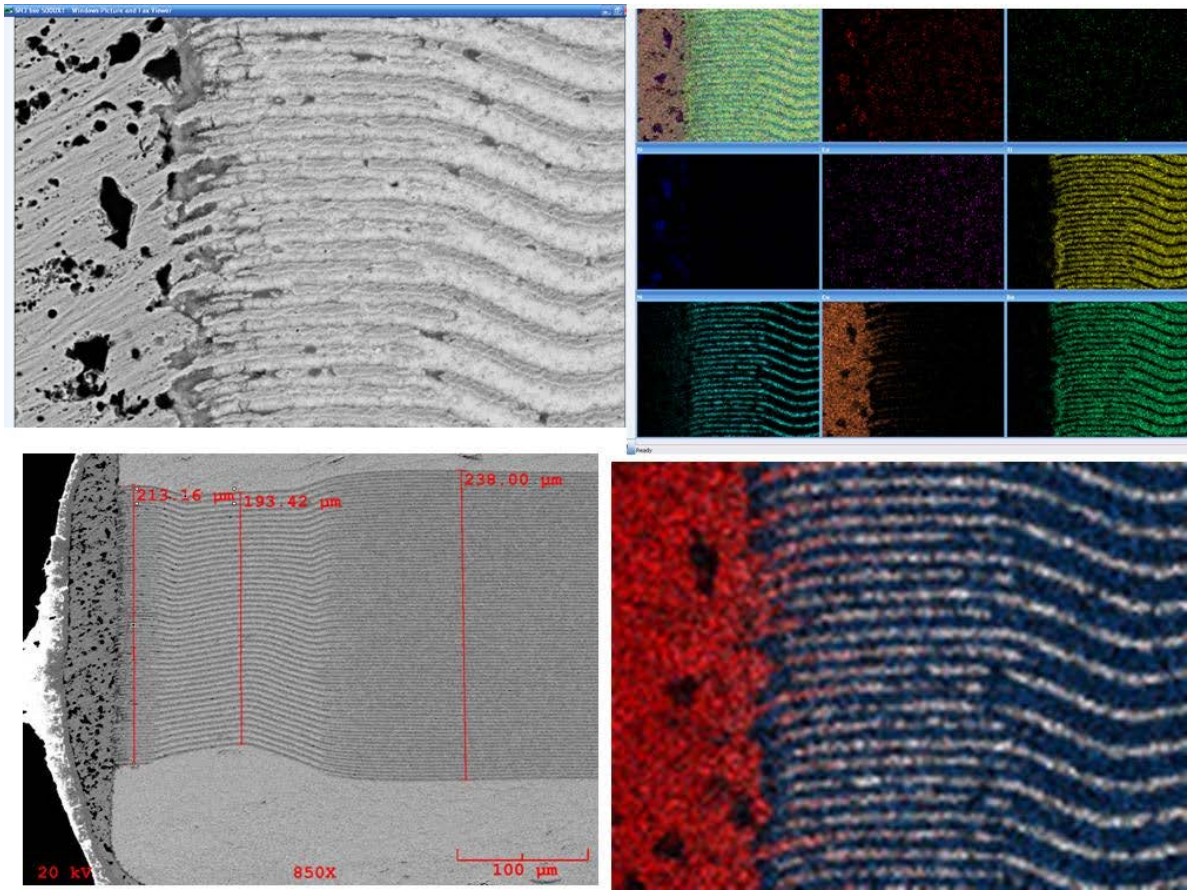

Figure 14. SEM photomicrographs of chip-capacitor showing EDS elemental analysis of layers and end cap as well as dimensions of those layers

Multilayer ceramic chip capacitors are fabricated as alternative layers of ceramic dielectric and metal electrodes. Initially, these electrodes were made of precious metals such as silver, platinum, palladium, and gold. For high reliability applications, precision metal electrodes (PME), MLCC version, have been widely used and their capacitance behavior and reliability under environmental conditions are well established for decades. Advantages and disadvantages of PME/BME capacitors are:

1. PME

   Reliability (bias/temp) well established

   Mix of Palladium Silver Electrode

2. BME

   High density, commercial/cost

   Ni electrode

   Barium Titanate – $BaTiO_3$

   Tetragonal (0/130C) on face centers, Barium at corners

   Titanium, 1% nanometer offset, voltage/move/storage

   Thinner dielectrics/more layers than PME

   Increase in capacitance/volumetric efficiency

BME capacitance volumetric efficiency (μF/cm3) may not be increased without limit since the dielectric constant of ceramic $BaTiO_3$ is confined by the grain size effect. The volumetric efficiency will reach a peak and then decline with further reduction in dielectric thickness.

The reliability of a BME or PME capacitor is mainly determined by the reliability of the single dielectric layer. The number of dielectric layers in an MLCC behaves like an amplifying factor to make a problematic part degrade more quickly. BME capacitors usually have higher layers and pose a higher demand for dielectric material reliability. Lack of reliability of BME with much higher layers and lower thickness in comparison to PME capacitors is a key concern in use of these capacitors for high reliability applications. Recent studies [7] (see Figure 15) have shed some light on the behavior of a number of the BME capacitors and provided recommendations for their effective use. Further investigations are needed to narrow restriction on the use condition based on reliability.

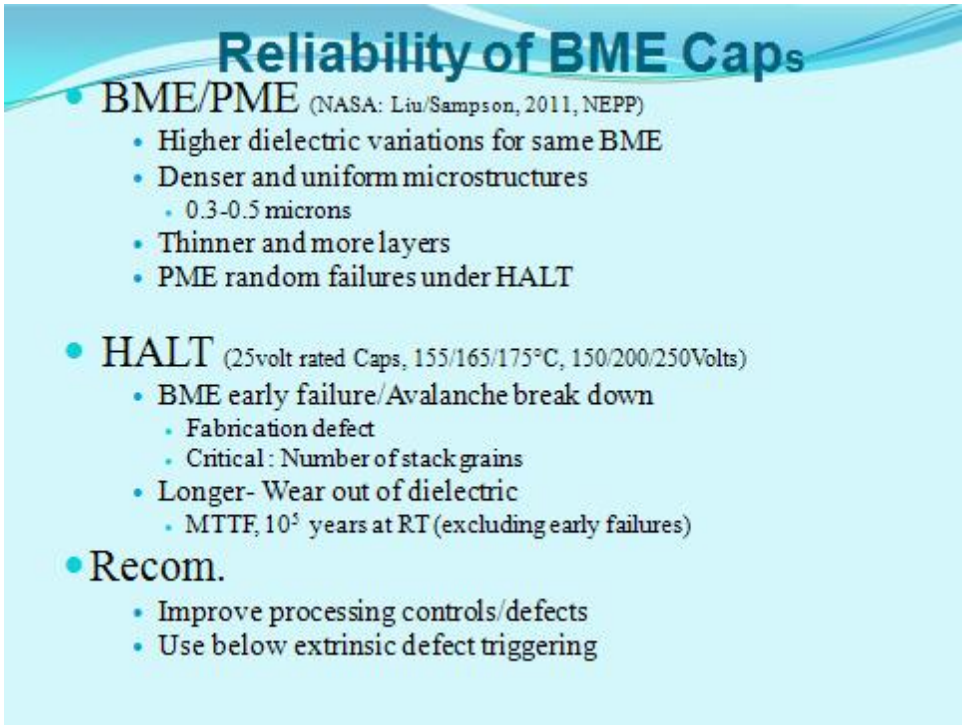

Figure 15. A brief reliability comparison of PM and BME capacitors (D. Liu, M. Sampson, [8])

3.2.5 BME Capacitor Grain Size Evaluation

The metallographic mount of chip capacitors, which had been removed from thermal cycled assemblies of CGA1752, were further polished in order to reveal grain microstructure. It is reported [7] that grain microstructure and size play an important role on capacitor reliability. Figure 16 shows an example of the thermal cycled BME capacitor layering at high magnifications to delineate grain size. To further emphasis grain structure, a number of grains were roughly traced since contrast between grains is low and it may be difficult to distinguish them when viewed in the SEM photomicrographs. Based on the scale given on the bottom of photomicrographs, grain sizes are in tenth of micron in length whereas the layers are in order of micron in thickness.

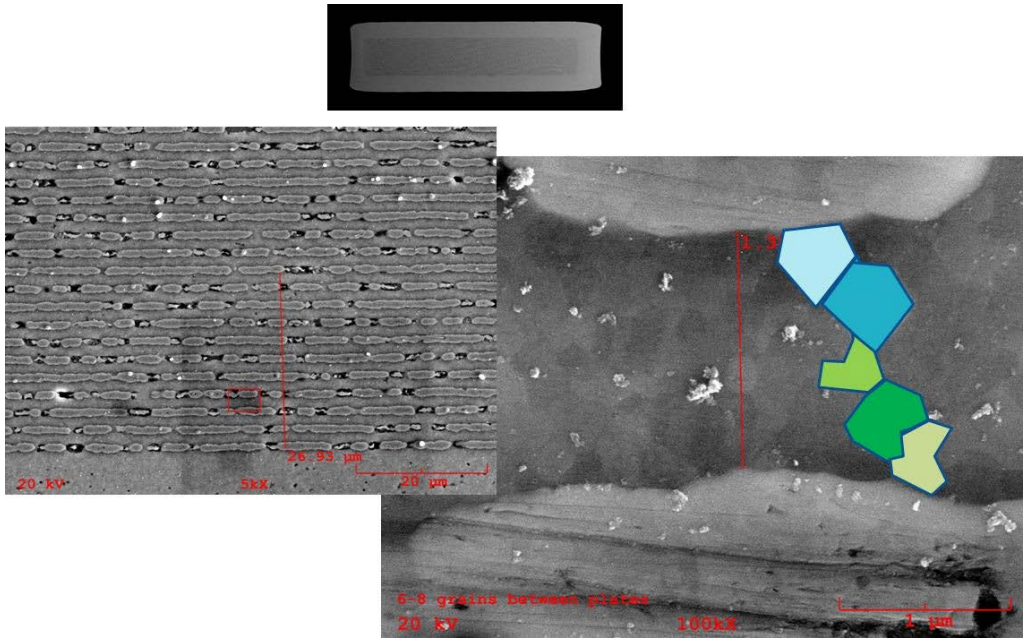

Figure 16. SEM photomicrographs of cross-section of a chip-capacitor showing layers and grain size distribution of $BaTiO_3$. Colors are traces of grain boundary to delineate grain sizes.

Another approach for revealing microstructure is to fracture capacitor and then perform SEM analysis on the fractured surface. Even though excellent contrast was achievable in the fractured surface (see Figure17), etching of surface for this sample was not sufficient to reveal the grain microstructures.

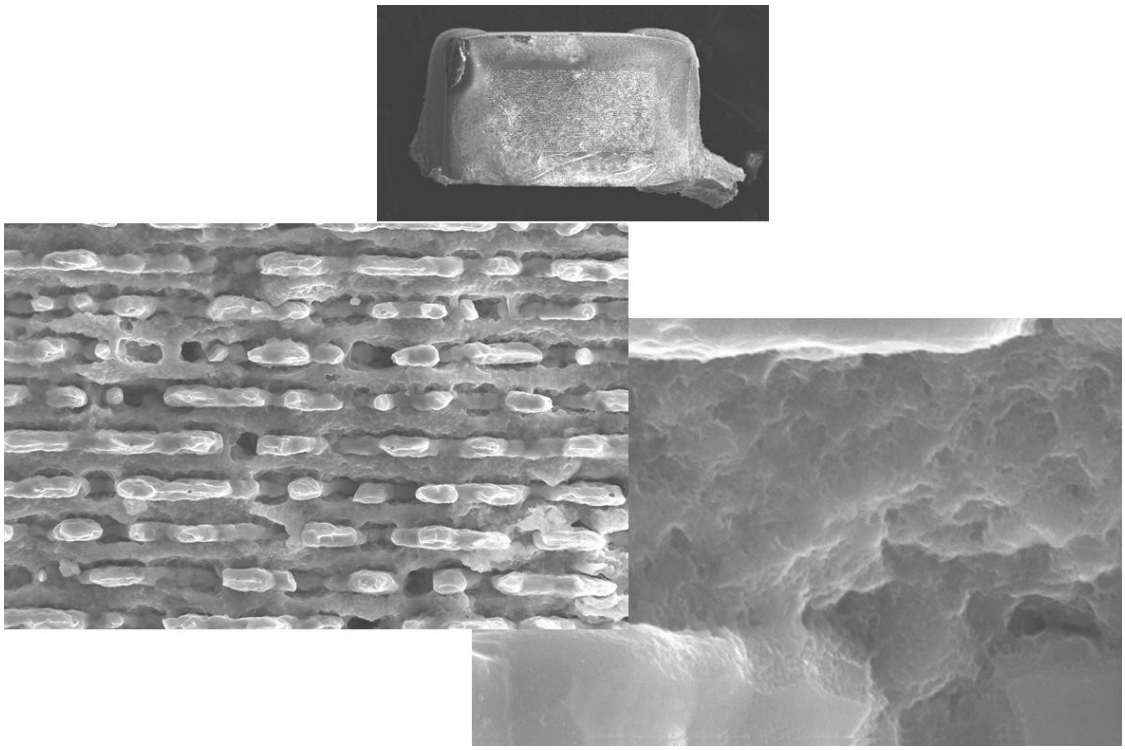

Figure 17. SEM photomicrographs of fracture surface of a chip-capacitor showing layers and indistinguishable grains of $BaTiO_3$.

3.3 Test Vehicle Design and Assembly Parameters for CGA1272/1752

To determine assembly reliability of the two CGA daisy-chain packages, the PCB was designed to match CGA patterns. Not all package styles from a manufacturer come in daisy-chain form; generally, manufacturers only select representative packages and offer them as daisy-chain, so the choice of packages for evaluation is limited. The daisy-chain patterns on PCB were designed to complement CGA patterns, forming a complete loop after assembly. The resistive loop is generally monitored during thermal cycling to allow detection of open loops due to solder joint opens of CGAs onto PCB. The two daisy-chain CGA packages, even though built by two different manufacturers, had roughly the same column dimensions.

A complex PCB was designed to accommodate the two CGA packages and also to provide sites for other advanced fine-pitch array and leaded/no-lead packages. Figure 18 shows the board design, with daisy-chain pattern, and how traces are routed to the edge of the board for daisy-chain monitoring.

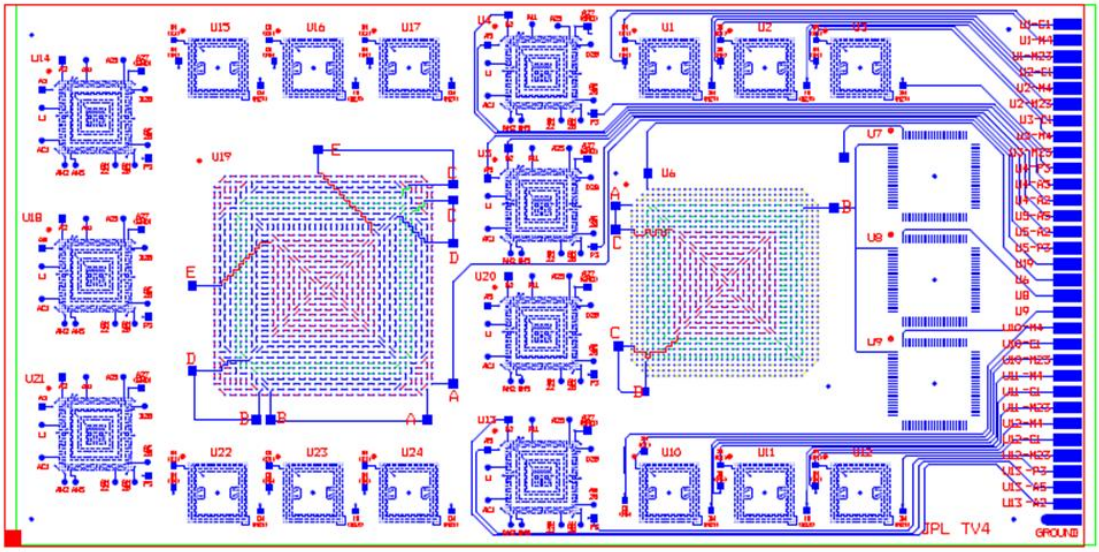

Figure 18. Test vehicle design showing both combined package and board daisy-chain patterns for the two CGA packages. A few other daisy-chain patterns currently not used for evaluation are also apparent in the design.

A design of experiments (DOE) technique was used to cover various aspects of processing and packaging assembly reliability. The following packages and parameters were evaluated as part of a larger DOE implementation:

- The CGA1752, with 1.0-mm pitch and 42.5-mm^2 body size, designed with enough space for rework evaluation at one side. Numerous daisy chains were designed on board to complement daisy chains on a package, in order to generate complete chains for solder joint failure monitoring. Probe pairs were added near packages to monitor subdivided daisy chains.
- The CGA1272, with 1.0-mm pitch and 37.5-mm^2 body size, designed with enough space for rework evaluation. Lead parts are designed to determine the influence of rework visually. Numerous daisy chains were designed on board to complement daisy chains on a package, in order to generate complete chains for solder joint failure monitoring. Probe pairs were added near packages to monitor subdivided daisy chains.
- Boards were made from high glass transition temperature (Tg) FR-4 materials with 0.093-inch thickness. They had a hot air solder leveling (HASL) tin-lead surface finish commonly used for tin-lead solder.

- A standard 6-mil-thick stencil was used for paste printing of the whole board when only the two CGAs are to be built. However, other stencil thicknesses or use of a mini stencil may be required to accommodate building a board of this complexity, or if reworking is performed.
- Three types of solder paste were evaluated for paste print quality. Solder paste volumes were measured at the four corners and at the center for several assemblies to document actual paste print volume, distribution, and solder paste release efficiency.
- Vapor phase reflow was used to assemble the two CGA packages. Placement of CGAs, however, was done using a rework station.

These assemblies were first subjected to inspection and daisy-chain continuity checks to determine manufacturing robustness of various package configurations. Figure 19 shows an assembled test vehicle. They will be then exposed to a number of environmental conditions to evaluate their reliability and failure mechanisms. Both the paste print quality evaluation and also inspection after assemblies are discussed below.

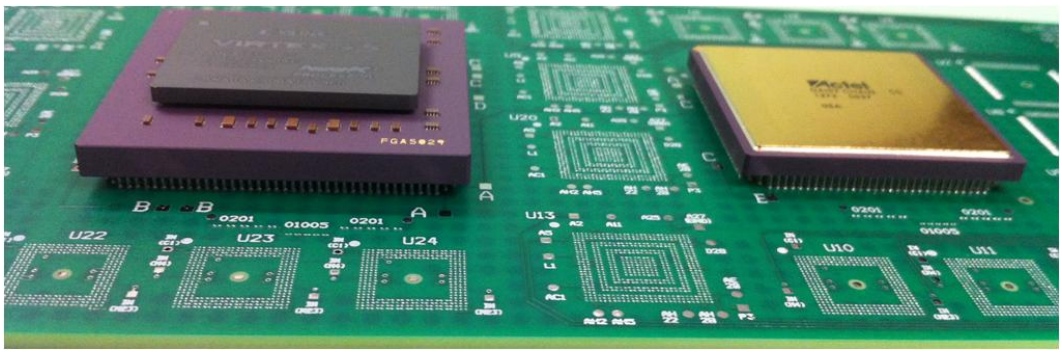

Figure 19. Assembled test vehicle showing the two CGA packages with different sizes and column styles.

3.4 Solder Paste Volume Measurement

Achieving a proper stencil design that accommodates both CGAs and other advanced packages is challenging. There are many variables to be considered, including stencil thickness, aperture opening, and solder paste type. The paste type is considered to be the most critical factor for finer pitch package assembly, but may have minimum effect on the assembly quality of CGA packages. Three types of solder pastes were considered:

- Type III (−325/+500, mesh size) RMA pastes, solder particle diameter between 20 and 45 microns, commonly used for conventional packages. Paste deposition on the PCB pad's patterns was accomplished using a paste print machine with standard parameters, including paste print speed and 1:1 aperture opening.
- Type IV (−400/+625, mesh size) RMA paste with slightly higher cost and solder particles (diameters between 20 and 38 microns) was used to improve assembly yield for conventional and potential fine pitch array packages.
- Type V (−500, mesh size) RMA paste, with even finer particles (diameters between 10 and 25 microns).

The rule of thumb for an aperture opening size is to be about four to five times the solder powder diameter. After deposition, each paste print was visually inspected using a microscope for detecting gross defects, such as bridging or insufficient paste deposition. On extremely rare occasions, print quality was improved by either adding a small amount of solder paste when insufficient paste was detected or by removing solder paste from the connecting pads when bridging was discovered. Figures 20 shows representative photomicrographs of paste print and quality for the CGA1272 and CGA1752 I/O packages. Note the daisy chain pattern on board that complements the packages.

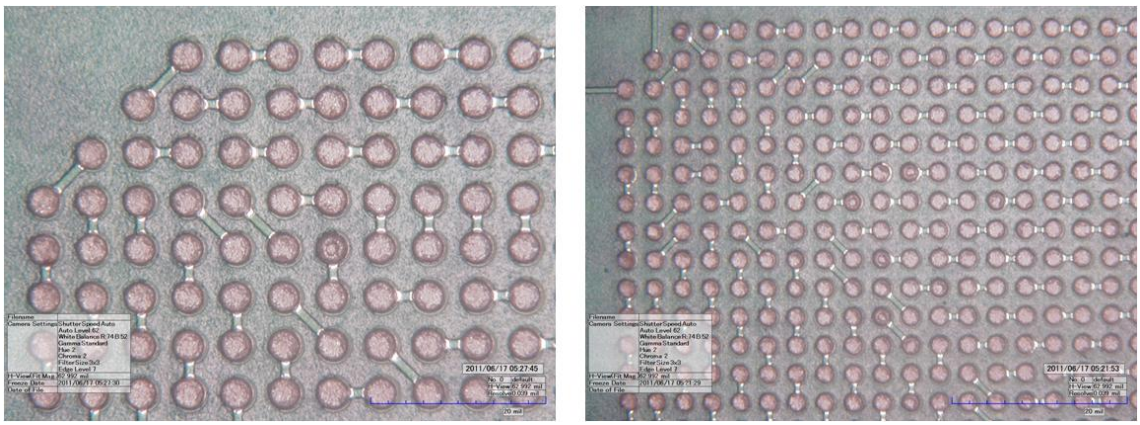

Figure 20. Representative photomicrographs of paste print deposition quality for the CGA1272 I/O (left) and CGA1752 I/O (right).

In addition, solder paste areas and heights were measured using a laser interferometer profilometer with a sophisticated three-dimensional (3D) measurement capability. Measurements were taken at numerous locations—including corner and center pads—to gather solder volume data and their corresponding distributions. Refer to previous report on this subject for the 3D solder-paste measurement plots and photomicrographs.

3.5 Attachment Procedures

Intentionally, a large number of fine pitch array advanced packages and leaded quad flat packages were designed close to the CGA packages. The reason for this configuration was to determine paste print quality and manufacturing challenges associated with a large column-grid-array package surrounded by small, fine pitch ones. Initial activity only concentrated on assembling large CGA packages, since these packages are new, with no heritage experience on assembly. Package placement was accomplished using a rework station.

Solder paste reflow was performed using a vapor phase reflow machine set up for the tin-lead process. Reflow profiles were based on a previously established profile that was tailored using a sample run with the attached thermocouple generating the reflow thermal profile. Vapor phase consists of an infrared preheating followed by a constant temperature boiling vapor zone. Infrared preheating temperature and time, as well as time in vapor phase, are the only key parameters that can be modified to achieve better solder attachment quality.

4.0 TEST RESULTS AFTER TV BUILD

4.1 Daisy-Chain Resistance Results

To verify assembly process acceptance, inspection and continuity of daisy chain of package/assembly provides an indication of quality of solder joint assembly. Daisy-chain resistances for CGA package assemblies were verified after the first test vehicle (TV) build and found to be continuous and acceptable. The resistance measurements were also taken for subsequent TVs after their built. Specifically, this provided the baseline to compare against any differences in resistivity for the type III–V solder pastes evaluated in this investigation. CGA1752 and CGA1272 had daisy-chain patterns, i.e., each package had pairs of connected pads, which by PCB design complemented specific pairs of connected PCB pads to build loops of continuous daisy chains. Loops cover continuity going from the PCB pad through solder joint at PCB level followed by column and solder joint at the package side. Continuous daisy-chain pattern indicates continuous path through both PCB and package solder joints; therefore, an open indicates a solder joint open. Five daisy-chain patterns are designed for CGA1752 and three patterns for CGA 1272. A gross short generally could be detected when lower-than-nominal resistance values were measured; shorts are more easily detected by X-ray. Except for relatively low solder balls, no shorts were observed for CGAs by X-ray. The results of manufacturing yield and daisy-chain resistances for various conditions of assembly using vapor reflow are summarized in Table 1. Manufacturing yield for CGAs was excellent, with no opens for those assembled.

Table 1. Summary of daisy-chain resistance measurements (in Ohms) within each CGA package, after assembly, using paste types III–V.

ID	Paste Type & Process	A-1752	B-1752	C-1752	D-1752	E-1752	A-1272	B-1272	C-1272
TV5-001	Type5 Tin-Lead Paste, Vapor Phase, Daisy Chain CGA1752 & CGA1272	7.61	10.71	10.61	11.50	12.02	1.92	2.53	2.15
TV5-002	Type3 Tin-Lead Paste, Vapor Phase, Daisy Chain CGA1752 & CGA1272	7.18	10.10	9.97	10.79	11.26	1.88	2.46	2.07
TV5-003	Type4 Tin-Lead Paste, Vapor Phase, Daisy Chain CGA1752 & CGA1272	7.61	10.74	10.63	11.48	12.01	1.88	2.50	2.11
TV5-004	Type4 Tin-Lead Paste, Vapor Phase, Daisy Chain CGA1752 & CGA1272	7.1	10.05	9.91	10.74	11.16	1.89	2.47	2.09
TV5-005	Type4 Tin-Lead Paste, Vapor Phase, Daisy Chain CGA1752 & CGA1272	7.19	10.1	9.95	10.81	11.34	1.83	2.18	2.06

4.2 Inspection

For high-reliability electronic applications, visual inspection is commonly performed by quality assurance (QA) personnel at various levels of packaging and assembly, known as mandatory inspection points (MIPs). Solder joints are inspected and accepted or rejected based on specific sets of workmanship criteria established for high-reliability applications. Further assurance is gained by subsequent short-time environmental exposure, including thermal storage, thermal cycling, vibration, mechanical shock, and so forth. These screening tests also allow detection of anomalies due to workmanship defects or design flaws at the system level. For space applications, it is usual for 100% visual inspection to be performed for the hybrid package, both pre-sealing (pre-cap) and after assembly prior to shipment. These screening tests also allow detection of anomalies due to workmanship defects or design flaws at the system level.

For CGA package assembly, visual inspection of peripheral columns with solder joints is possible if they are not blocked. Such inspection provides valuable information on solder joint attachment and process quality. It is impossible, however, to inspect hidden columns under the package. X-ray evaluation is needed to determine shorts and, on rare occasions, opens, for area array packages. For the test vehicle with daisy-chain package configuration, verifications were performed using:

1. Daisy-chain continuity checking
2. X-ray quality detection for shorts, and on rare occasions, for opens

3. Visual inspection with optical microscopy photographs of peripheral columns

For the CGA assemblies, except for solder balls, no shorts were detected by X-ray, which sometimes are apparent by being a smaller, darker area. In addition, no apparent cracks or other anomalies were observed with an optical microscope. Extensive X-ray and optical characterization was performed, but only a few representative photomicrographs documenting quality were shown.

4.3 X-Ray Characterization

X-ray inspection was performed, following visual inspection and the daisy-chain continuity check, to selectively verify package/assembly conditions. The 2D real time X-ray transmission system with oblique angle views was utilized for this inspection. Figure 21 shows representative X-ray photomicrographs for the CGA1752 and CGA1272 packages after assembly.

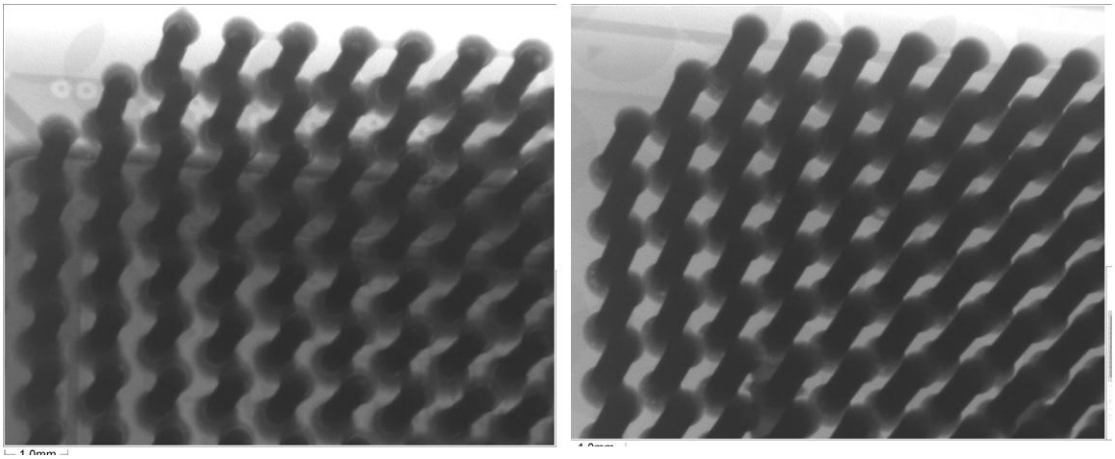

Figure 21. As-assembled X-ray photomicrographs for the CGA1272 I/O (left) and CGA1752 I/O.

4.4 Optical Microscopy Characterization

Visual inspection of peripheral columns was performed for most assemblies, since the board was designed for visual characterization (most of the PCBs were only populated with CGAs). Only outer row, and in some cases, second and third rows could be assessed for solder joint quality. The representative photomicrographs in Figure 21 show the quality of solder joints for CGA1752 and CGA1272 I/O assemblies. Note that solder joint fillet formations are different for the pure column and copper-wrapped solder columns. Solder joints were generally acceptable even though they appear different solder wetting configuration and solder coverage of column periphery.

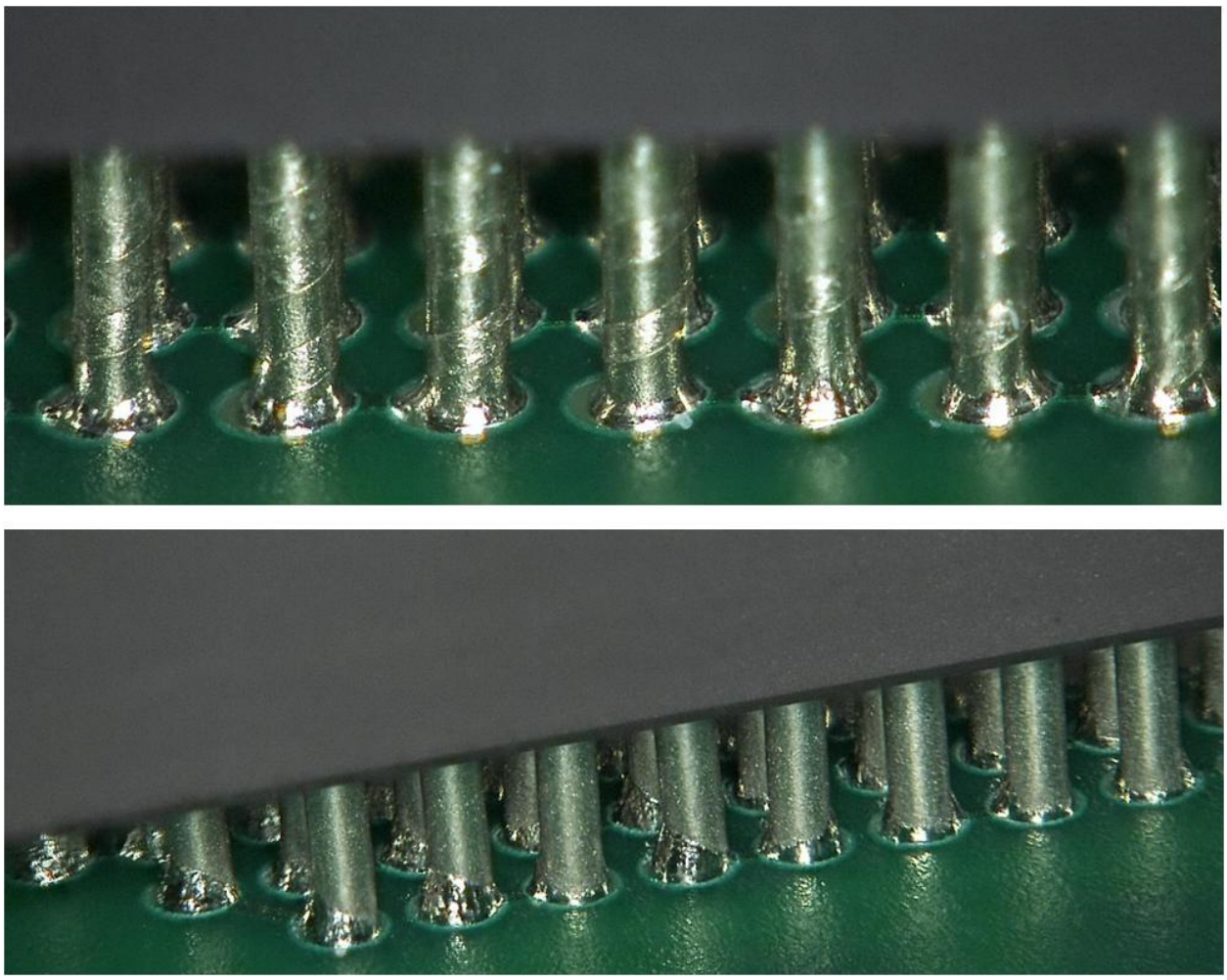

Figure 22. Representative photomicrographs of solder joint quality after assembly for CGA1272 (top) and CGA1752 (bottom).

4.5 Thermal Cycle Test Profiles

Two different thermal cycles were used with the following thermal profiles:

4. Cycle A: Ranged from –55° to 100°C with a 2° to 5°C/min (3°C/min) heating/cooling rate. Dwells at extreme temperatures were about 17 minutes with duration of 140 minutes.
5. Cycle B: Ranged from –55° to 125°C with a 2° to 5°C/min (3°C/min) heating/cooling rate. Dwells at extreme temperatures were about 15 minutes with duration of 210 minutes for each cycle.

For quality assurance verification, damage progress documentation, and sample size limitation, visual inspection of peripheral columns also performed at thermal cycling. For ease of visual inspection, test vehicles were populated only with one or two CGAs. This enables solder joint and column integrity verification for these two package types since enough gap exists between PCB and package surfaces. The criteria for an open solder joint specified in IPC-9701 were used as guidelines to interpret electrical interruptions. Opens are verified manually at convenient intervals, but generally every 100 thermal cycles or less. Daisy-chain measurements were performed at RT during cycling and were compared to resistance values prior to cycling after assembly. The resistance values after 100 and 200 of condition A and B thermal cycles are presented in Table 2. No solder joint failure was detected under either condition to two hundred thermal cycles.

Table 2. Summary of daisy-chain resistance measurements (in Ohms) within each CGA package, after assembly and thermal cycles (–55°/100°C and –55°/125°C) at 100 and 200 cycles.

ID	Paste Type & Process	A-1752	B-1752	C-1752	D-1752	E-1752	A-1272	B-1272	C-1272
TV5-001	Type5 Tin-Lead Paste, Vapor Phase, Daisy Chain CGA1752 & CGA1272	7.61	10.71	10.61	11.50	12.02	1.92	2.53	2.15
	100 Cycles (-55 °C to 125 °C)	***7.78***	***10.92***	***10.82***	***11.72***	***12.25***	***2.01***	***2.62***	***2.24***
	200 Cycles (-55 °C to 125 °C)	***7.67***	***10.77***	***10.68***	***11.55***	***12.1***	***1.99***	***2.61***	***2.23***
TV5-002	Type3 Tin-Lead Paste, Vapor Phase, Daisy Chain CGA1752 & CGA1272	7.18	10.10	9.97	10.79	11.26	1.88	2.46	2.07
	100 Cycles (-55 °C to 125 °C)	***7.36***	***10.32***	***10.19***	***11.04***	***11.52***	***1.95***	***2.57***	***2.15***
	200 Cycles (-55 °C to 125 °C)	***7.25***	***10.16***	***10.04***	***10.88***	***11.34***	***1.94***	***2.54***	***2.14***
TV5-003	Type4 Tin-Lead Paste, Vapor Phase, Daisy Chain CGA1752 & CGA1272	7.61	10.74	10.63	11.48	12.01	1.88	2.50	2.11
	100 Cycles (-55 °C to 125 °C)	***7.81***	***11***	***10.8***	***11.75***	***12.26***	***1.99***	***2.61***	***2.23***
	200 Cycles (-55 °C to 125 °C)	***7.66***	***10.79***	***10.69***	***11.55***	***12.07***	***1.97***	***2.59***	***2.2***
TV5-004	Type4 Tin-Lead Paste, Vapor Phase, Daisy Chain CGA1752 & CGA1272	7.1	10.05	9.91	10.74	11.16	1.89	2.47	2.09
	100 Cycles (-55 °C to 100 °C)	***7.16***	***10.09***	***9.95***	***10.78***	***11.21***	***1.95***	***2.54***	***2.16***
	200 Cycles (-55 °C to 100 °C)	***7.16***	***10.1***	***9.95***	***10.77***	***11.22***	***1.95***	***2.54***	***2.15***
TV5-005	Type4 Tin-Lead Paste, Vapor Phase, Daisy Chain CGA1752 & CGA1272	7.19	10.1	9.95	10.81	11.34	1.83	2.18	2.06
	100 Cycles (-55 °C to 100 °C)	***7.24***	***10.17***	***10.03***	***10.88***	***11.43***	***1.89***	***2.25***	***2.16***
	200 Cycles (-55 °C to 100 °C)	***7.27***	***10.18***	***10.01***	***10.88***	***11.42***	***1.91***	***2.27***	***2.17***

4.5.1 Damage Progress with Thermal Cycling (–55°/100°C)

Damage progress with thermal cycling was established using an optical microscope. Figures 23–25 present representative photomicrographs of solder joint condition and damage progress due to thermal cycling in the range of –55° to 100°C up to 200 cycles. Damage due to thermal cycling, noticeable from these photomicrographs, can be categorized as follows:

- CGA1272 with Cu-spiral column showed good solder joint uniformity and wetting, concave solder surrounding columns. Minimum solder damage was detected due to 100 thermal cycles that slightly increased at 200 cycles; solder/columns showing signs of graininess representing tin-lead solder grain growth due to exposure at 100°C during thermal cycling. Column distortions were minimal, except for graininess of solder exposed between the Cu wrap at 200 thermal cycles. In addition, no apparent column shifts due to shear-induced deformation due to CGA/PCB CTE during thermal cycling.
- CGA1752 with high lead solid-solder columns showed partial solder joint coverage of column perimeter with good wetting on the coverage area. Several displaced columns showing a larger corner column shift are apparent. Some column distortions were observed, signs of graininess of solder joints also observable at 200 thermal cycles. In addition, slight apparent column shifts due to shear-induced deformation due to CGA/PCB CTE during thermal cycling.

In general, less deformation occurred due to thermal cycling to 200 cycles for CGA1272 having lower package size and high column rigidity due to Cu wrap— both factors cause to induce lower thermal stress on solder joint attachment— compared to larger CGA1752 package assembly with no strengthening Cu wrap.

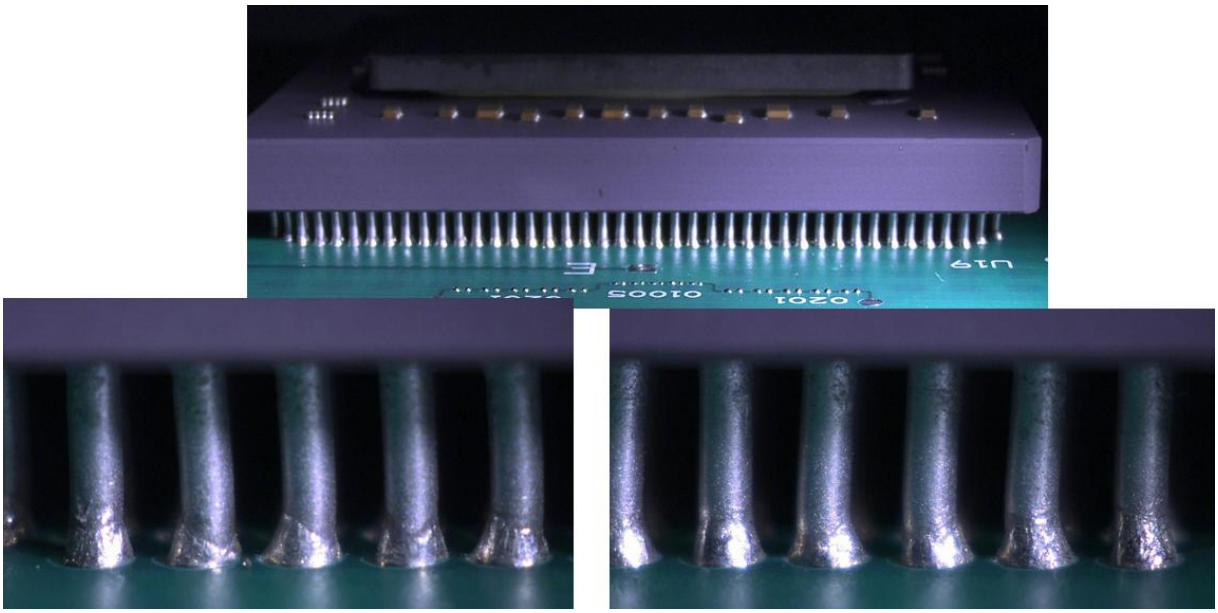

Figure 23. Representative photomicrographs of solder joint quality after 100 thermal cycles (–55°/100°C) for CGA1752.

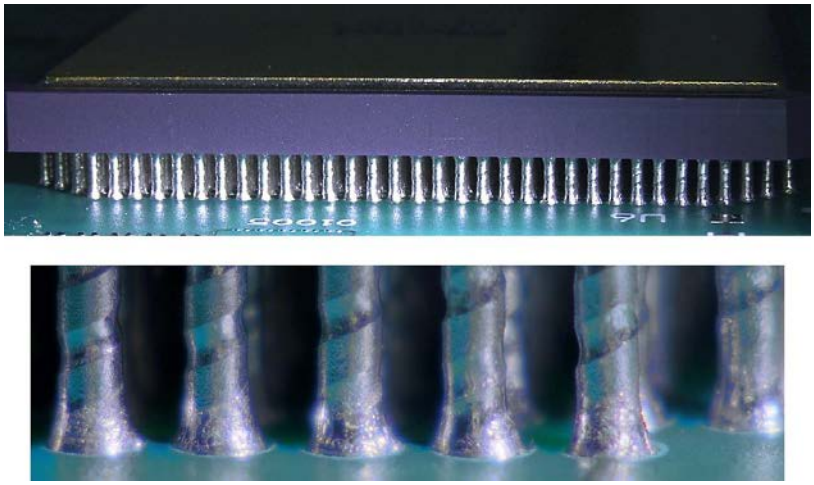

Figure 24. Representative photomicrographs of solder joint quality after 100 thermal cycles (–55°/100°C) for CGA1272.

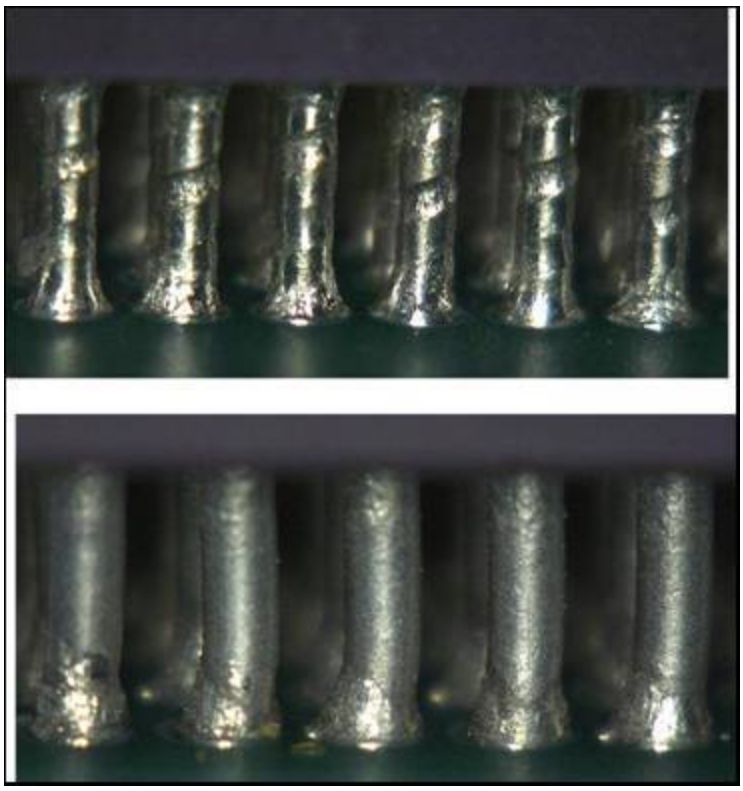

Figure 25. Representative photomicrographs of solder joint quality after 200 thermal cycles (–55°/100°C) for CGA1272 (top) and CGA1752 (bottom).

4.5.2 Damage Progress with Thermal Cycles (–55°/125°C)

Visual inspection was performed to establish damage progress of outer columns of CGAs at thermal cycling intervals by optical microscopy. Figures 26–27 present representative photomicrographs of solder joint condition and damage progress due to thermal cycling in the range of –55° to 125°C at 200 cycles. Damage due to thermal cycling, noticeable from these photomicrographs, can be categorized as follows:

- CGA1272 with Cu spiral column showed good solder joint uniformity and wetting. Some solder damage at 200 cycles showing signs of graininess representing of tin-lead solder grain growth due to exposure at 125°C during thermal cycling. Column distortions were minimal, except for signs of graininess of solder between Cu wrap, at 200 thermal cycles with no apparent column shifts due to thermal cycling.
- CGA1752 with high lead solder column showed partial solder joint coverage of column perimeter and good wetting on the coverage area. Several displaced columns showing a larger corner column shift are apparent. Magnified photomicrographs of corner columns clearly show signs of damage and even microcrack formation. Damage is much more severe when compared to previous thermal cycle condition with 100°C maximum TC.

Similarly to thermal cycle condition A, less deformation occurred for CGA1272 with lower package dimension and higher rigidity of columns—both factors induce lower thermal stress on solder joint attachment—compared to larger CGA1752 package and lower rigid pure solder columns. Note also that solder damage and microcracks induced especially for CGA1752 were generally significantly higher than those under A cycling condition.

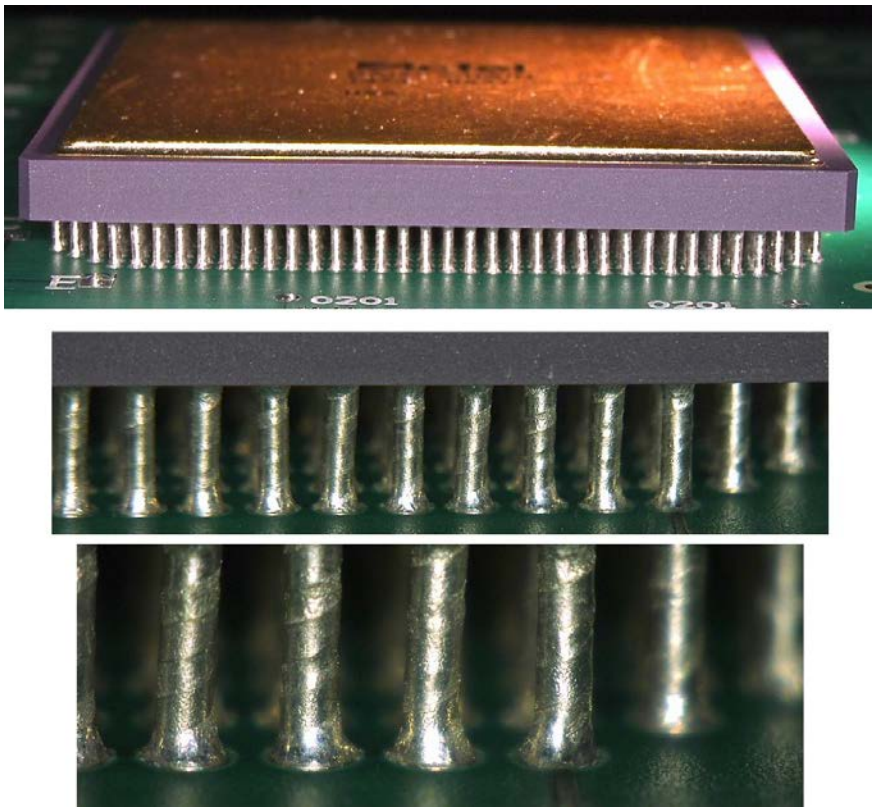

Figure 26. Representative photomicrographs of solder joint quality after 200 thermal cycles (–55°/125°C) for CGA1272.

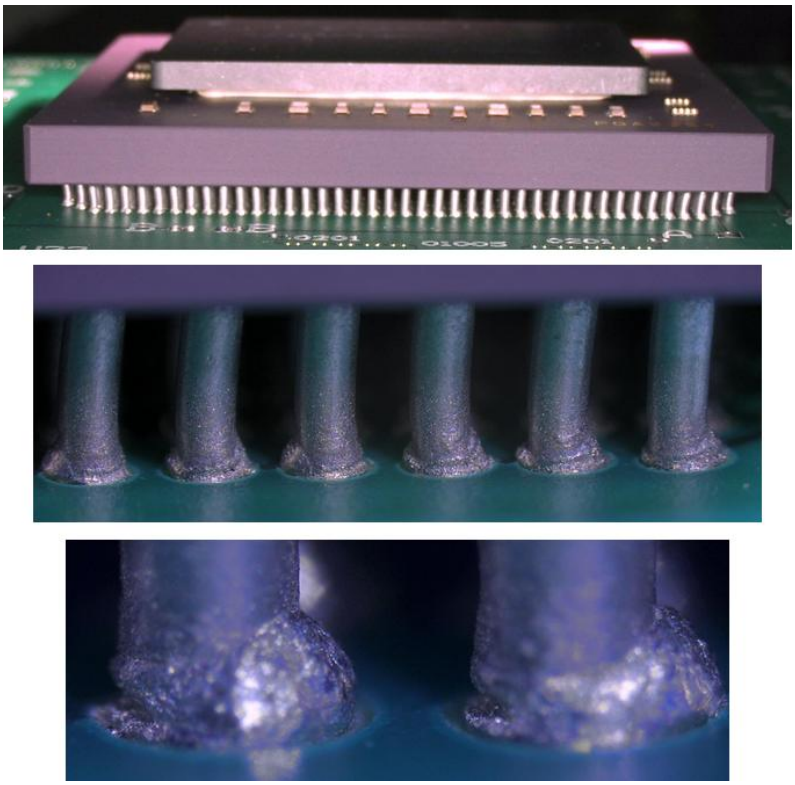

Figure 27. Representative photomicrographs of solder joint quality after 200 thermal cycles (–55°/125°C) for CGA1752.

5.0 EXPERIMENTAL APPROACHES FOR LGA PACKAGES

5.1 LGA Column Attach

This report covered many aspects of advanced area array packaging and high density printed circuit boards. The purpose of the following aspect of the investigation was to characterize the reliability of LGA1517 packages with 1-mm pitch. LGAs were subject to both copper-wrapped column and microspring coil attachment for subsequent evaluation. Column attachment integrity was evaluated by subjecting a CGA version to isothermal aging and pull tested before and at intervals during environmental aging. Figure 22 shows photomicrographs of the LGA package after it was transformed to CGA.

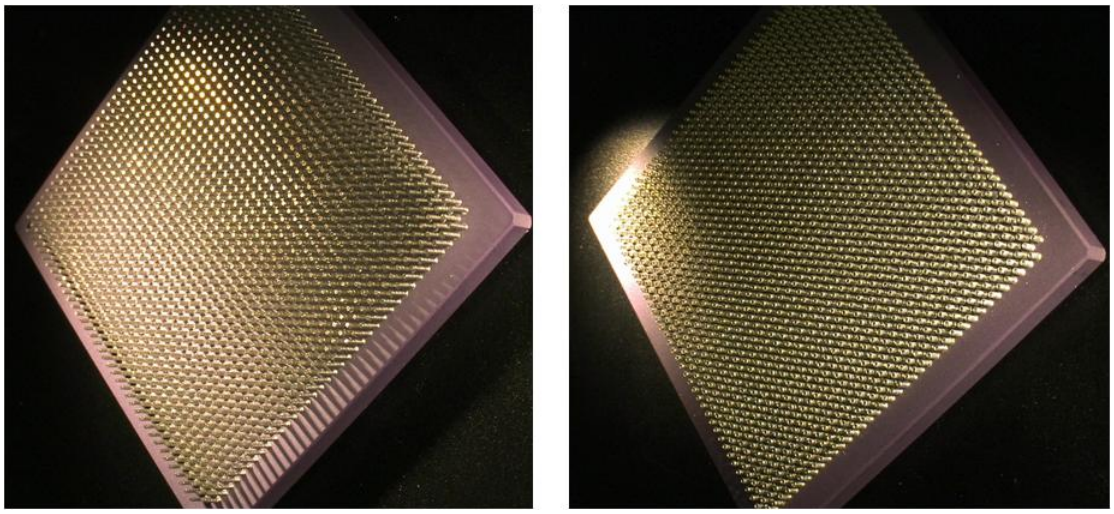

Figure 28. Representative photomicrographs of an LGA package after copper column (left) and micro-spring coil column (right) attachment.

5.2 Test Vehicle Design and Assembly Parameters for CGA1272/1509/1517

To determine assembly reliability of the CGAs made from the LGA, the test vehicle design with CGA1752 pad pattern was used to accommodate assembly of these sets of lower I/O CGAs. Two TV designs were used, one with the same pad size pattern as those for CGA1752, TV5, and the other with smaller pad sizes for CGAs (TV4). Smaller pad sizes required for the lower diameter columns; such design also provided additional reliability data for CGA1272 with lower than ideal solder volumes. Not all package styles from a manufacturer come in daisy-chain pattern; generally, manufacturers only select representative packages and offer them as daisy-chain, so the choice of packages for evaluation is limited.

Only CGA1272 had daisy-chain pattern. For this package, the daisy-chain patterns on PCB were designed to complement CGA1272 package patterns, forming complete chain loops after assembly. The resistive loops of this package assembly were monitored during thermal cycling to allow detection of an open loop due to solder joint opens of either PCB or package sides. The other CGAs (1509 and 1517) with no daisy-chain configurations were monitored by visual inspection of peripheral columns and destructive cross-sectioning, and dye-and-pry at appropriated thermal cycles.

A DOE technique was used to cover various aspects of processing and packaging assembly reliability. The following packages and parameters were evaluated as part of a larger DOE implementation:

- The CGA1272, with 1.0-mm pitch and 37.5-mm^2 body size, was designed with enough space for rework evaluation. Numerous daisy-chain loops were designed on board to complement daisy chains on a package, in order to generate complete chains for solder joint failure monitoring. Probe pairs were added near packages to monitor subdivided daisy chains.

- The CGA1509, with 1.0-mm pitch and 40-mm^2 body size, was placed on CGA1752 pattern configuration with a larger pad pattern. This allowed comparison with data generated for CGA1272 as control without redesign of the board. Having no daisy-chain loops, the quality assurance monitoring was carried out through visual inspection of peripheral columns as well as destructive testing evaluation.
- Boards were made from high glass transition temperature (Tg) FR-4 materials with 0.093-inch thickness. They had an HASL tin-lead surface finish commonly used for tin-lead solder. Another board with smaller pad sizes was fabricated to accommodate CGAs with 15-mil column size.
- A standard 6-mil-thick stencil was used for paste printing of the whole board when only the two CGAs are to be built. However, other stencil thicknesses or use of a mini stencil may be required to accommodate building a board of this complexity, or if reworking is performed. A stencil was designed with smaller aperture opening for test vehicle with smaller pad size design.
- Two types of solder paste were evaluated for paste print quality. Solder paste volumes were measured at the four corners and at the center for several assemblies to document actual paste print volume, distribution, and release efficiency of solder paste.
- Vapor phase reflow was used to assemble most CGA packages. Placement of CGAs, however, was done using a rework station.
- Rework station was also used for reflowing; in this evaluation, only one CGA1272 package was used.

After paste prints and inspection characterization to assure their acceptance were performed, CGAs were placed onto solder paste using a rework station. Solder paste reflow was performed using a vapor phase reflow machine set up for tin-lead process. Reflow profiles were tailored based on a previously established profile, the same profile as narrowed for other CGAs. These assemblies were first subjected to inspection and daisy-chain continuity checks for CGA1272 package to determine manufacturing robustness of various package configurations. Then they were exposed to a number of environmental conditions to evaluate their reliability and failure mechanisms. Results of inspection and environmental tests are presented.

5.3 Optical Microscopy Characterization of LGA/CGA

5.3.1 After Assembly

LGAs with copper-spiral solder columns and those with microspring coils were assembled onto two different PCBs with both standard and smaller pad diameters; this accommodated the two column/spring diameters. During the processing of LGAs with microspring coils, a CGA1272 was also assembled onto the board as a baseline for process and reliability evaluation. Visual inspection of peripheral columns was performed for these assemblies since the board was designed for visual characterization, especially since most of the PCBs were only populated with CGAs. Only outer rows, and in some cases, second and third rows, could be assessed for solder joint quality. Verification by daisy-chain resistance measurement was not possible since LGAs had no daisy-chain package design. The photomicrograph in Figure 29 shows the quality of solder joints for microspring coil of a column CGA assembly. Note that solder joint fillet formations are different since there are no solid solder columns; however, good quality solder fillet formation is apparent. Figure 30 shows solder joint quality of a copper-wrapped column assembly.

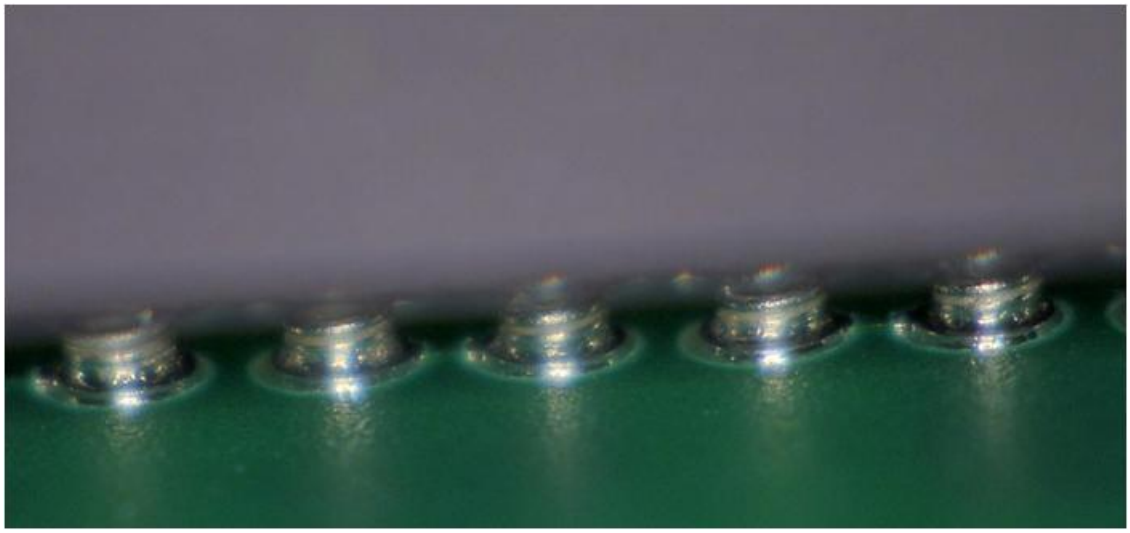

Figure 29. Representative photomicrographs of solder joint quality after assembly for microspring coil column CGA1571**.**

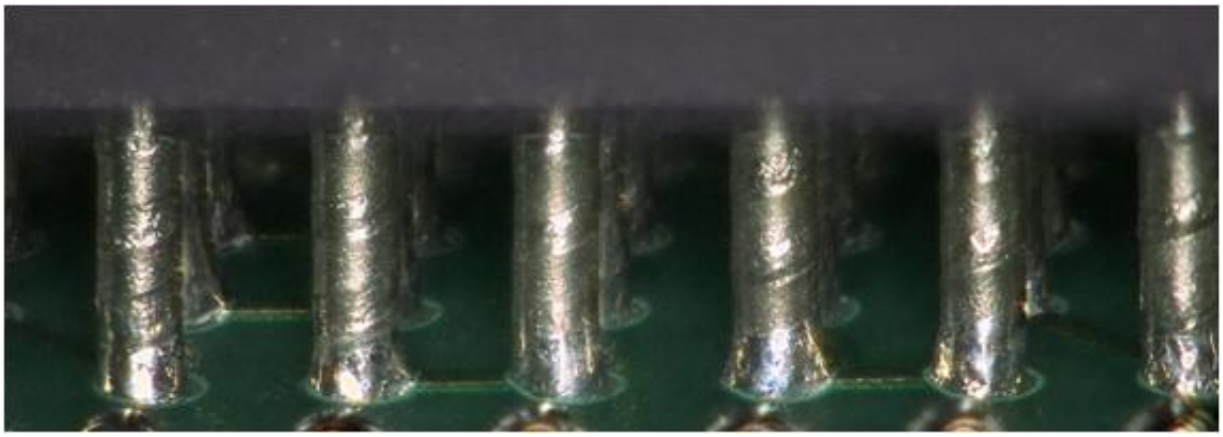

Figure 30. Representative photomicrographs of solder joint quality after assembly for CGA1571 with copper-wrapped solder columns**.**

5.4 Thermal Cycle Test Results (–55°/100°C)

Table 3 presents a summary of assembly condition of CGA1509, CGA1517, and daisy-chain resistance values for CGA1272 after assemblies. Condition of assemblies are presented in the column 2 of the table describing details on the board design types (TV4 or TV5), paste types (type 4 or type 5), CGA types (1509, 1517, 1272), column types (solid or Cu-spiral column), and daisy-chain values (3 patterns) for CGA1272 assemblies as fabricated and after thermal cycling (–55°C to 100°C). These assemblies were subjected to condition A cycling, ranging from –55°C to 100°C with a 3°C/min heating/cooling rate and dwells at the extreme temperatures were 17 minutes with duration of 140 minutes.

The criteria for an open solder joint specified in IPC-9701 were used as guidelines to interpret electrical interruptions. Opens were verified manually at convenient cycling intervals, but also at 100 and 200 thermal cycles. Measurements were performed at RT for CGA1272 that had daisy-chain configuration and compared to resistance values prior to thermal cycling to identify opens. The resistance values after 100 and 200 cycles indicated no failures, except TV5-032 that failed after assembly build. This package was assembled using rework station, not vapor phase reflow as described in the summary column.

Table 3. Summary of daisy-chain resistance measurements (in Ohms) within each CGA package, after assembly and thermal cycles (–55°/100°C) at 100 and 200 cycles

ID	Paste Type & Process	CGA	A-1272	B-1272	C-1272
TV5-011	Type5 Tin-Lead Paste, Vapor Phase, CGA1517 MicroSpring and CGA1272 DC	**1517**	1.89	2.49	2.15
	100 Cycles (-55 °C to 100 °C)		1.99	2.57	2.49
	200 Cycles (-55 °C to 100 °C)		1.96	2.57	2.53
TV5-014	Type4 Tin-Lead Paste, Vapor Phase, CGA1517 MicroSpring and CGA1272 DC	**1517**	1.85	2.42	2.04
	100 Cycles (-55 °C to 100 °C)		*1.91*	*2.5*	*2.11*
	200 Cycles (-55 °C to 100 °C)		*1.91*	*2.5*	*2.12*
TV5-017	Type4 Tin-Lead Paste, Vapor Phase/Stencil 5, CGA1517 Cu Column and CGA1272 DC	**1517**	1.82	2.39	2.07
	100 Cycles (-55 °C to 100 °C)		*1.9*	*2.48*	*2.11*
	200 Cycles (-55 °C to 100 °C)		*1.87*	*2.45*	*2.1*
TV4-021	Type5 Tin-Lead Paste, Vapor Phase, CGA1517 Cu Column and No CGA1272 DC	**1517**	NA	NA	NA
	100 Cycles (-55 °C to 100 °C)		NA	NA	NA
	200 Cycles (-55 °C to 100 °C)		NA	NA	NA
TV5-032	Type5 Tin-Lead Paste, Vapor Phase, CGA1509 90/10 Column and CGA1272 Rework Station	**1509**	1.67	open	0.43
	100 Cycles (-55 °C to 100 °C)		*1.7*	*open*	*0.46*
	200 Cycles (-55 °C to 100 °C)		*1.73*	*open*	*0.47*

In addition to daisy-chain monitoring for CGA1272, visual inspection was also performed by optical microscopy to establish damage progress of outer columns of all CGA assemblies at thermal cycle intervals. Figure 31 presents representative photomicrographs of solder joint condition of microspring columns and damage due to thermal cycling in the range of −55°C to 100°C at 200 cycles. Shiny appearance of solder joint reflection light from the microspring column attachment clearly indicates extremely minor damage induction due to 200 thermal cycling.

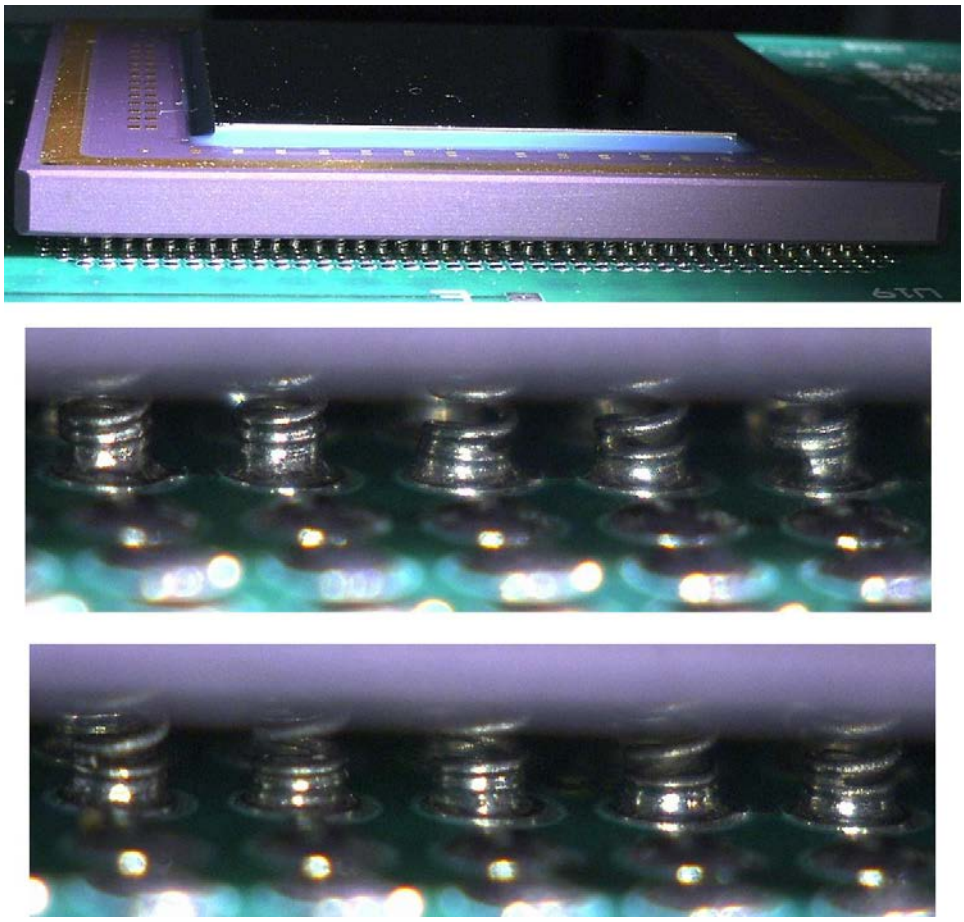

Figure 31. Representative photomicrographs of solder joint quality of microspring column attachment after 200 thermal cycles (–55°/100°C) for CGA1517.

5.5 Thermal Cycle Test Results (–55°/125°C)

Table 4 presents a summary of assembly condition of CGA1509, CGA1517, and daisy-chain resistance values for CGA1272 after assemblies. Condition of assemblies are presented in column 2 of the table describing details on the board design types (TV4 or TV5), paste types (type 4 or type 5), CGA types (1509, 1517, 1272), column types (solid or Cu-spiral column), and daisy-chain values (3 patterns) for CGA1272 assemblies as fabricated and after thermal cycling. They were subjected to cycling ranging from –55°C to 125°C with a 3°C/min heating/cooling rate and dwells at the extreme temperatures were 15 minutes with duration of 210 minutes. The criteria for an open solder joint specified in IPC-9701 were used as guidelines to interpret electrical interruptions. Opens were verified manually at convenient cycling intervals, but also at 100 and 200 thermal cycles. Measurements were performed at RT for CGA1272 that had daisy-chain loops and compared to resistance values prior to thermal cycling to identify opens. The resistance values after 100 and 200 cycles indicate no failures, except the TV4-024 that failed after assembly build due to an attempt to induce intentional defects for evaluation.

Table 4. Summary of daisy-chain resistance measurements (in Ohms) within each CGA package, after assembly and thermal cycles (–55°/125°C) at 100 and 200 cycles

ID	Paste Type & Process	CGA	A-1272	B-1272	C-1272
TV5-012	Type4 Tin-Lead Paste, Vapor Phase, CGA1517 MicroSpring and CGA1272 DC	**1517**	1.88	2.48	2.1
	100 Cycles (-55 °C to 125 °C)		*1.95*	*2.57*	*2.18*
	200 Cycles (-55 °C to 125 °C)		*1.92*	*2.53*	*2.15*
TV5-013	Type4 Tin-Lead Paste, Vapor Phase, CGA1517 MicroSpring and CGA1272 DC	**1517**	1.87	2.45	2.09
	100 Cycles (-55 °C to 125 °C)		*1.92*	*2.53*	*2.17*
	200 Cycles (-55 °C to 125 °C)		*1.91*	*2.52*	*2.15*
TV5-015	Type4 Tin-Lead Paste, Vapor Phase/Stencil 4, CGA1517 Cu Column and CGA1272 DC	**1517**	1.88	2.48	2.11
	100 Cycles (-55 °C to 125 °C)		*1.97*	*2.57*	*2.19*
	200 Cycles (-55 °C to 125 °C)		*1.97*	*2.55*	*2.19*
TV5-016	Type4 Tin-Lead Paste, Vapor Phase/Stencil 5, CGA1517 Cu Column and No CGA1272 DC	**1517**	1.86	2.45	2.07
	100 Cycles (-55 °C to 125 °C)		*1.9*	*2.51*	*2.14*
	200 Cycles (-55 °C to 125 °C)		*1.89*	*2.51*	*2.13*
TV4-022	Type4 Tin-Lead Paste/Stencil4, Vapor Phase, CGA1517 Cu Column and CGA1272 DC	**1517**	1.94	2.53	2.11
	100 Cycles (-55 °C to 125 °C)		*1.98*	*2.57*	*2.18*
	200 Cycles (-55 °C to 125 °C)		*1.98*	*2.57*	*2.16*
TV4-023	Type4 Tin-Lead Paste/Stencil4, Vapor Phase, CGA1517 Cu Column and CGA1272 DC-Ink Defect	**1517**	1.98	2.57	2.16
	100 Cycles (-55 °C to 125 °C)		*2.05*	*2.65*	*2.23*
	200 Cycles (-55 °C to 125 °C)		*2.02*	*2.63*	*2.21*
TV4-024	Type4 Tin-Lead Paste/Stencil4, Vapor Phase, CGA1517 Cu Column and CGA1272 DC-Kapton Defect	**1517**	Open	2.54	2.11
	100 Cycles (-55 °C to 125 °C)		*Open*	*2.62*	*2.19*
	200 Cycles (-55 °C to 125 °C)		*Open*	*2.61*	*2.19*
TV5-031	Type4 Tin-Lead Paste, Vapor Phase, CGA1509 90/10 Column and CGA1272 DC	**1509**	1.92	2.52	2.14
	100 Cycles (-55 °C to 125 °C)		*1.95*	*2.54*	*2.17*
	200 Cycles (-55 °C to 125 °C)		*2*	*2.59*	*2.21*
TV5-035	Type5 Tin-Lead Paste, Vapor Phase, CGA1509 90/10 Column and CGA1272 DC	**1509**	1.95	2.77	2.39
	100 Cycles (-55 °C to 125 °C)		*2.01*	*278*	*2.41*
	200 Cycles (-55 °C to 125 °C)		*1.8*	*2.75*	*2.4*
TV5-036	Type5 Tin-Lead Paste, Vapor Phase, CGA1509 90/10 Column and CGA1272 DC	**1509**	2	2.61	2.21
	100 Cycles (-55 °C to 125 °C)		*1.92*	*2.53*	*2.16*
	200 Cycles (-55 °C to 125 °C)		*1.95*	*2.56*	*2.18*

In addition to daisy-chain monitoring for CGA1272, visual inspection was also performed to establish damage progress of outer columns of all CGA assemblies at thermal cycle intervals by optical microscopy. Figure 32 presents representative photomicrographs of solder joint condition of microspring columns and damage due to thermal cycling in the range of –55°C to 125°C at 200 cycles. Slight darker appearance of solder joints at the PCB side of microspring column attachments indicates minimum sign of damage due to 200 thermal cycling.

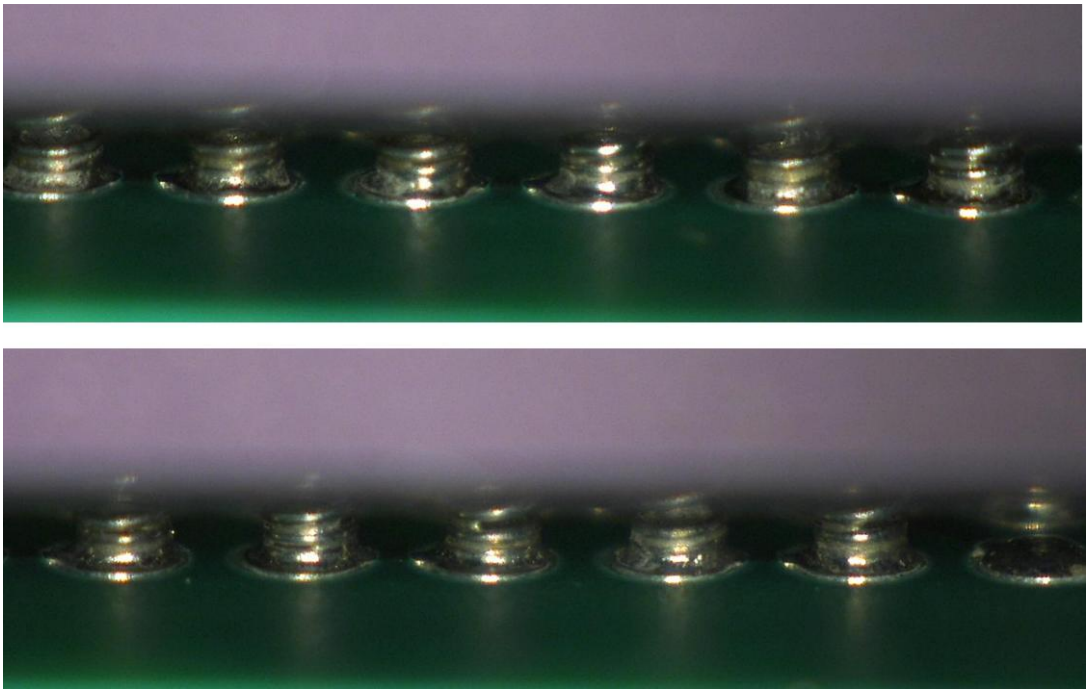

Figure 32. Representative photomicrographs of solder joint quality of microspring column attachment after 200 thermal cycles (–55°/125°C) for CGA1517.

5.6 Direct LGA Assembly on PCB

This section covers direct attachment of LGA1517 package with 1-mm pitch onto PCB to understand more generic issues associated with land-grid-array package attachment. For high reliability applications, this approach may become a popular approach with a much wider implementation of restriction of hazardous substances (ROHS). LGA in plastic package version with much smaller sizes has been available for thinner consumer products because of lower cost and lower assembly standoff compared to ball-grid-array version. High coefficient of thermal expansion (HCTE) ceramic LGA has been recently introduced replacing HCTE BGA packages. The LGA solder interconnect is formed solely by solder paste applied at the board assembly because there are no sphere attached to the LGA.

For HCTE LGA, a lower standoff height of approximately 0.06 mm to 0.1 mm, depending on solder paste volume and PCB geometry, could be achieved. The pad surface finish of LGA is generally electroless gold plating, 0.1 to 0.5 μm, over electroless nickel. The LGAs with such surface finish become ROHS compliant, including the exemption given for high-lead bump use in the flip-chip die. Key benefits of an LGA package over a BGA package include:

- LGA eliminates risk that customers receive components with missing or damaged spheres due to shipping or handling
- LGA devices can be used for either lead containing or lead-free assemblies depending on the type of solder paste used in surface mount technology (SMT) assembly

- LGA devices have a lower mounted height than BGA; this can allow for more space above the device for a heat-sink solution or for small form-factor applications
- Board-level reliability of HCTE ceramic version with lead-free solder paste shown to be better than CBGA versions with tin-lead when the design and processes are optimized. LGA process should be similar to CBGA assembly

The purpose of the following aspect of the investigation was to determine the direct assembly challenge of an LGA1517 package with 1-mm pitch where both large size and heavy weight of package are of concern. It was already shown that LGAs can be converted successfully to CGA by either attachment of copper-wrapped or microspring-coiled columns. The CGA versions then can be assembled and pass a number of thermal cycles with no failures.

Assembly procedure currently recommended for smaller size and plastic version of the LGA package using only solder paste for assembly is considered to cause significant solder bridges. To avoid bridging, the LGA1517 package was first subjected to tin-lead solder paste printing in order to increase solder height as well as to provide some control on standoff during subsequent assembly onto PCB. Solder paste was printed onto package and then reflowed to achieve solder bumps. This process was successful and generated uniform solder bumps with no bridging (see Figure 33).

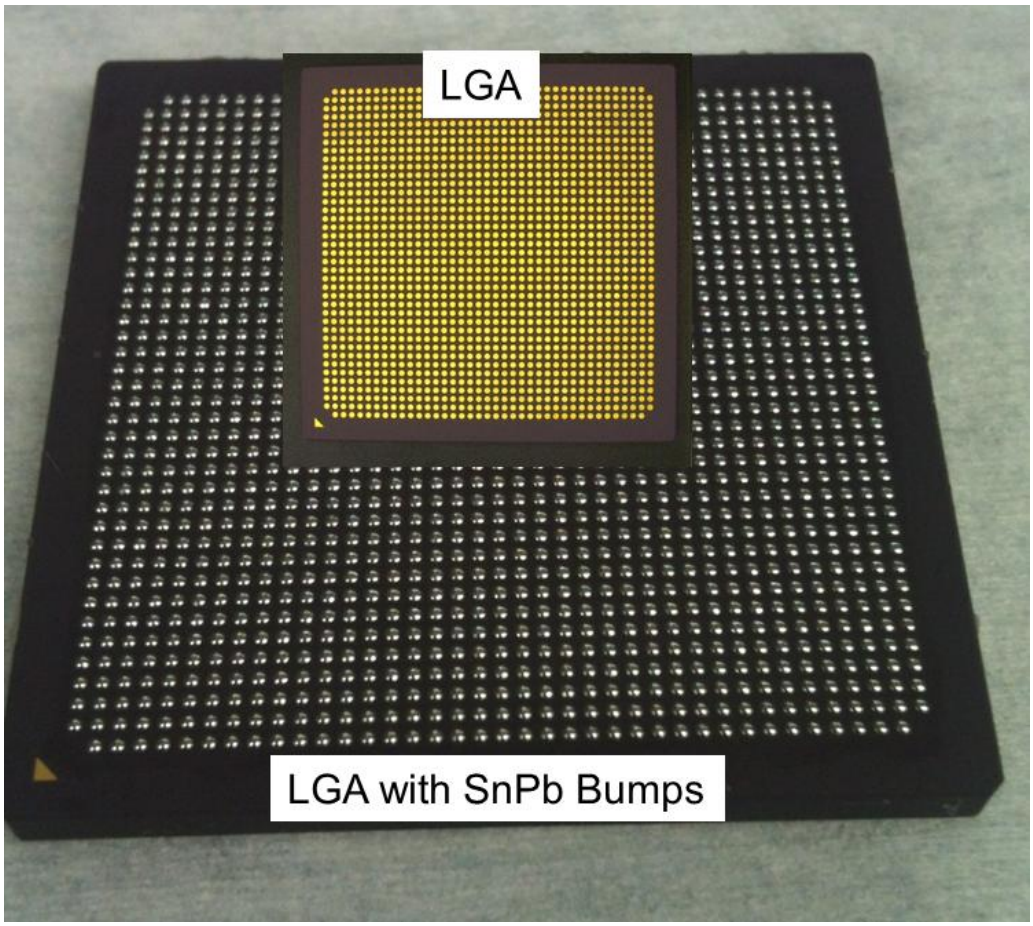

Figure 33. Ceramic land grid array (LGA) package as received (top) and with solder bumps generated by SnPb paste print and reflow (bottom).

The next step was to assemble an LGA package with newly formed solder bumps onto a PCB. Even with solder bumps on pads, collapse of package during assembly still was of concern. Additional spacing controls were added (Figure 34) on the periphery of LGA package in order to control height of assembly.

After paste print and placement of LGA by a rework station, assembly was reflowed using the process developed for CGA1517. Because of lower height, visual inspection did not reveal the condition of the peripheral solder joint. LGA assembly was subject to 2D X-ray for detecting quality of assembly, solder balls, and bridging. The overall X-ray photomicrograph of the LGA assembly is shown in Figure 35. Quality of solder joints appear to be acceptable and only one solder short was detected. The magnified photomicrograph of this short also shown in the X-ray figure.

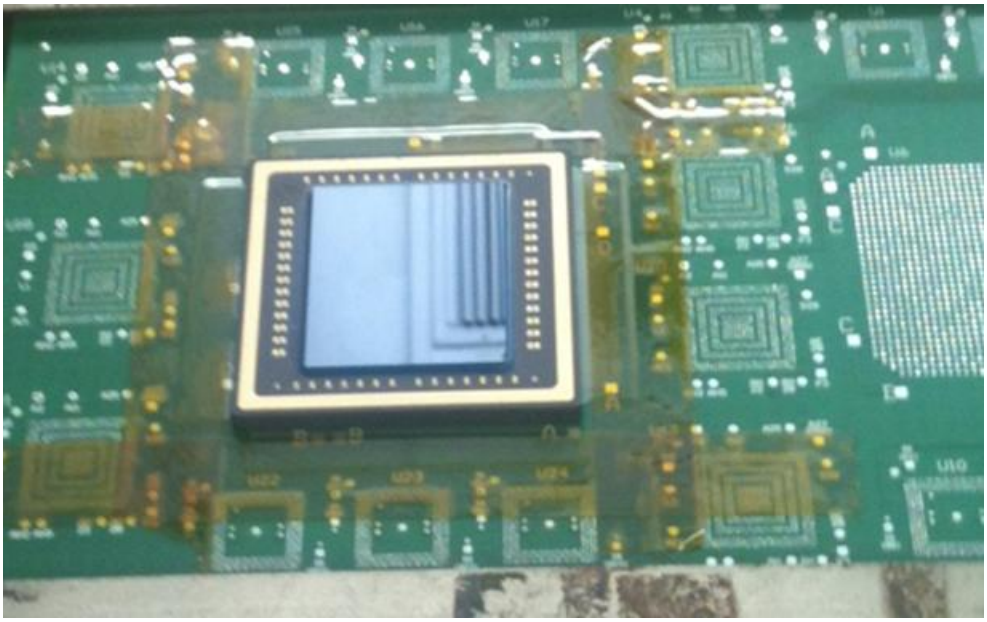

Figure 34. Ceramic land grid array (LGA) package with SnPb solder bumps assembled onto PCB.

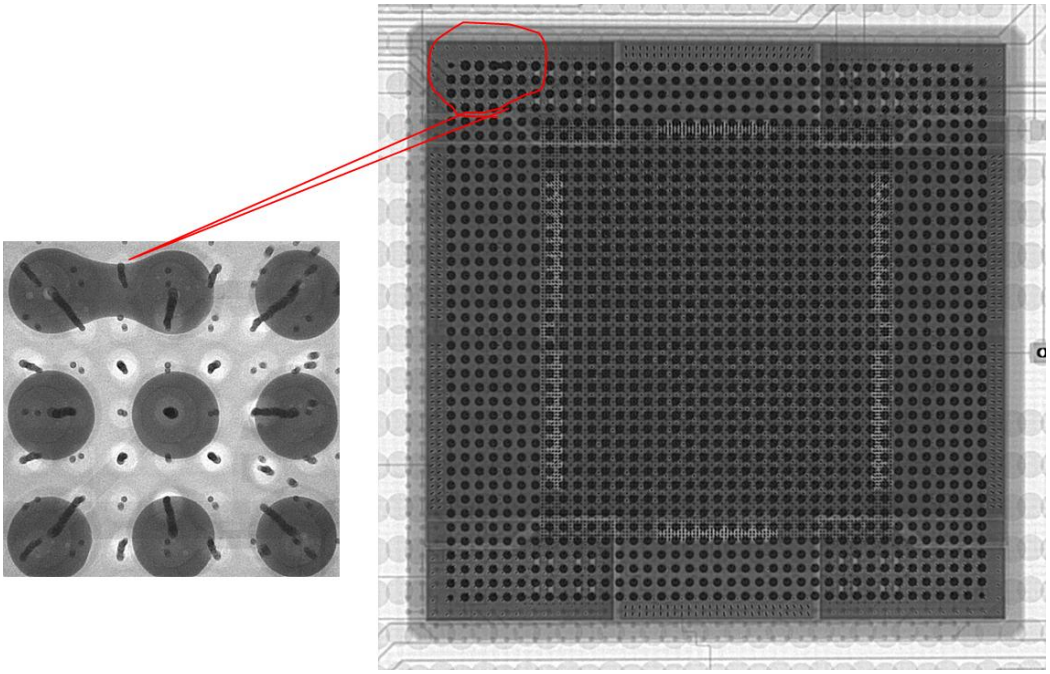

Figure 35. X-ray photomicrographs of assembled ceramic land grid array (LGA) package showing quality of assembly and one solder short.

To further verify condition of assembly and reserve the package, the assembly was subjected to removal using a rework station. Several attempts allowed removal of LGA package such that most solder bumps remain on the LGA package. The aim was to verify quality of assembly by preserving the integrity of the solder and possibly the bridge; but this goal could not be achieved because of solder melting and distortion during removal procedure, as is apparent in Figure 36. The next step is to clean solder from the LGA pads, use a new PCB, repeat processes, and include lessons learned from the first trial.

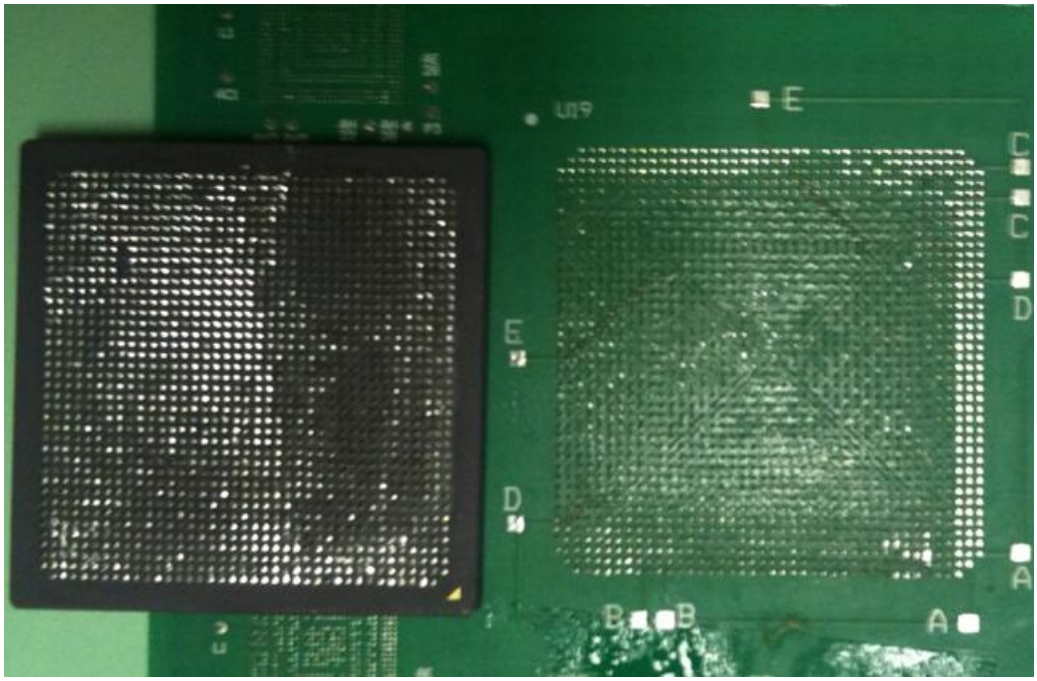

Figure 36. Rework of ceramic land grid array (LGA) package assembly show both package and PCB conditions.

6.0 STATUS RESULTS

This updated report presents preliminary test data for four CGA packages and assemblies with 1272, 1509, 1517, and 1752 inputs/outputs (I/Os), three column types (pure solder, copper-wrapped, and microspring), and 1-mm pitch. Four CGA assemblies on standard printed circuit boards were subjected to thermal cycling for quality assurance and reliability evaluation of solder joints, as well as capacitor and internal flip-chip die on package. Assemblies were subjected to two extreme profiles representative of use for high reliability applications. The thermal cycles ranged from a low temperature of –55°C to maximum temperatures of either 100°C or 125°C with slow ramp up rate of 3°C/min and dwell times of about 15 minutes at the two extremes. Optical, SEM, and X-ray inspection of assemblies were performed prior to thermal cycling to evaluate solder joint quality and workmanship defects. Subsequent inspections during thermal cycling exposures established solder damage and progress with cycling. Photomicrographs illustrate key inspection findings after up to 200 thermal cycles. Damage due to thermal cycling, evident from the photomicrographs, can be categorized as follows:

- For thermal cycle profile of –55°/100°C, CGA1272 with Cu spiral column showed good solder joint uniformity and wetting, with concave solder surrounding columns. Minimum solder damage was detected due to 100 thermal cycles that slightly increased at 200 cycles (–55/100°C); solder/columns showed signs of graininess representing tin-lead solder grain growth due to exposure at 100°C during thermal cycling. Column distortions were minimal, except for graininess of solder exposed between the Cu wrap at 200 thermal cycles. In addition, no apparent column shifts due to shear-induced deformation because of mismatch CTE of CGA and PCB were observed during thermal cycling.
- For thermal cycle profile of –55°/100°C, CGA1752 with high lead solid-solder columns showed partial solder joint coverage of column perimeter with good wetting on the coverage area. Several displaced columns showing a larger corner column shift were apparent. Some column distortions were observed with signs of graininess of solder joints at 200 thermal cycles. In addition, slight apparent column shifts due to shear-induced deformation due to CGA/PCB CTE mismatches were observed during thermal cycling.
- For thermal cycle profile of –55°/125°C, CGA1272 with Cu-spiral column showed good solder joint uniformity and wetting. Some solder damage at 200 cycles was observed showing signs of graininess representing tin-lead solder grain growth due to exposure at 125°C during thermal cycling. Column distortions were minimal, except for signs of graininess of solder between Cu wrap at 200 thermal cycles, with no apparent column shifts due to thermal cycling.
- For thermal cycle profile of –55°/125°C, GA1752 with high lead solder column showed partial solder joint coverage of column perimeter and good wetting on the coverage area. Several displaced columns showing a larger corner column shift are apparent. Magnified photomicrographs of corner columns clearly showed signs of damage and even microcrack formation. Damage is much more severe when compared to previous thermal cycle condition with 100°C maximum TC profile.

For both thermal cycle conditions (–55°/100°C and –55°/125°C), less deformation occurred for CGA1272 with smaller package dimension and higher rigidity of columns—both factors cause lower thermal stresses on solder joint attachment—compared to larger CGA1752 package and lower rigid pure solder columns. Note also that solder damage and microcracks induced especially for CGA1752 were generally significantly higher for the –55°/125°C thermal cycle profile than those under the –55°/100°C cycling condition.

The test plan matrix clearly documented key variables for advanced and extremely large ceramic area array packages both LGA and CGA styles. It was demonstrated that LGAs can be converted to CGAs using different column types: solder columns with copper wrapping or microspring coils with no solder columns. It also was shown that the CGA versions of LGA packages can be assembled onto PCBs if the

PCB pad design and other processing parameters are appropriately optimized for the type/size of package and column. Extremely large/thick CGA packages with 1752 I/O were successfully assembled onto PCBs. Thermal cycling reliability is a key issue that was addressed for four types of CGA package assemblies and the BME chip capacitors. Even though signs of damage and microcracks were detected, no failures of CGA assemblies up to 200 thermal cycles (–55°/100°C, –55°/125°C) were observed. Further reliability evaluation is currently underway and will be included in the final report for both conventional and HDI PCBs.

7.0 ACRONYMS AND ABBREVIATIONS

3D	three dimensional
BGA	ball grid array
BME	base metal electrode
CBGA	ceramic ball grid array
CCGA	ceramic column grid array
CGA	column grid array
COTS	commercial-off-the-shelf
CQFP	ceramic quad flat pack
CSP	chip scale (size) package
CTE	coefficient of thermal expansion
Cu	copper
DOE	design of experiment
EDX/EDS	energy dispersive x-ray
FPGA	field programmable gate array
FCBGA	flip-chip ball grid array
HASL	hot-air solder leveling
HCTE	high coefficient of thermal expansion
HDI	high density interconnect
I/O	input/output
JPL	Jet Propulsion Laboratory
LGA	land grid array
MIP	mandatory inspection point
NASA	National Aeronautics and Space Administration
NEPP	NASA Electronic Parts and Packaging
PBGA	plastic ball grid array
PCB	printed circuit board
PME	precision metal electrode
PWB	printed wiring board
QA	quality assurance
QFP	quad flat pack
ROHS	restriction of hazardous substances
SEM	scanning electron microscopy
SMT	surface mount
Tg	glass transition temperature
TV	test vehicle

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