The Evaluation of Combinatorial Logic and Routing Affects to Single Event Transient (SET) Propagation in the Actel RTAXs FPGA

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Motivation

- **Regarding the combinatorial logic (RTAXs: C-CELL) contribution to Single Event Effects(SEEs), a significant amount of research concentrates on C-CELLs as if they have linear effects**
- **This suggests that the Single Event Upset (SEU) cross-section can be calculated by:**

$$nP_{R-CELL} + kP_{C-CELL}$$

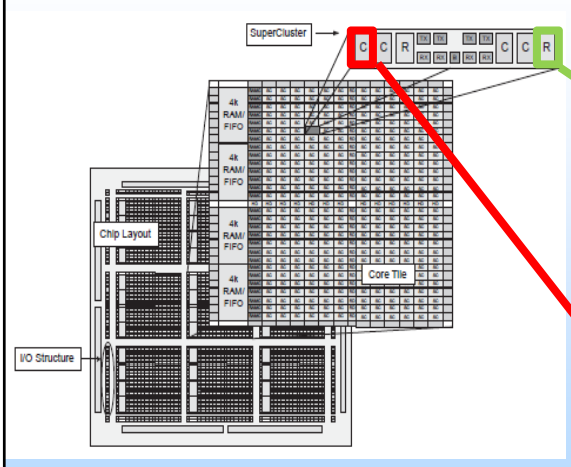
Upset Probability from flip-flops (R-Cells) ***Upset Probability from C-Cells***

- **However – this equation is not applicable to real circuits:**
  - **C-CELL SEU effects have been shown to be non-linear**
    M. Berg et. Al. "SEU Analysis of Complex Circuits Implemented in Actel RTAX-S Field Programmable Gate Array (FPGA) Devices", IEEE RADECS 2010, Langenfeld, Austria
  - **Consideration should be given to how placement and routing of cells affect SEUs**

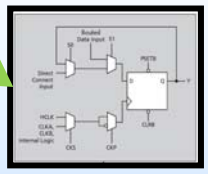
Abstract

- The intent of this presentation is to demonstrate the non-linear effects that RTAXs C-CELLs and their routing have on SEU cross-sections
- Analysis is pertinent to all configuration-hardened FPGA types and ASICs

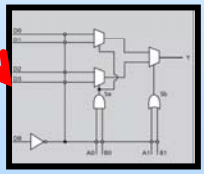
RTAXs FPGA Core Logic



R-CELL: Sequential + Combinatorial



C-CELL: Combinatorial



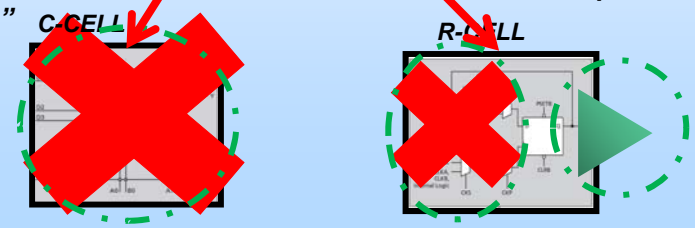
Combinatorial Logic is susceptible to Single Event Transients (SETs)
(RCELLs & CCELLs are susceptible to SETs)

Do You Believe that C-CELLs Are Significantly Responsible for SETs?

Quotes from: "SEE Characterization of the New RTAX-DSP RTAX-D Antifuse-Based FPGA", http://www.actel.com/documents/TNS10_IEEE_SR_R1.pdf

"The first published data, with the clock frequency ranging from 150MHz [3], attributed the frequency-dependent SET-induce errors to ion-strikes on C-CELLs." *Referencing work from NASA REAG*

"However, further beam tests by Actel radiation group[4] and confirmed later by The Aerospace Corporation radiation group [5] showed that most of these errors are actually originating from ion-strikes on the R-CELLs. Detailed analysis indicates the sensitive element to be the output buffer of the R-CELL[4]."



C-CELL or R-CELL Susceptibility. Why Do We Care?

- **There's many ways to create a function. Designers told the wrong thing will make the wrong assumptions.**
- **The significance of C-CELL versus R-CELL contributions to SEU cross-sections drives design choices**
- **For instance: Do you think that your Error Detection and Correct Circuitry (EDAC) which is purely non-redundant combinatorial logic can incur an upset?**
  - **It can…We tested it with heavy ions! CCELLs are susceptible**
  - **Upset rate is low because RTAXs is a robust device**
- **How does REAG handle the analysis of C-CELLs versus R-CELLs?**

Model then Test

NASA REAG FPGA Susceptibility Model

M. Berg Selection of Integrated Circuits for Space Systems IEEE NSREC 2009 Short Course, Quebec City, CN

$$P(fs)_{error} \propto P_{Configuraton} + P_{functionaLogic} + P_{SEFI}$$

Design Specific SEE upset rate — *Configuration SEE upset rate* — *Functional logic SEE upset rate* — *Single Event functional Interrupt*

$$P_{DFFSEU} + P(fs)_{SET \rightarrow SEU}$$

DFF Upset Rate — *Combinatorial logic upset Rate*

$$\sum_{i=1}^{\#CCELLs} P_{gen(i)} P_{prop(i)} \tau_{width(i)} fs$$

$P(fs)_{SET \rightarrow SEU}$ is based on:

- Number of combinatorial logic gates (*#CCELLs*)
- SET Generation (P_{gen})
- SET Propagation (P_{prop})
- Width of SET (width)
- Clock Frequency (*fs*)

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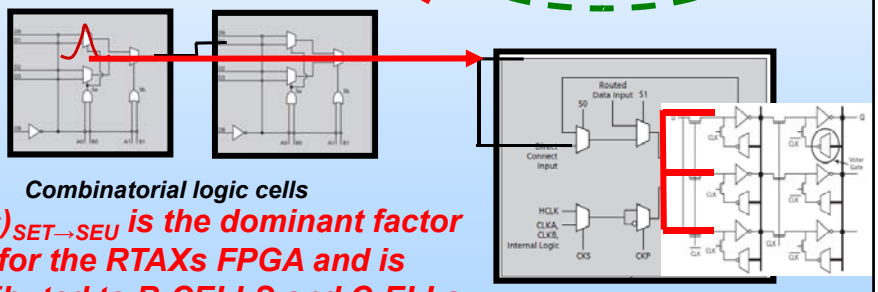
Model Application to RTAXs

M. Berg Selection of Integrated Circuits for Space Systems IEEE NSREC 2009 Short Course, Quebec City, CN

$$P(fs)_{error} \propto P_{Configuraton} + P_{functionaLogic} + P_{SEFI}$$

Design Specific SEE upset rate — *Configuration SEE upset rate* — *Functional logic SEE upset rate* — *Single Event functional Interrupt*

$$P_{DFFSEU} + P(fs)_{SET \rightarrow SEU}$$



Combinatorial logic cells

DFF

$P(fs)_{SET \rightarrow SEU}$ is the dominant factor for the RTAXs FPGA and is attributed to R-CELLS and C-ELLs

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The Dominance of $P(fs)_{SET \rightarrow SEU}$ from The NASA REAG Perspective

- Combinatorial gates are susceptible to ionizing particles and can generate SETs
- Increasing the number of combinatorial logic gates provides additional vehicles that can generate SETs

$$P_{SET \rightarrow SEU} \propto \sum_{i=1}^{\#CCELLs} P_{gen(i)} P_{prop(i)} \tau_{width(i)} fs$$

- Model allows for non-linear effects. Each C-CELL can have its own P_{gen}, P_{prop}, and τ_{width}

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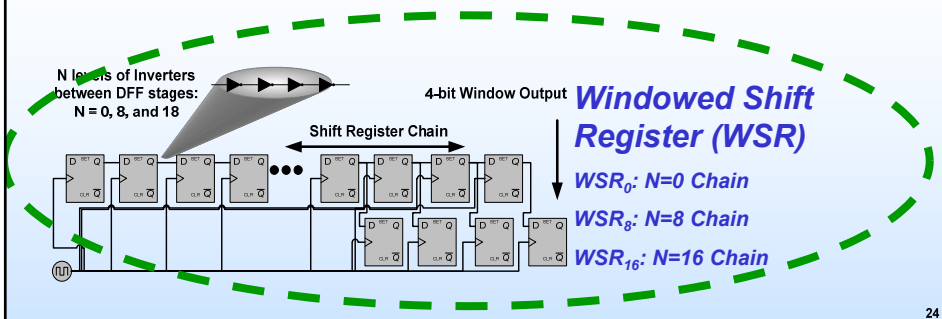
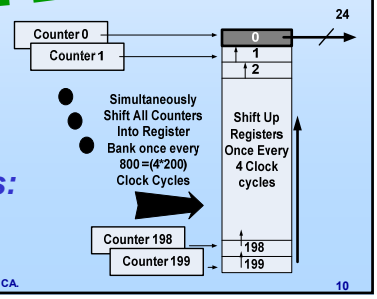
Testing C-CELL Contributions to SEU Cross-Sections





Counter Arrays:

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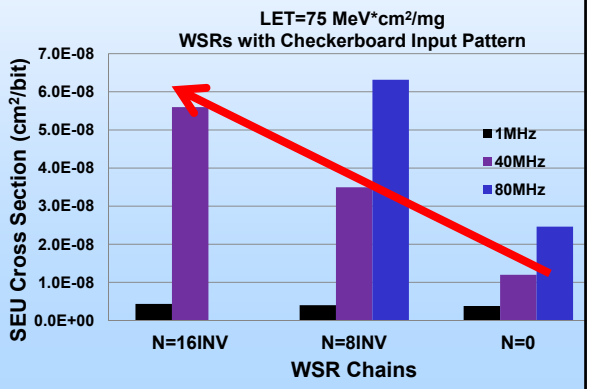
REAG's Assessment: C-Cells Significantly Contribute to SEU Cross Sections

- **High Linear Energy Transfer (LET) heavy-ion testing of WSR strings:**
  - **If most of the errors were coming from R-CELLs, WSR_0 would have the largest SEU Cross Section (it does not at high LET)**
  - **As the number of C-CELLs increases, the SEU Cross Sections increases**

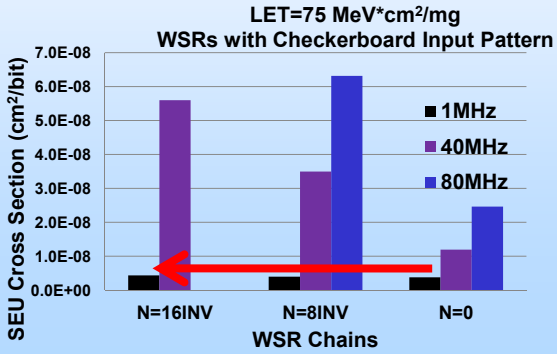
If we add C-CELLs and observe a change in SEU Cross-Section, then it follows that they have a significant contribution to SEU Cross Section



Why Not Valid Over All Frequencies?

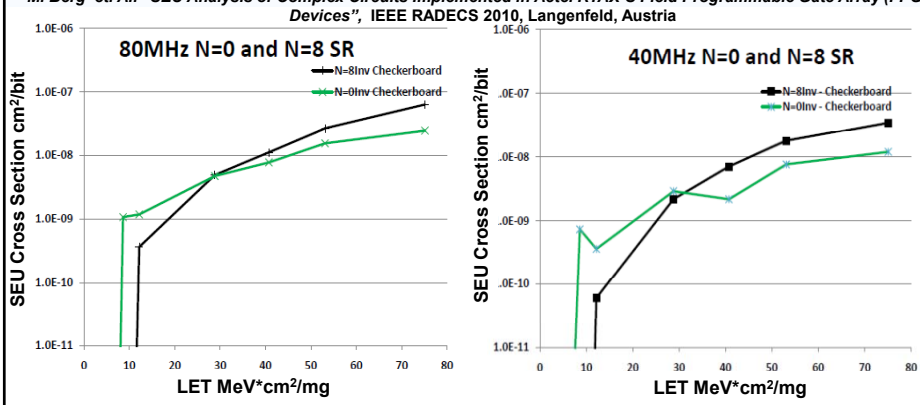
- **If *fs* is small then $P(fs)_{SET \rightarrow SEU}$ becomes insignificant**

$$P_{SET \rightarrow SEU} \propto \sum_{i=1}^{\#CCELLs} P_{gen(i)} P_{prop(i)} \tau_{width(i)} fs$$



At Low LETs SETs Can Get Attenuated

M. Berg et. Al. "SEU Analysis of Complex Circuits Implemented in Actel RTAX-S Field Programmable Gate Array (FPGA) Devices", IEEE RADECS 2010, Langenfeld, Austria



High LET: WSR_8 SEU cross-section > WSR_0 SEU cross-section

Low LET: WSR_8 SEU cross-section <WSR_0 SEU cross-section

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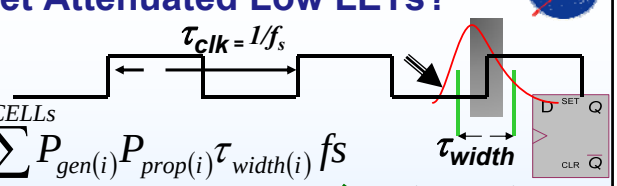
Why Do SETs Get Attenuated Low LETs?



$$P(fs)_{SET \to SEU} \propto \sum_{i=1}^{\#CCELLs} P_{gen(i)} P_{prop(i)} \tau_{width(i)} fs$$

$$\left(\frac{\tau_{width(i)}}{\tau_{clk}} \right)$$

Source: M. Berg Design for Radiation Effects MAPLD 2008 Annapolis, MD

- **Each CCELL has a P_{gen} that can create a SET with τ_{width}**
- **The question is: Can this SET reach its destination DFF without getting attenuated?**
  - **Low LET produces smaller SETs → τ_{width} is smaller → $P(fs)_{SET \to SEU}$ probability of capture is lower**
  - **In addition, at Low LET P_{prop} is reduced**
- **High LET SETs have enough energy to reach destination DFF**

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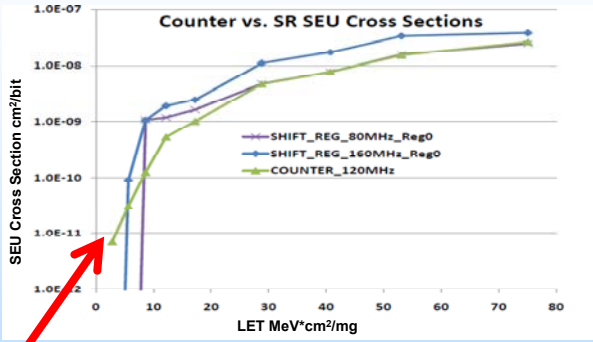
However $P(fs)_{SET \rightarrow SEU}$ from C-CELLs are still Significant for Designs with Fan-in and Fan-out >1

M. Berg et. Al. "SEU Analysis of Complex Circuits Implemented in Actel RTAX-S Field Programmable Gate Array (FPGA) Devices", IEEE RADECS 2010, Langenfeld, Austria



- *Counters tested have fan-in and fan-out >1*
- *Now multiple paths can produce a SET that can reach the destination DFF*
- *Counters have a lower LET Threshold (LET_{TH}) than WSR strings*

Evaluating linear circuits (fan-in=fan-out=1) such as shift registers can limit analysis

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Routing: Further Investigation into the Significance of $P(fs)_{SET \rightarrow SEU}$

- **Routing also can affect propagation and $P(fs)_{SET \rightarrow SEU}$. How should we test?**
- **Start with implementing WSR chains in two separate FPGAs.**
- **Routing is forced to be different between the FPGAs**

A-series FPGA	B-Series FPGA
5 separate WSR chains	3 separate WSR Chains
N=0, 2, 4,8, and 16	N=0, 8, and 16

- **WSR chains with equivalent N differ only in place and route**
- **Analyze at higher LET and higher frequencies so that other attenuation effects do not disrupt evaluation**

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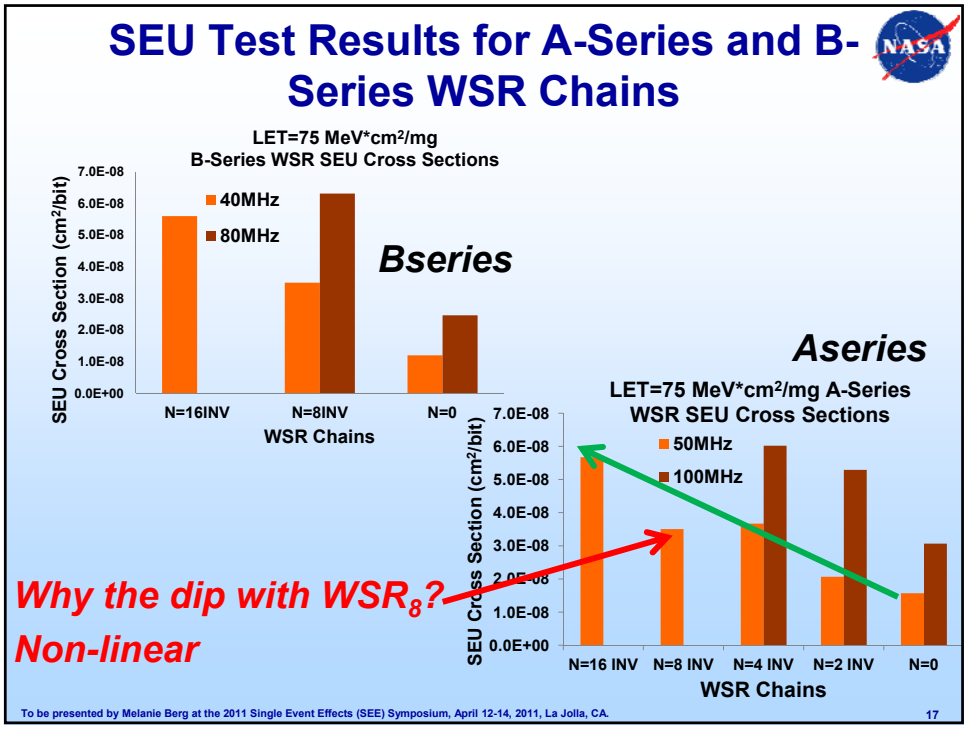
SEU Test Results for A-Series and B-Series WSR Chains
LET=75 MeV*cm²/mg
B-Series WSR SEU Cross Sections
SEU Cross Section (cm²/bit)
7.0E-08
6.0E-08
5.0E-08
4.0E-08
3.0E-08
2.0E-08
1.0E-08
0.0E+00
40MHz
80MHz
Bseries
N=16INV
N=8INV
N=0
WSR Chains
Aseries
LET=75 MeV*cm²/mg A-Series
WSR SEU Cross Sections
50MHz
100MHz
N=16 INV
N=8 INV
N=4 INV
N=2 INV
N=0
Why the dip with WSR8?
Non-linear
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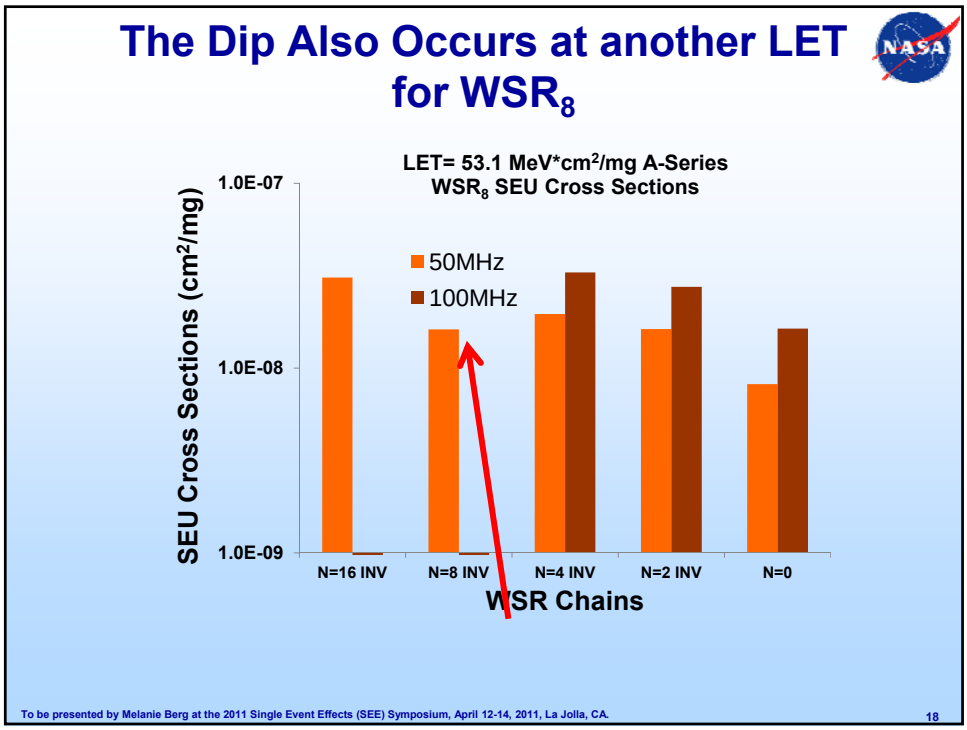
The Dip Also Occurs at another LET for WSR8
LET= 53.1 MeV*cm²/mg A-Series
WSR8 SEU Cross Sections
SEU Cross Sections (cm²/mg)
1.0E-07
1.0E-08
1.0E-09
50MHz
100MHz
N=16 INV
N=8 INV
N=4 INV
N=2 INV
N=0
WSR Chains
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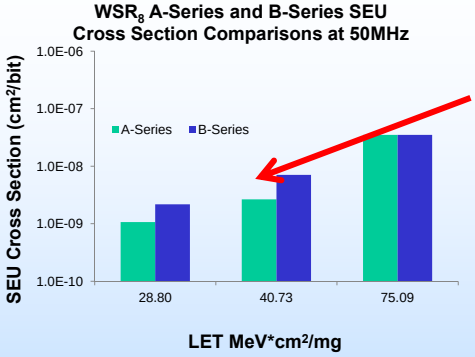
WSR_8 A-Series and B-Series Comparison



A-Series SEU cross-section drops off more than B-Series as LET decreases

- **Engineering 101 dictates:**
  - **As route length increases, its net capacitance increases**
  - **A signal propagating through a long route can incur attenuation**
- **Does the A-Series have longer routes – i.e. are its SETs getting attenuated due to routing?**

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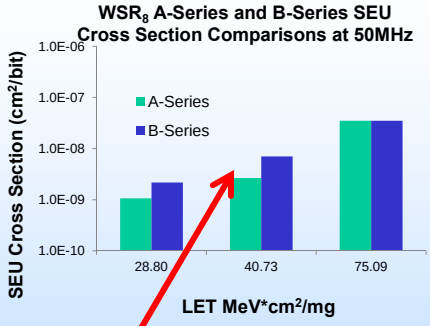
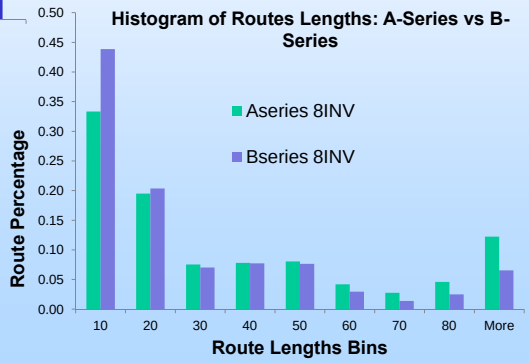
Low and Behold: A-Series WSR_8 Does have A Higher Percentage of Long Routes



This is why A-Series has a greater drop off than B-Series



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Conclusion

- We have proven that attenuation from C-CELLs and their routes can affect P_{prop} and hence $P(fs)_{SET \rightarrow SEU}$
- This is a non-linear effect
  - Each C-CELL and its route will contribute differently based on
    - Length of route
    - C-CELL configuration
    - C-CELL state
    - C-CELL loading capacitance
  - Cannot calculate for one C-CELL and then multiply by the number of C-CELLs in a chain of logic
  - Cannot extrapolate – must test and analyze for all instances

Cannot evaluate a C-CELL alone. Its routing must also be considered