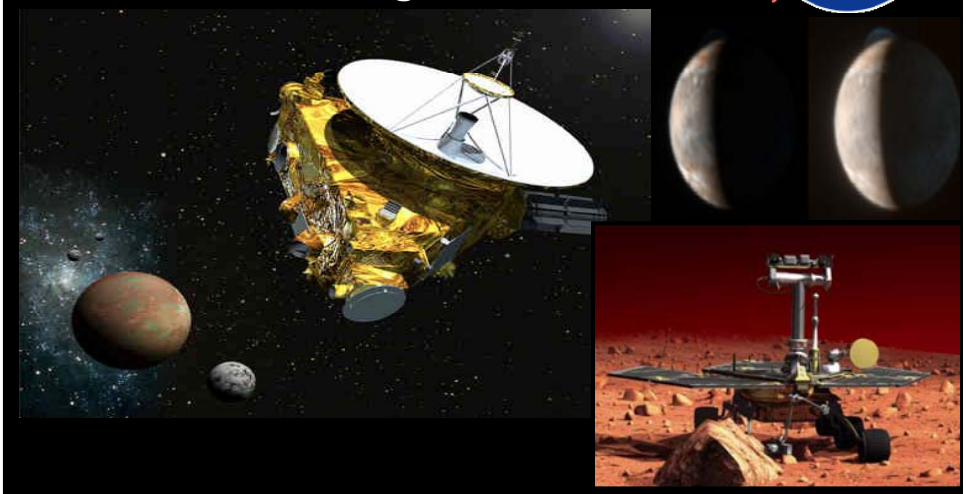
Characterizing Data Path Single Event Upsets in a Synchronous Design



Melanie Berg, MEI Technologies in support of NASA/GSFC

Acknowledgements

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- *Thanks is given to the NASA Goddard Radiation Effects and Analysis Group (REAG) for their technical assistance and support. REAG is led by Kenneth LaBel and Jonathan Pellish*

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Before we get started… here are some things to keep in mind during this presentation

Single Event Effects (SEEs) and Common Terminology

- Single Event Latch Up (SEL): Device latches in high current state
- Single Event Burnout (SEB): Device draws high current and burns out
- Single Event Gate Rupture: (SEGR): Gate destroyed typically in power MOSFETs
- Single Event Transient (SET): current spike due to ionization. Dissipates through bulk
- Single Event Upset (SEU): transient is caught by a memory element. Causes an incorrect state. SETs are categorized under SEUs
- Single Event Functional Interrupt (SEFI) - upset disrupts function

FPGA SEU Susceptibility

- **FPGA SEUs or SETs can occur in:**
  - **Configuration**
  - **Combinatorial Logic (CL)… including global routes or control**
  - **Sequential Logic**
  - **Memory Cells**
  - **Hidden logic (SEFI)**

Every Device has different Error Responses – We must understand the differences and design (or plan) accordingly

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FPGA SEU Cross Section (σ_{SEU}) Categorization as defined by NASA Goddard REAG:

$$P(fs)_{error} \propto P_{Configuration} + P(fs)_{functionalLogic} + P_{SEFI}$$

Design σ_{SEU} ***Configuration σ_{SEU}*** ***Functional logic σ_{SEU}*** ***SEFI σ_{SEU}***

Sequential and Combinatorial logic (CL) in data path

Global Routes and Hidden Logic

SEU Testing is required in order to characterize the σ_{SEU} for each of FPGA categories

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σ_{SEU}s and Error Rates – How We Apply Them to FPGAs

- A goal of FPGA SEU testing is to provide error rate (*dE(fs)/dt*) predictions to critical missions
- Depending on the FPGA type, calculations are performed with respect to flip-flops (DFFs) or configuration memory bits
- *dE(fs)/dt* for FPGA devices are calculated using :

System upset rate — SEU bit upset — Number of used Bits

$$\frac{dE(fs)}{dt} < \frac{dE_{bit}(fs)}{dt} * (\#UsedBits)$$

This presentation will focus solely on $dE_{bit}(fs)/dt$ for bits that are in a functional data path (DFFs) of a synchronous design: $P(fs)_{functionalLogic}$

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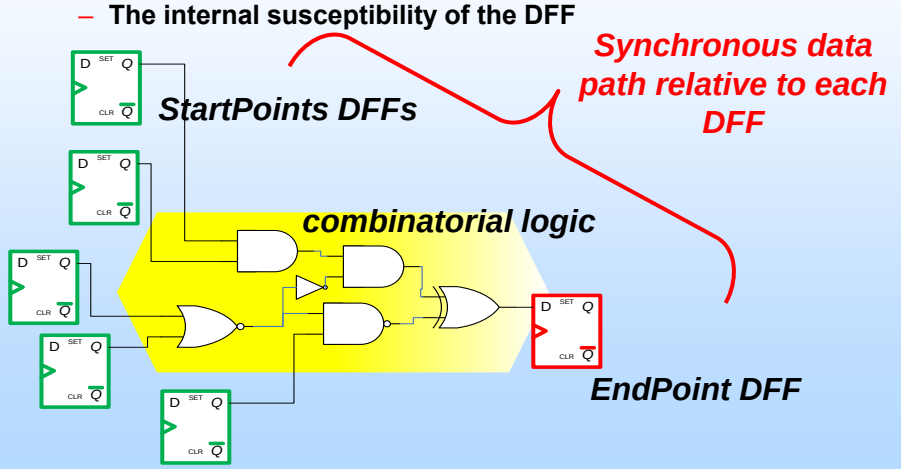
Probability that an FPGA will flip its state ($dE_{bit}(fs)/dt$)

- The probability that a DFF will flip its state is based on
  - Logic that feeds into the DFF input pin
  - The internal susceptibility of the DFF



StartPoints DFFs and combinatorial logic → EndPoint DFF

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Agenda

- **Section I: Synchronous Design Concepts**
- **Section II: SEU and SET Generation in Data Path DFFs and Combinatorial Logic**
- **Section III: System capture of generated data path SEUs**
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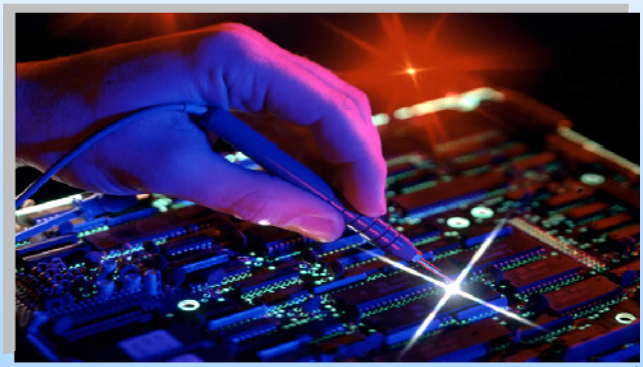
SEU Characterization of a Synchronous Data Path

$$P(fs)_{error} \propto P_{Configurat\ ion} + P(fs)_{functional\ Logic} + P_{SEFI}$$



Synchronous Design Methodology and SEU Modeling

- **Design topology dictates SEU susceptibility**
  - Edge triggered Flip flops (DFFs) versus latches
  - Logic cells: Sea of gates versus look up tables (LUTs)
  - High capacitive routing
  - Large fan-out or large fan-in or feedback paths
- **Synchronous design has proven to be the most reliable means of design and is the most common design strategy used world wide**
  - Makes state transitioning deterministic
  - Provides distinct boundary points – relates state to clock cycle
  - Easiest method to verify
  - Automated design tools are geared for synchronous methodology

This presentation pertains to synchronous designs

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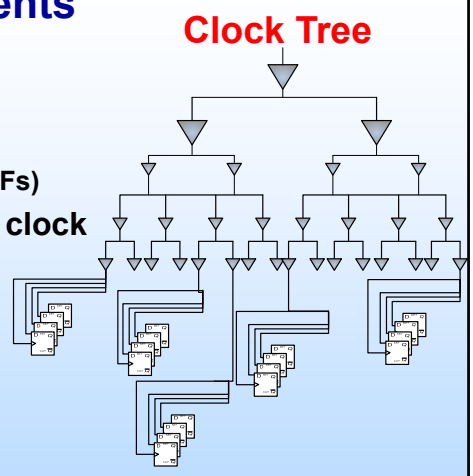
Synchronous Design Data Path Components

- **Designs are comprised of:**
  - Combinatorial Logic (CL)
  - Edge Triggered Flip-Flops (DFFs)
- **All DFFs are connected to a clock**
- **Clock period:** τ_{clk}
- **Clock frequency:** f_s



$$\tau_{clk} = \frac{1}{fs}$$

The premise of synchronous design is to compute and hold in a deterministic manor

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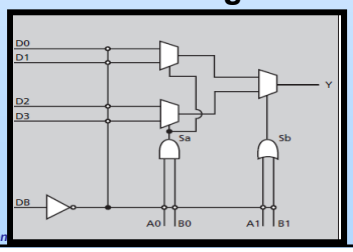
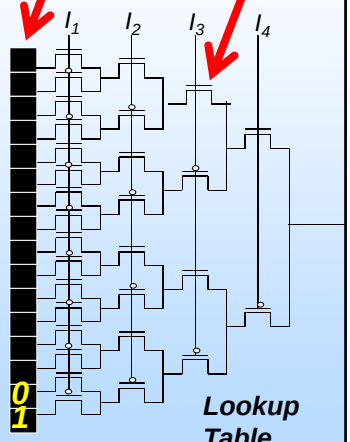
Combinatorial Logic: Data Path Computation

- Output is affected by inputs after gate delay
- Used for computing or routing
- FPGAs provide blocks of combinatorial logic (library components)… blocks vary per manufacturer
- Combinatorial Loops are not allowed in synchronous design

Microsemi RTAXs C-CELL: Does not require SRAM



Xilinx Virtex LUT uses SRAM + Combinatorial



Lookup Table LUT

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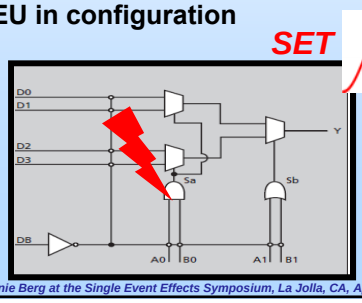
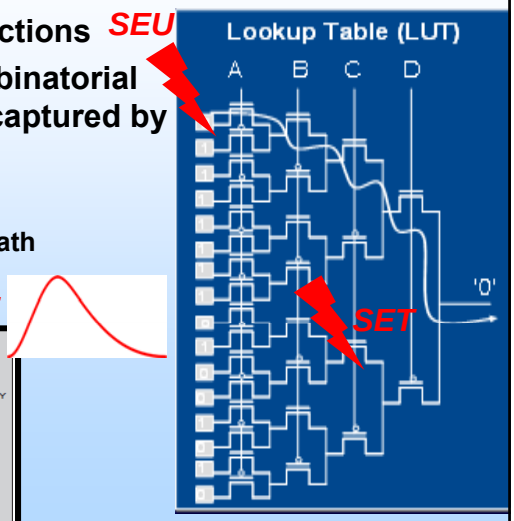
SETs and Combinatorial Logic

- SETs are double sided functions
- Because there are no combinatorial logic loops, SETs are not captured by the combinatorial path
- In SRAM based FPGAs:
  - SET in combinatorial logic path
  - SEU in configuration





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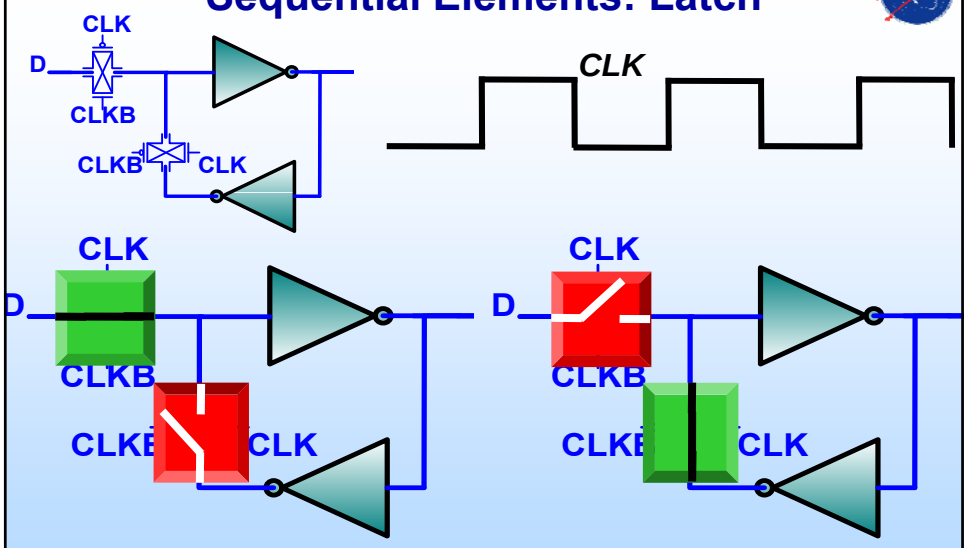
Sequential Elements: Latch



When CLK is low: Latch is in Transparency Mode

When CLK is high: Latch is in hold Mode

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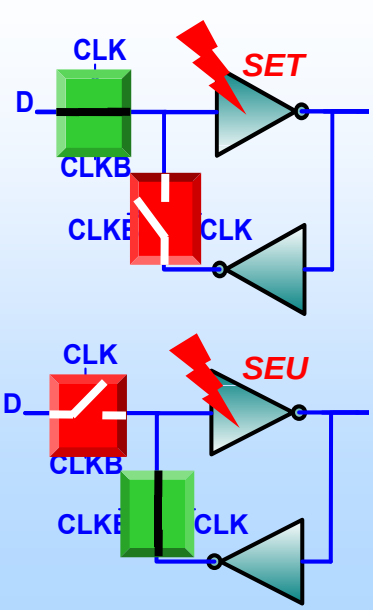
SEUs and SETs in Latch Structures



***SET** when CLK is low: Latch is transparent and is a series of combinatorial logic*

Glitch: Double Sided

***SEU** when CLK is high: Latch is in hold state and is a loop that will hold the flipped state*

Single Sided

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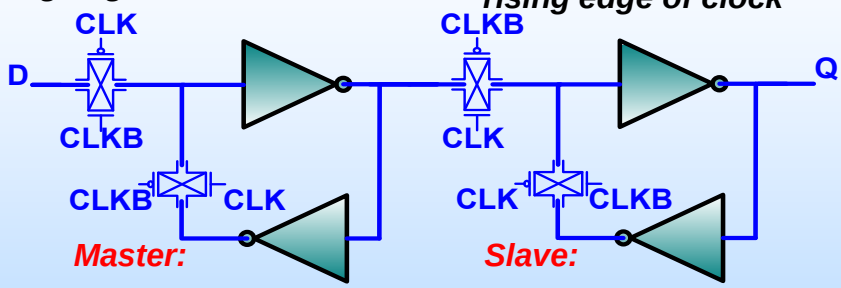
Edge Triggered Flip Flops... Creating Deterministic Boundary Points

D input must be settled by rising edge of clock

Output will only change at rising edge of clock



Master:

Clock Low: Transparent

Clock High: Hold

Slave:

Clock Low: Hold

Clock High: Transparent

*In order to create precise boundary points of state capture, **Latches** are **NOT allowed** in Synchronous designs*

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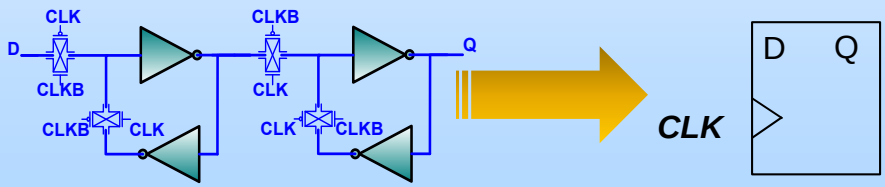
DFF SEU Generation ($P(fs)_{DFFSEU}$)

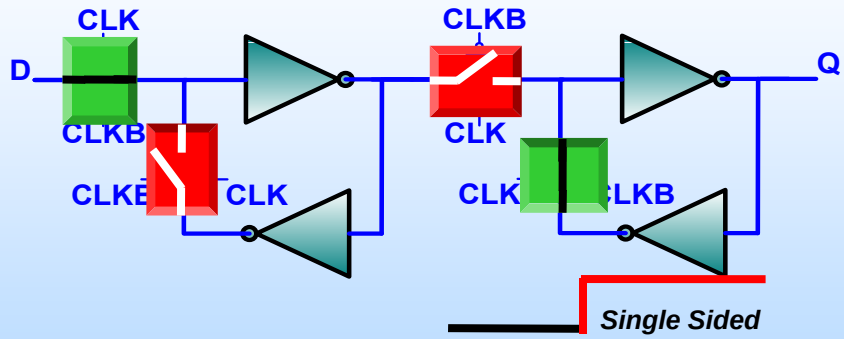
- DFF outputs define the state of the design.
- We will characterize DFF upset generation ($P(fs)_{DFFSEU}$) based on DFF output
- $P(fs)_{DFFSEU}$ can affect the system differently depending on when and where the upset is actually generated



How is the DFF's Output Affected?... Clock Low

Master is transparent and Slave is in hold.

Master is cut off from slave and an SEU can occur in the slave



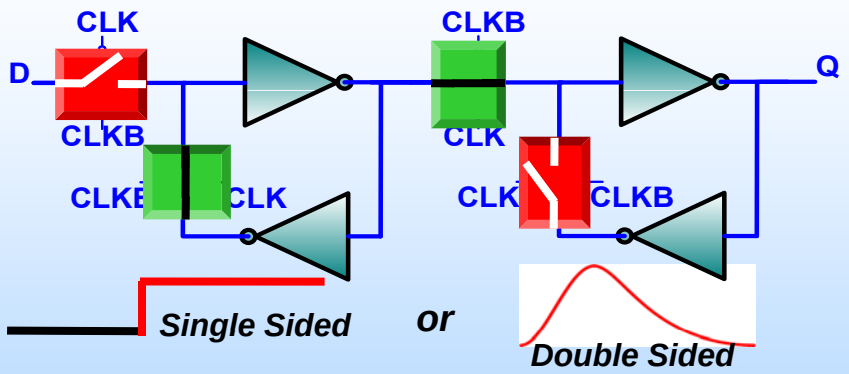
States are defined at the rising edge of clock

If a single sided upset is generated while clock is low, generation occurs during an intermediate state

Will the upset disrupt system behavior?

How are DFFs' Outputs Affected? Clock High

Master is in a hold state and Slave is transparent



States are defined at the rising edge of clock

If single sided or double sided upset is generated while clock is high, generation occurs during an intermediate state

Will the upset disrupt system behavior?

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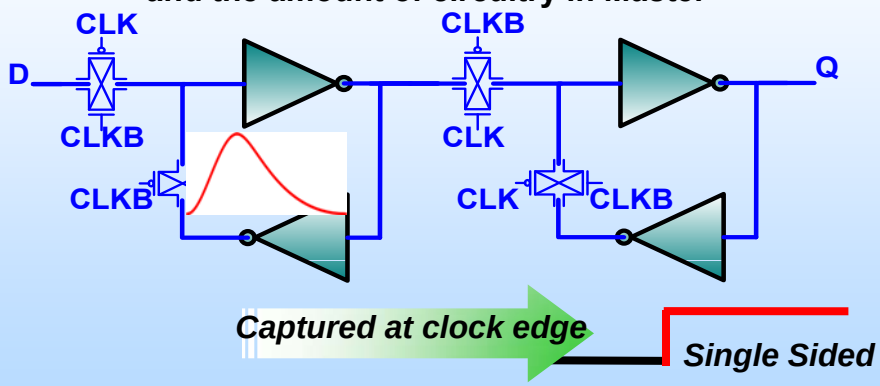
How is the DFF's Output Affected? Clock Edge… Clock Low ➔ Clock High

Master can capture an SET from its transparent state. Single sided upset at output. Depends on the frequency, SET width, and the amount of circuitry in Master



Output changes at clock edge, hence it will affect the system state

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Single Sided Upset DFF Generation

$P(fs)_{DFFSEU}$

- Single Sided upset = DFF flipped state
- Two categories relative to system state:

1. DFF flips its state at clock edge (low to high transition):
   - Master SET gets trapped during Master transition from transparent to hold state
   - This is considered a state change
   - Frequency dependent
   - $\alpha P(fs)_{DFFSEU}$: *Percentage of upsets that occur at clock edge*
2. DFF flips its state between clock edges (while clock is low or high):
   - Master or slave is in hold state
   - This is not considered a definitive state change
   - Not Frequency dependent
   - $\beta P(fs)_{DFFSEU}$: *Percentage of upsets that occur between clock edges*

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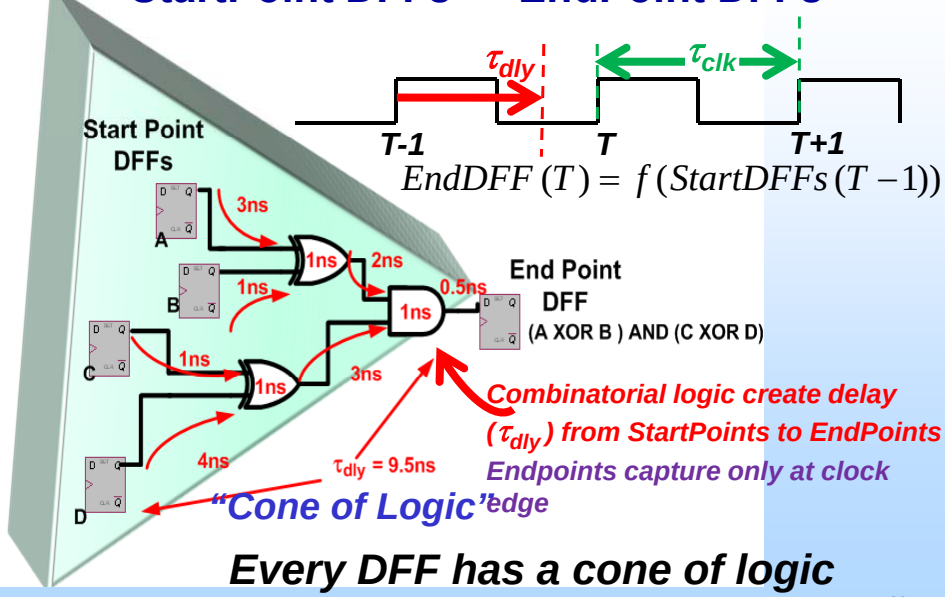
SEU Generation versus SEU Capture in Synchronous Systems

- We discussed SET generation and SEU generation
- It is not definitive that an SET or SEU will cause system upsets
- It is essential to differentiate between SEE generation versus system upset
- Clock edge upset:
  - Will be a system upset if not logically masked
- Intermediate clock edge upset:
  - Will be a system upset if it affects a DFF at the next clock edge

The question becomes, will the upset be missed or will it manifest… depends on design topology

Synchronous System Data Paths: StartPoint DFFs → EndPoint DFFs



$$EndDFF(T) = f(StartDFFs(T-1))$$

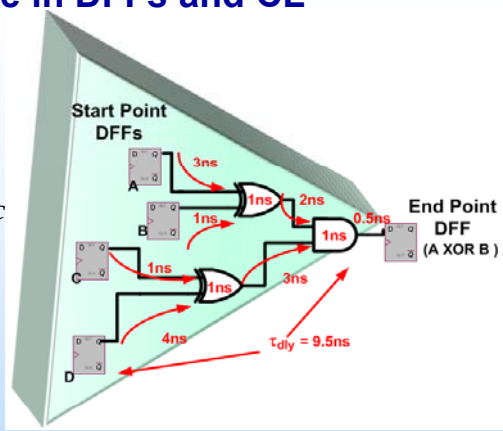
Combinatorial logic create delay (τ_{dly}) from StartPoints to EndPoints

Endpoints capture only at clock edge

Every DFF has a cone of logic

Data Path Model and DFF Logic Cones: Upsets Originate in DFFs and CL

$P(fs)_{functional\ Logic}$



Evaluate Each DFF as an EndPoint

$\exists_{DFF}$ ***EndPoint DFF SEUs + StartPoint DFF SEUs + CL SETs***

DFF_k Cone of Logic

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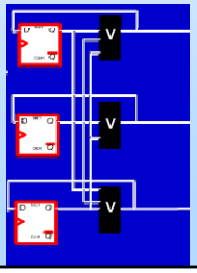
Characterizing EndPoint DFF SEU Capture:

- **EndPoint Internal SET is Generated between Clock Edges and is Captured at Clock Edge**
- **EndPoint DFF SEU Capture ($\alpha P(fs)_{DFFSEU \rightarrow SEU}$):**
  - **SEU Generation in EndPoint DFF ($P(fs)_{DFFSEU}$)**
  - **Capture is at clock edge – there is no propagation path to analyze**
  - **Logic Masking (P_{logic}) is after the EndPoint DFF**

Single Sided

EndPoint Logic Masking



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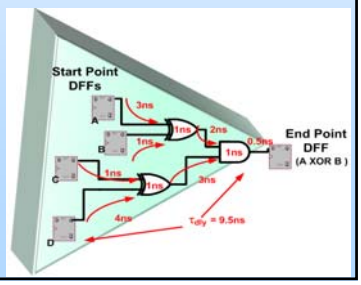
Characterizing StartPoint DFF SEU Capture:

- StartPoint SEU generation occurs between clock edges and EndPoint Capture might occur at the clock edge
- StartPoint DFF SEU Capture ($\beta P(fs)_{DFFSEU \rightarrow SEU}$):
  - SEU Generation in DFF ($\beta P(fs)_{DFFSEU}$)
  - Capture depends on path from StartPoint to EndPoint
  - Logic Masking (P_{logic}) is after the StartPoint
  - Capture:

$(1-\tau_{dly}/\tau_{clk}) = (1-\tau_{dly} fs)$

Single Sided



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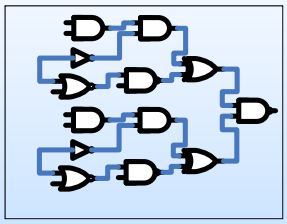
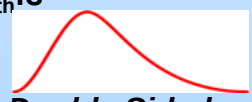
Characterizing Combinatorial Logic SET Capture

- SET Generation Occurs Between Clock Edges and Capture might Occur at Clock Edge
- CL SET Capture $P(fs)_{SET \rightarrow SEU}$:
  - SET Generation in CL (P_{gen})
  - SET Propagation strength (P_{prop})
  - Logic Masking (P_{logic})



- Capture is proportional to the SET width (τ_{width}^{CL}) and the clock period (τ_{clk}): $\tau_{width}/\tau_{clk} = \tau_{width} fs$



Double Sided

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Putting it All Together: NASA REAG FPGA Data Path Susceptibility Model

$$P(fs)_{functionalLogic}$$

$$\sum_{k=1}^{\#EndPoint\ DFFs} P_{logic(k)} * \left(\alpha P(fs)_{DFFSEU(k)} + \sum_{j=1}^{\#StartPoint\ DFFs} \left(\beta P(fs)_{DFFSEU(j)} (1 - \tau_{dly(j)} fs)) * P_{logic(j)} \right) + \sum_{i=1}^{\#CL} (P_{gen_{(i)}} * P_{prop_{(i)}} * P_{logic_{(i)}} * \tau_{width_{(i)}} fs) \right)$$

EndPoint Logic Masking

EndPoint

StartPoints

Combinatorial Logic

Details of Combinatorial Logic SET Capture

$$\exists_{DFF} \left(\sum_{i=1}^{\#Combinator\ ialCells} (P_{gen(i)} P_{prop(i)} P_{logic} \tau_{width(i)} fs) \right)$$

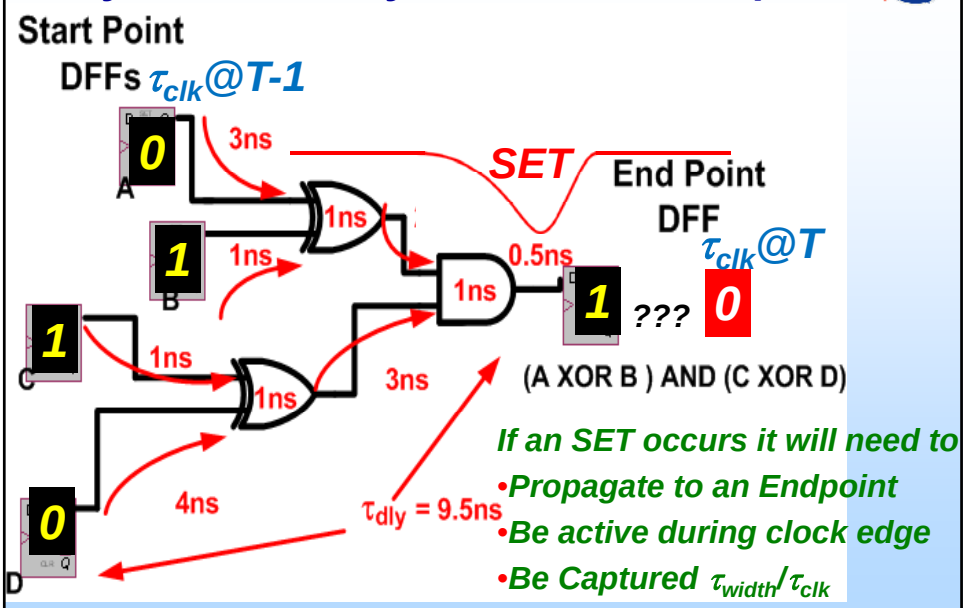
Generation

Propagation

Logic Masking

Capture

Synchronous System: CL SET Capture



If an SET occurs it will need to

- *Propagate to an Endpoint*
- *Be active during clock edge*
- *Be Captured τ_{width}/τ_{clk}*

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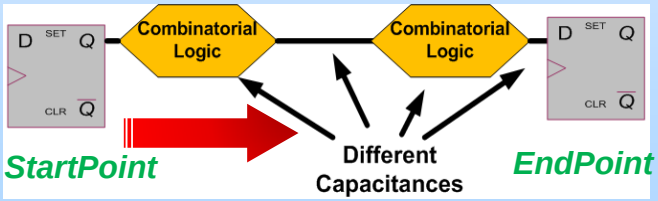
SET Propagation to an EndPoint DFF: P_{prop}

- **In order for the data path SET to become an upset, it must propagate and be captured by its Endpoint DFF**
- **P_{prop} only pertains to electrical medium (capacitance of path… combinatorial logic and routing)**
  - **Capacitive SET amplitude reshaping**
  - **Capacitive SET width reshaping**
- **Small SETs or paths with high capacitance have low P_{prop}**
- **P_{prop} contributes to the non-linearity of $P(fs)_{SET \rightarrow SEU}$ because of the variation in path capacitance**



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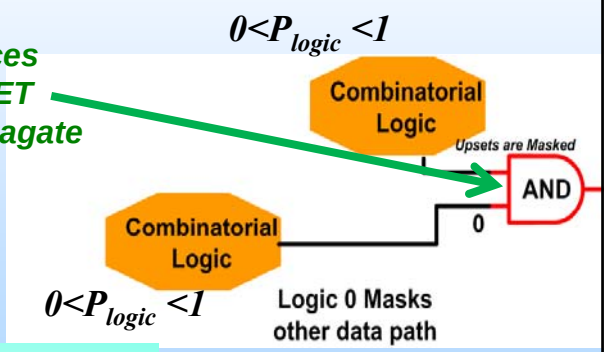
SET Logic Masking: P_{logic}

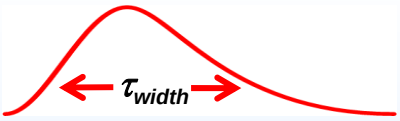
- P_{logic}: Probability that a SET can logically propagate through a cone of logic. Based on state of the combinatorial logic gates and their potential masking.

"AND" gate reduces probability that SET will logically propagate



Determining P_{logic} for a complex system can be very difficult

SET Capture at Destination DFF



The transient width (τ_{width}) will be a fraction of the clock period (τ_{clk}) for a synchronous design in a CMOS process.

$$P(\tau_{clk})_{SET \to SEU} \propto \frac{\tau_{width}}{\tau_{clk}}$$

$$P(fs)_{SET \to SEU} \propto \tau_{width} fs$$

Probability of capture is proportional to the width of the transient as seen from the destination DFF

Details of Capturing StartPoint DFFs

$$\exists_{DFF}\left(\left(\sum_{j=1}^{\#StartPoint\,DFFs} \beta P(fs)_{DFFSEU(j)}(1-\tau_{dly(j)}fs)P_{logic(j)}\right)\right)$$

Generation

Capture

Logic Masking

Generation $P(fs)_{DFFSEU}$ versus Capture $P(fs)_{DFFSEU \rightarrow SEU}$

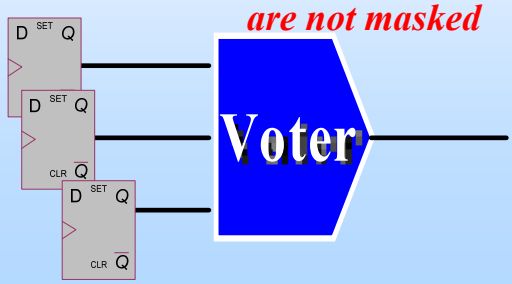
$\alpha P(fs)_{DFFSEU}$	$\beta P(fs)_{DFFSEU}$	$P(fs)_{DFFSEU \rightarrow SEU}$
Probability an SEU is generated in an EndPoint	Probability an SEU is generated in a StartPoint	Probability that the StartPoint or Endpoint upset will be captured by the system
Occurs at clock edge	Occurs between clock edges	Occurs at a clock edge (capture)
Frequency dependent	Not frequency dependent	Frequency dependent

Logic Masking DFFs… P_{logic}

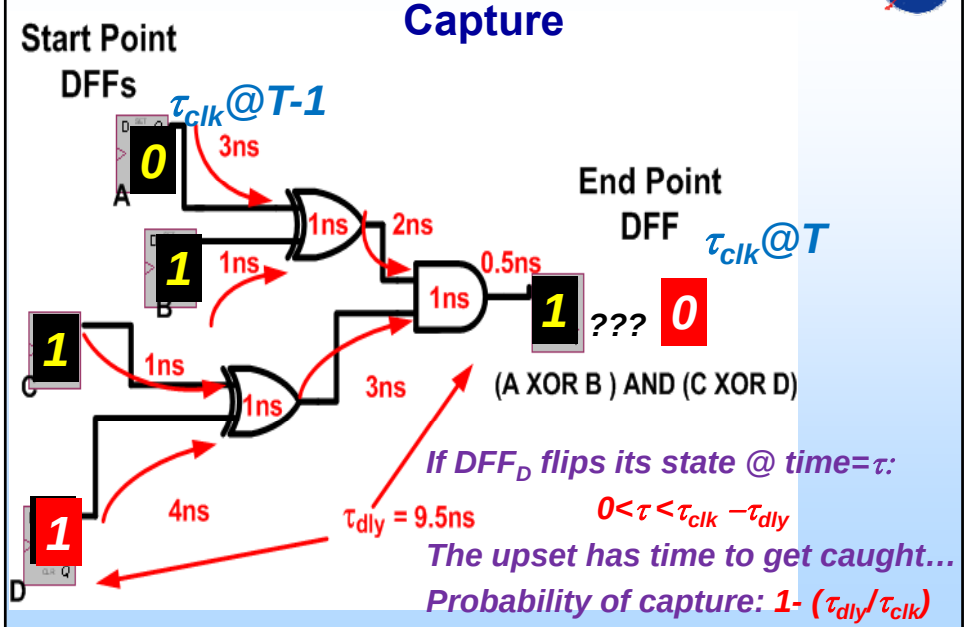
- Logic masking for DFFs is similar to logic masking of combinatorial logic.
- DFF logic masking is generally the point where Triple Modular Redundancy (TMR) is inserted

P_{logic}=0 for DFFs… their upsets are masked

P_{logic}>0 for Voter… its upsets are not masked



Synchronous System: StartPoint SEU Capture



Percentage of Clock Cycle for SEU Capture:

$$\tau < \tau_{clk} - \tau_{dly}$$

Upset is caught within this timeframe

$$\frac{\tau}{\tau_{clk}} < \frac{\tau_{clk} - \tau_{dly}}{\tau_{clk}} = 1 - \frac{\tau_{dly}}{\tau_{clk}}$$

Fraction of clock period for upset capture

$$\tau \ fs < 1 - \tau_{dly} \ fs$$

upset capture with respect to to frequency

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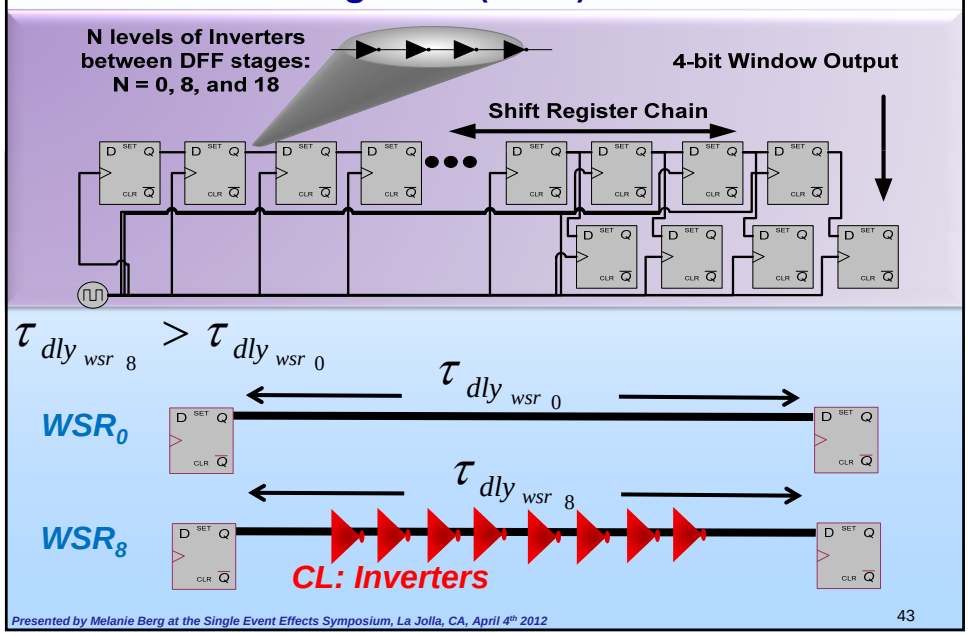
- **Section IV: FPGA SEU Model and Radiation Data Evaluation**

Radiation Test Structures: Windowed Shift Registers (WSR)



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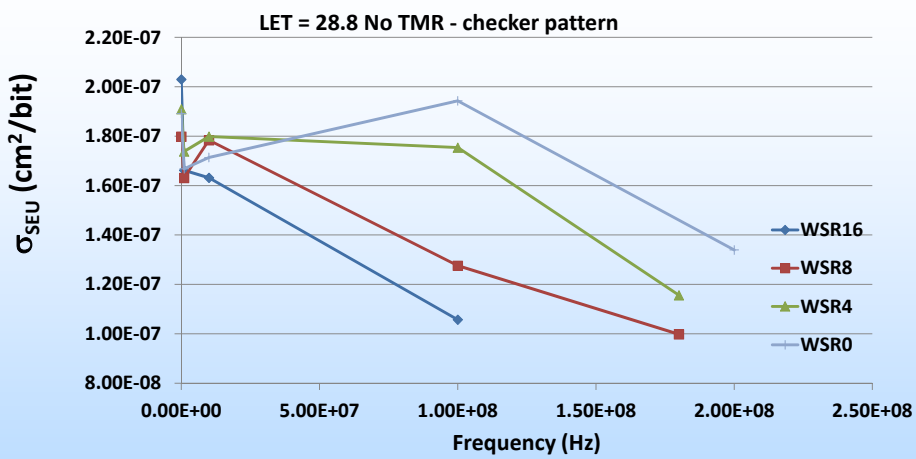
WSR σ_{SEU} across Frequency



Shift Register: P_{logic} = 1 Everywhere; and StartPoint = 1 for each EndPoint

$$\sum_{k=1}^{\#EndPoint\ DFFs} \left(\alpha P(fs)_{DFFSEU(k)} + \beta P(fs)_{DFFSEU(J)} (1 - \tau_{dly(j)} fs) \right)$$

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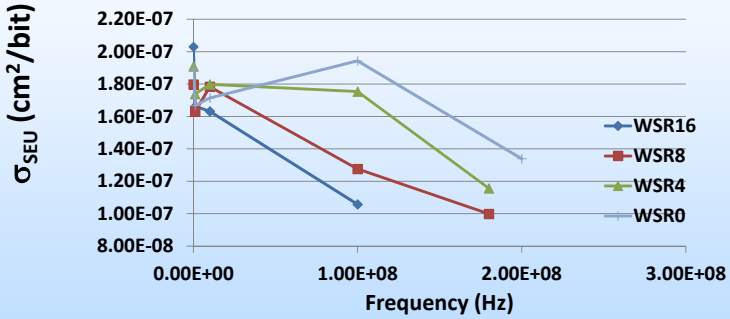
System σ_{SEU} Response at Lower Frequencies

$$\sum_{k=1}^{\#EndPoint\ DFFs} \left(\alpha P(fs)_{DFFSEU(k)} + \beta P(fs)_{DFFSEU(j)} (1 - \tau_{dly(j)} fs) \right)$$

LET = 28.8 No TMR - checker pattern



- ***A large percentage of StartPoint DFF upsets can reach EndPoints ((1-τ_{dly}fs)➔1)***
- ***In this frequency range, the σ_{SEU} drop is not dominant and is therefore not observable***

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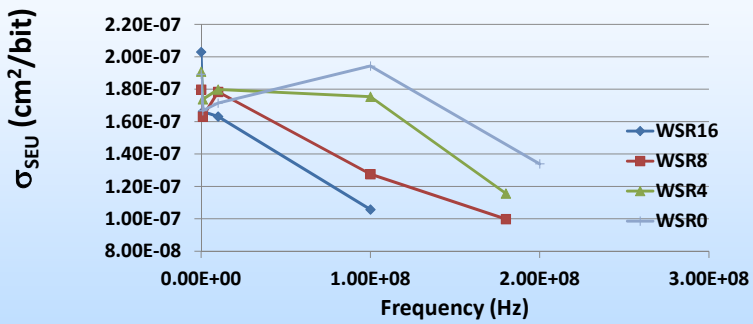
System σ_{SEU} Response at Higher Frequencies

$$\sum_{k=1}^{\#EndPoint\ DFFs} \left(\alpha P(fs)_{DFFSEU(k)} + \beta P(fs)_{DFFSEU(j)} (1 - \tau_{dly(j)} fs) \right)$$

LET = 28.8 No TMR - checker pattern



- ***A large percentage of StartPoint DFF upsets cannot reach EndPoints ((1-τ_{dly}fs)➔0)***
- ***In this frequency range, the σ_{SEU} drop is observable and is due to losing the StartPoint SEU contribution***

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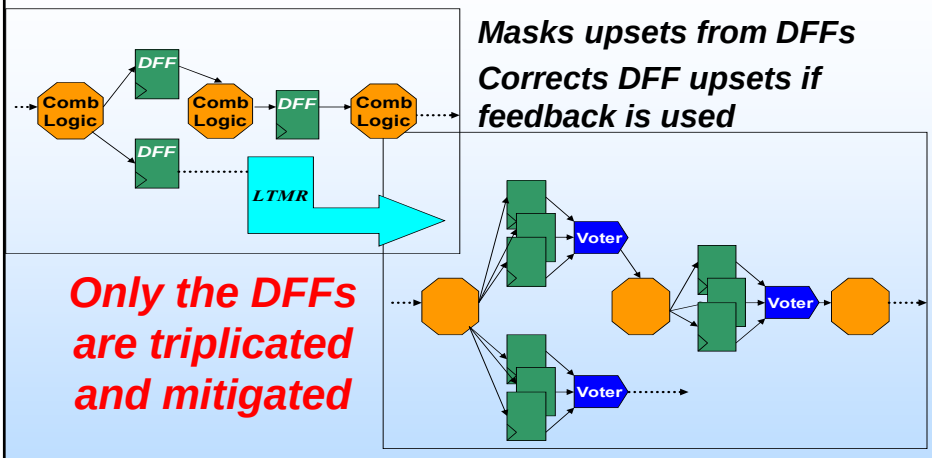
What about the SET Contribution

- Some of the WSRs have combinatorial logic.
- There should be an SET contribution to the σ_{SEU}.
- The σ_{SEU} is expected to increase with frequency
- The SET contribution can be measured by forcing DFF $P_{logic} = 0$
- This is performed by testing WSRs with localized redundancy

Localized Mitigation

- Localized mitigation is defined with respect to DFFs.
- Only the DFF is mitigated (or has radiation hardened by design components – RHBD).
- Examples:
  - Localized Triple Modular Redundancy (LTMR)
  - Dual Interlock Cell (DICE)
- Testing circuits with LTMR is an effective method for evaluating SET trends in a synchronous design

Local Triple Modular Redundancy (LTMR)



Masks upsets from DFFs

Corrects DFF upsets if feedback is used

Only the DFFs are triplicated and mitigated

$$P(fs)_{error} \propto P_{configuration} + P(fs)_{functionalLogic} + P_{SEFI}$$

$$\underbrace{P(fs)_{DFFSEU \rightarrow SEU} + P(fs)_{SET \rightarrow SEU}}_{0}$$

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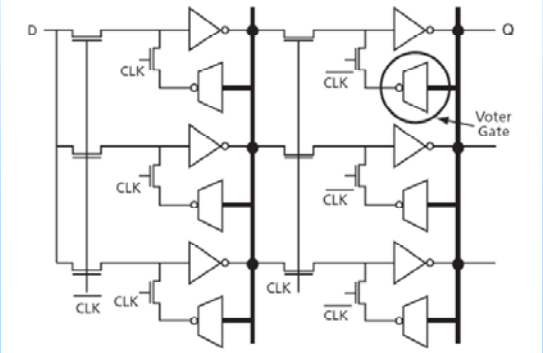
DFF with Embedded LTMR: Microsemi (Actel) RTAXs Family of FPGA

- **Localized (only at DFF)**
- **Microsemi uses Wired "OR" approach to voting – no SETs on voters**
- **Correction doesn't require a clock (asynchronous internal voter feedback)**



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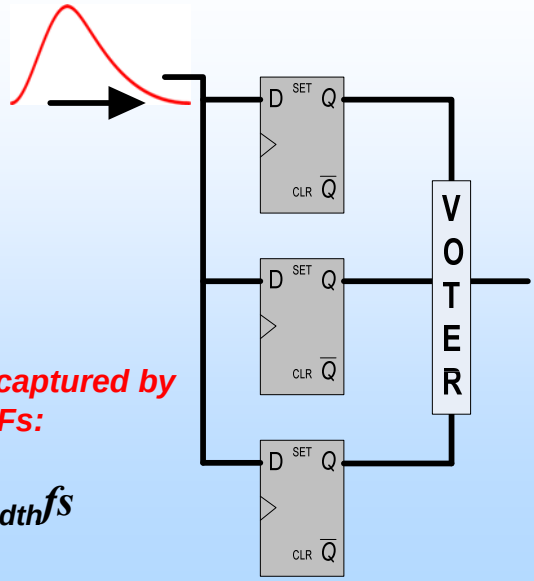
LTMR Failure

- Shared Data Path into DFFS
- Voters can upset
- Global routes



Data path SETs can be captured by the LTMR'd DFFs:

$$P_{gen}P_{prop}P_{logic}\tau_{width}fs$$

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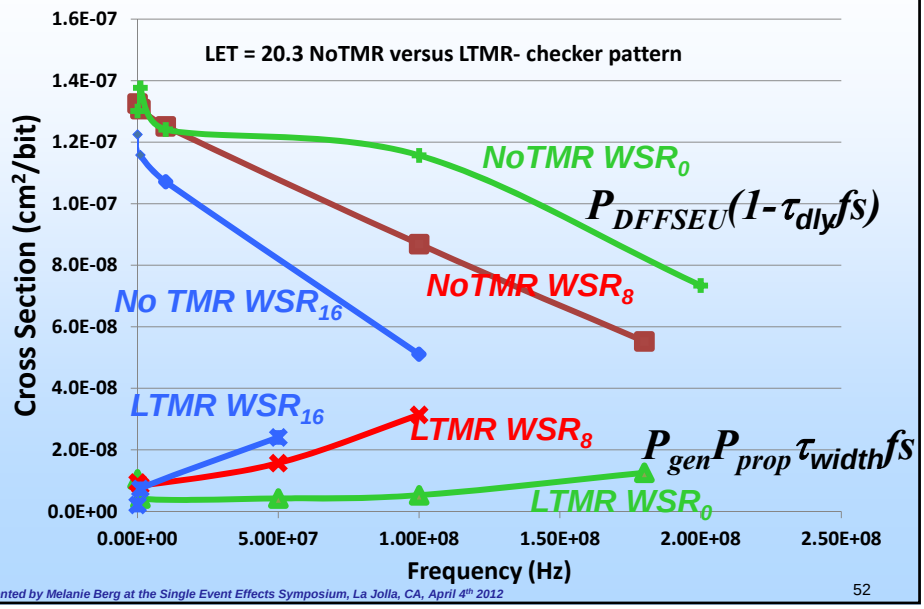
A Comparison of No-TMR versus LTMR Regard the Frequency Trends



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Comparison of StartPoint Capture versus Combinatorial Logic Capture

$$\exists_{DFF}\left(\left(\sum_{j=1}^{\#StartPoint\,DFFs} P_{DFFSEU(j)}(1-\tau_{dly(j)}fs)P_{\log ic(j)} \right) + \sum_{i=1}^{\#CombinatorialCells} (P_{gen(i)}P_{prop(i)}P_{\log ic}\tau_{width(i)}fs) \right)$$

	$P(fs)_{DFFSEU\rightarrow SEU}$	$P(fs)_{SET\rightarrow SEU}$
Logic	**StartPoint DFF Capture by EndPoint DFF**	**CL SET Capture by EndPoint DFF**
Capture percentage of τ_{clk}	$(1-\frac{\tau_{dly}}{\tau_{clk}}) = (1-\tau_{dly}\,fs)$	$\frac{\tau_{width}}{\tau_{clk}} = \tau_{width}\,fs$
Frequency Dependency	**As frequency increases, $P(fs)_{DFFSEU\rightarrow SEU}$ decreases**	**As frequency increases, $P(fs)_{SET\rightarrow SEU}$ Increases**
CL Effects	**Increase CL increases τ_{dly} and decreases $P_{DFFSEU\rightarrow SEU}$**	**Increase in CL increases P_{gen} and increases $P_{DFFSEU\rightarrow SEU}$**

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Conclusions

- **NASA Goddard REAG has developed a model to characterize upsets in synchronous designs.**
- **The characterization for the functional data path has been presented**

$$\sum_{k=1}^{\#EndPoint\,DFFs} P_{logic(k)} * \left(\begin{array}{l} \alpha P(fs)_{DFFSEU(k)} + \\ \sum_{j=1}^{\#StartPoint\,DFFs} \left(\beta P(fs)_{DFFSEU(j)}(1-\tau_{dly(j)}fs)) * P_{logic(j)} \right) + \\ \sum_{i=1}^{\#CL} (P_{gen_{(i)}} * P_{prop_{(i)}} * P_{logic_{(i)}} * \tau_{width_{(i)}}fs) \end{array} \right)$$

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Conclusions (2)

- Separation of SEU or SET generation versus system capture was described and is represented in the REAG FPGA SEU Model
- Frequency effects have been observed in DFF SEU generation as opposed to traditional theory
  - SEU generation if DFFs will increase with frequency
- Opposing frequency σ_{SEU} responses are observed for SEU generation versus SEU capture at high frequencies
  - At high frequencies, more SEUs are generated in StartPoint DFFs
  - At high frequencies, the ratio of the path delay (τ_{dly}) to the system clock period (fs) can limit StartPoint SEU capture
  - The cut-off due to the $1-\tau_{dly}fs$ term is significant and can override the increase in SEU generation

σ_{SEU} Data and REAG FPGA SEU Model agree