National Aeronautics and Space Administration

# Rapid Component Selection for RF Sub-Assemblies
# NEPP FY12 Report

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NASA Electronic Parts and Packaging (NEPP) Program
Office of Safety and Mission Assurance

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NASA WBS: 724297.40.49.11
JPL Project Number: 104593
Task Number: 40.49.01.11

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This research was carried out at the Jet Propulsion Laboratory, California Institute of Technology, and was sponsored by the National Aeronautics and Space Administration Electronic Parts and Packaging (NEPP) Program.

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## 1.0 DISCUSSION OF RF DEVICE ISSUES

The space electronic community has long established qualification standards for Electronic, Electrical, Electromechanical (EEE) device manufacturers of passive, microcircuit, and hybrid devices. These qualification specifications include standards on subcomponent element evaluation (prequalification of all subcomponent lots), wafer selection, in-process verification testing, device screening, and lot qualification. The collection of these standards has established a suitable set of devices needed for current space electronics. RF devices have, however, been left out of this device set. A major contributor to this issue exists because the bulk of RF device manufacturers are driven by the telecommunication industry, not the space radio or radar industry. Other contributing factors include unique RF designs that many RF manufacturers do not want to standardize. Space radio and radar designs have adjusted to these issues by using telecommunication/commercial-grade devices within their space designs. This practice has become acceptable because RF designers must keep pace with advancing technology and there are little to no options otherwise.

The telecommunication/commercial RF device industry is driven by handset and base-station technology demands. Other commercial device categories, in particular digital/computing elements, are also driven by similar demands; however, space-grade components still present a marketable business sector for a set of manufacturers (unlike the RF commercial MMIC market). Handset device requirements expect the lowest cost per component. Advanced screening steps add little commercial value. Commercial manufacturers supplying the handset business section, however, must ensure yields remain high to increase profit margins. The space industry can benefit from this push for high yield because of the correlation between yield and reliability [Ohring].

Base-station device requirements tend to target established reliability product lines. While infant mortality failures are acceptable to handset manufacturers, due to product warranties, base-stations must operate failure free for tens of thousands of hours between failures. Higher failure rates would pose unacceptable risk due to network failures.

One goal of the RF space community is and should continue to be to leverage the product performance of the telecommunication industry for space device requirements. In many cases, commercial-grade devices are procured and up-screened to space-level requirements to accomplish this goal. This approach, however, ignores the space electronic industries requirements of customer source inspection, in-process controls, and element evaluation.

Another goal for space RF component manufacturers is to screen out device RF components earlier rather than later in the manufacturing/assembly process. This will reduce the risk, cost, and schedule delays for failures of downstream hardware. This is not necessarily a practical goal for the commercial RF industry where success is based on profits, not mission success. The two most effective methods to deliver infant-mortality-free devices include postproduction screening to eliminate defective devices from flight lots or to manufacturer the devices with robust processes that prevent defects.

Because the space RF community will continue to use commercial-grade devices for space designs, a comprehensive quality program needs to be established that ensures the greatest amount of risk is removed from hardware at the earliest stages of manufacturing. Because the RF space community has little influence on the commercial RF community, many of the useful process controls used for space microcircuits and hybrids will not be implemented at the component manufacturing level. New process controls will have to be implemented during post-delivery device screens and system-level testing. All attempts should be made to engage manufacturers to implement quality programs beneficial to the space industry; however, the purchasing volume by space contractors might make certain process improvements undesirable for commercial manufactures. The cost of implementing these improvements would, however, benefit both electronic industries in the long term.

Current space RF designs might not be able to wait until a space manufacturer implements desired process improvement. Many space designers want to use current commercial technology without the delay of extended collaboration and audits. A custom RF development could take as long as three years, from initial conception to device delivery. Projects using nonrecurring designs might also not want to make the large investments into a manufacturer to achieve space-grade components—especially if the customer is not likely to repeat the design in future hardware.

In this paper, many of these possible process improvements will be discussed, as well as post-production screens, which also reduce infant mortality risk. A combination of manufacturer process improvement and postproduction processing can make commercial RF technology a viable and cutting edge solution for space.

## 1.1 Space qualification of RF devices

Common space-grade devices used by aerospace companies meet the standards of MIL-PRF-38534 (hybrids), MIL-PRF-38535 (monolithic microcircuits), and MIL-PRF-19500 (discrete semiconductors). Common RF devices used for space application, however, do not meet such standards initially and must be up-screened to space-grade part requirements. The fact that MIL-PRF-19500 slash sheets and MIL-PRF-38535-compliant surface-mount devices (SMDs) do not exist for common RF devices is troubling. It is not completely understood why standardized requirements have never been a priority, but demand and profits are the obvious contributing factors.

Many space-discrete semiconductor manufacturers (such as Microsemi) have produced qualified lots of large-signal bipolar junction transistors (BJTs) following equivalent MIL-PRF-19500 standard, yet the demand by their customers has not pushed this manufacturer to qualify these particular devices, per Qualified Manufacturer List (QML) requirements.

Likewise many microwave monolithic integrated circuit (MMIC) manufacturers do not qualify product lines for space. Despite a need by RF space designers for qualified MMIC devices, many manufacturers have steered clear of standardized “off-the-shelf” qualified lines and only deliver space-grade devices per individual customer orders. Many RF MMIC vendors will not even package their devices (a typical must for space electronics) due to electrical parasitics that degrade performance. A viable packaging solution for the die that meets both performance and reliability requirements is left up to the customer.

A slew of RF hybrid manufacturers familiar with space hybrid requirements do exist. Many of these vendors are competent providers of space-qualified custom hybrids; however, because these custom hybrids have unique designs and low production volumes, many of these manufacturers do not qualify these product lines. A close relation between RF manufacturers and space customers is needed to ensure quality processing and supply of space-grade RF components.

An additional set of RF devices also exists. This category of devices includes both passive and active devices and includes RF couplers, isolators, power dividers, and mixers. There are not even current viable QML standards to establish baseline device requirement for current surface mount devices of these families. Older military-grade standards are often referred to; many do not address current manufacturing issues and testing. Qualifying these devices depends heavy on the experience of the device specialist and collaboration with the manufacturer.

Manufacturers (such as Merrimac) specialize in couplers and power dividers for space applications. Their space requirements, however, do not come from a QML performance specification, but rather the manufacturer’s own internal requirement document. Many space RF companies have released similar documents. Issues, however, arise from the lack of universal requirements. This issue might come from the fact that many typical screens, such as burn-in, have little to no relevance on many of these passive devices. The likely cause for a device failure is a workmanship defect. Burn-in could not properly screen out these issues.

Many RF manufactures have no interest in screening devices for aerospace companies. Their commercial product lines are thriving and they have no interest in changing their business model. This becomes as larger issue when subcomponents (elements) are installed without element evaluation. At this point, it becomes almost impossible to qualify these devices to space requirements.

Getting a vendor to quote, build, and screen to a space-level source control drawing (SCD) is not a trivial effort. Many vendors are not willing to allow external customers insight to internal processes. While they might agree to customer source inspection and pre-cap visual inspections, insight into standard packaging, wafer selection, and device testing is withheld from a customer. These details become important in determining the suitability of a commercial device for space and what screens are needed to insure the delivery of an infant mortality-free flight lot.

The ultimate goal for a rapid RF assembly development would be to eliminate two/three-year lead times for custom RF devices and use existing technology that can appropriately be screened for space. With proper implementation the second option can reduce lead times to 12 to 18 months.

## 1.2 How does JPL handle rapid RF development?

How does JPL (or any aerospace contractor) take commercial/hi-rel devices that do not initially meet space EEE part requirements and rapidly qualify these devices for space application?

In the attempt to balance the cost of mission requirements with acceptable failure rates, most aerospace companies have established separate levels for part requirements. These levels can be divided into multiple categories. The highest categories are the most stringent and allow little to no deviation from the requirements. The lowest levels allow for requirement flexibility and could allow the shifting of device screening/qualification to different assembly levels.

The highest level requirements are intended for large missions primarily built in-house using complex single-string spacecraft architectures. Mission durations typically are greater than five years. Mission durations greater than 10 years are common. Device requirements include full wafer-level acceptance, in-process verification, 100% flight lot screening, and a full flight lot qualification. Only approved space-qualified manufactures should be used. Deviations from standard space requirements are highly ill advised.

The lower level mission requirements, which allow for flexibility in requirements, are shorter life and lower cost missions. These missions typically are technology demonstrations or science instruments whose failure would not/could not be detrimental to overall mission success. Many of these technology demonstrations or instruments could benefit greatly by leveraging the performance of commercial-grade RF technology. In addition, many aerospace companies will not invest into an advanced RF technology without first proving its viability during a demonstration mission. Once a technology has initially been successfully, further space adaptations to the product line would be seen as beneficial to both the aerospace customer and the device manufacturer.

Lower level mission requirements would allow custom qualification plans (a case study will be discussed) to be used and approved by a review board of RF device specialists, RF designers, mission assurance, and management. Additional examples will be presented covering a variety of device types. Alternate screening scenarios will also be discussed.

## 2.0 NON-STANDARD RF DEVICES UP-SCREENED FOR SPACE APPLICATIONS

Tables 2.0-1 through 2.0-4 list nonstandard RF devices used on various JPL missions. Each device had to be up-screened to project requirements. Typically the time period between the devices being selected in a preliminary design to releasing an approved SCD for the flight lot is six to nine months. Once the manufacturer has agreed to the requirements of the SCD an additional four- to six-month lead time can be an expected for flight lots.

Table 2.0-1. RF-discrete semiconductors used by JPL (no QML qualification).

| Part Number | Manufacturer | Description | Project | How Up-Screened? |
|---|---|---|---|---|
| 1214-300M | Microsemi | Transistor, BJT, Common Base, 600W, 70V | SMAP | Manufacturer up-screened to JPL SCD |
| MLD00130 | M/A-COM | Transistor, RF, Silicon, Low Noise, Bipolar | MSL | Approved via wavier |
| AT 42070 | AVAGO | Transistor, High Frequency, Silicon | MSL | Manufacturer up-screened to subcontractor SCD |
| MGF2430AV-12 | Mitsubishi | Transistor, FET, GaAs, 5W, 800mA | SMAP | Manufacturer up-screened to manufacturer specification |
| 1SV305 | Toshiba | Varactor Diode, GaAs, PEM | GRAIL | Test house up-screened to JPL SCD |

Table 2.0-2. Packaged RF MMICs used by JPL (no QML qualification).

| Part Number | Manufacturer | Description | Project | How Up-Screened? |
|---|---|---|---|---|
| HMC4988LH5 | Hittite Microwave | Amplifier, Power, Medium, PHEMT, GaAs | GRAIL | Manufacturer up-screened to JPL SCD |
| PE97042-11 | Peregrine | Synthesizer, Frequency, PLL, 3.5 GHz | SMAP | Manufacturer up-screened to manufacturer space specification (01/0015~00D) |
| AFS2-02000400-08-HE-4V/883 | Miteq | LNA, S Band, 4V, 2–4 GHz, 20dB | GRAIL | Manufacturer up-screened to 883 Military specification (traveler 150218) with additional pre-cap and electrical testing |
| SLN-286 | Stanford Microdevices | Amplifier, LNA, MMIC, PEM, 3V, DC–3.5GHz | JASON-3 | Test house up-screened to JPL SCD |

Table 2.0-3. RF MMICs die used by JPL (no QML qualification).

| Part Number | Manufacturer | Description | Project | How Up-Screened? |
|---|---|---|---|---|
| B016621-0001 | Triquint | Gain Block, HBT, InGaP, DC–6GHz | GRAIL | Approved via nonstandard part approval request (NSPAR) |
| AP640R2-00 | Alpha | Switch, MMIC, SPDT | JASON-3 | Commercial die with assembly-level screening |
| CHA3689-99S/00 | UMS | Amplifier, LNA, MMIC, | JASON-3 | Manufacturer wafer and lot acceptance testing per MIL-STD-883; assembly-level screening by manufacturer |
| FMM5703X-S | Sumitomo | Amplifier, LNA, MMIC, 24–32 GHz | JASON-3 | Manufacturer wafer and lot acceptance per manufacturer specification; assembly-level screening |

Table 2.0-4. General RF devices used by JPL (no QML qualification).

| Part Number | Manufacturer | Description | Project | How Up-Screened? |
|---|---|---|---|---|
| H-2014 | EMC | Coupler, Hybrid, RF, 100W | SMAP | Manufacturer up-screened to JPL SCD |

| Part Number | Manufacturer | Description | Project | How Up-Screened? |
|---|---|---|---|---|
| 2IMC-21.3-2-21.3BW26.29 | Dorado | Isolator, RF, 18.5–24.1GHz, 1W, 20dB | JASON-3 | System-level screening; DPA and qualification tests |
| DS-313 | M/A-COM | Divider, Two way, 10–2000 MHz | SMAP | Manufacturer up-screened to JPL SCD |
| QHdZ-2H-2.1G/79831SQ | Merrimac | Quad Hybrid, 2–3 GHz | GRAIL | Vendor up screened; manufacturer space specification |
| M2-0002 | Marki Microwave | Mixer, Triple-Balanced | AQUARIUS | Test house up-screened to JPL SCD |

As discussed, many commercial RF device manufacturers are not willing to space qualify particular product lines for space applications without a large investment from their customers. JPL cannot and/or will not fund procurement of this nature due to the small volume of devices it uses. These manufacturers are willing, however, to screen individual device lots per an SCD.

How can JPL develop screening and qualification plans that use as many prepackaging screens provided by the manufacturer, with a combination of package/die screens either at the component or assembly level to ensure RF components are infant mortality free?

A balanced approach can be used. Commercially proven technology can be adapted for space with a well-defined qualification plan. Required steps will depend on device type and packaging parasitics. If standard screens are not viable, suitable alternatives must be found to mitigate these risks. One example is numerous MMIC devices sold are bare die. The manufacturers of these die will guarantee performance; however, they cannot guarantee die performance after packaging. Users of these devices may not want to package the device, but instead use the bare die on a chip-on-board/chip-on-carrier solution [Lau]. By implementing the design with a chip-on-carrier approach, many packaging parasitics that affect RF electrical performance can be eliminated.

These issues are not unique to RF devices; however, the combination of high frequency/high power verification testing, a variety of device construction, and using multiple vendors for manufacturing and testing can complicate screening and must be monitored carefully.

With a balanced approach, screening and testing can occur at various stages in the implementation of the final space-qualified device. These stages include die/element-level testing, in-process testing during packaging, component-level screening, and final qualification of the components at the assembly level. These different screening paths will be discussed, as well as the steps JPL can even perform in-house to reduce cost, risk, and schedule delays.

## 3.0 DIE/ELEMENT-LEVEL TESTING

Prior to the installation of a subcomponent (die, substrate, passive) into an RF assembly, multiple screening methods could be used or developed to reduce the likelihood of a faulty element being selected. These methods include SEM examination, element evaluation, wafer probe, and even design-for-testability approach. Many commercial RF manufacturers may be unable to implement these inspection steps. A space customer must be willing to either fund the manufacturer to establish these capabilities, provide alternate sources for these capabilities (in-house or third party), or devise a plan where the risk for not performing these inspection is minimized. These screening methods and their issues are discussed below.

### 3.1 Scanning electron microscope (SEM) examination

Wafer lot acceptance should only occur after a successful SEM metallization exam. Requirements are based on MIL-STD-883 TM 2018 for MMICs and MIL-STD-750 TM 2077 for discrete semiconductors. Many die manufacturers, however, do not perform this examination on a 100% lot basis. 100% lot SEM examination is, however, extremely desirable. It allows the manufacturer to track wafer lot variation. A space customer could, however, perform this testing in-house on the actual flight lot if it is not available from manufacturer. SEM examination failures would deem a lot unusable for flight. The use of other lots of the same die design would need to be subjected to additional SEM examination. The risk of a new nonconforming lot would increase, however, due to the possibility of a lack of process control by the manufacturer, which caused the initial lot failure.

### 3.2 Active element evaluation

Wafer lot acceptance should also only occur after a successful microcircuit/semiconductor dice evaluation. Requirements are based on MIL-PRF-38534 section C.3. Project requirement will dictate the level and necessity of element evaluation requirements. While basic element evaluation provides 100% electrical and visual inspection of all flight lot dice, it does not provide a 100% burn-in of all the dice. Burn-in would occur at a high level of integration, which can pass on an infant mortality risk and schedule delays if failures occur. Although it would be advantageous to perform burn-in at the component level, it is not feasible due to these bare die components.

More stringent subgroup 4 element evaluations can provide a sample wafer lot “qualification,” which includes a sample screening/burn-in plan and life-test. Due to the low sample requirements, subgroup 4 might provide an unrealistic expectation of 100% successful burn-in for flight lot devices at the next higher level of integration. The exact conditions of the subgroup 4 burn-in/life-test may not be fully replicated in higher level assemblies either. There can be no guarantee the packaging used during the die element evaluation will replicate the conditions for the actual flight units. This is because die attachment plays a critical role in both thermal dissipation and signal grounding. Such differences could manifest as unexpected shifts in parametric performance when assembly integration is completed.

### 3.3 Passive element evaluation

In cases were RF devices require power-grade-discrete passives, element evaluation can be avoided by procuring space-grade passives, which have been individually screened and qualified with Group A and B testing directly from the manufacturer. By avoiding element evaluation, schedule delays can be avoided. This practice is extremely valuable for small production lots.

### 3.4 Wafer probe

Current probe tests for RF MMICs include both DC and RF measurements. DC measurements are more prevalent and have established methodologies. There is a need for on-wafer S-parameter measurements [Fisher]. Such measurements require microwave probes that have correct impedance matching and must

be calibrated to ensure proper s-parameter measurements. Modern microwave probes have abandoned coaxial structures in lieu of three lead planer probes. On these probes, the center signal probe is surrounded by two ground probes. Die must be designed to include signal pads that accept all three probes. With proper high speed impedance matching, all s-parameter measurements could be recorded with compatible vector network analyzers (VNAs). The commercial RF manufacturer must be willing to incorporate the correct pad design onto die to accommodate these types of microwave probes. Finding die that already incorporate this technology would add a valuable rapid screen, which would allow a space customer to use Known Good Die (KGD).

The demand for KGD is still critical for RF devices due to the high cost of RF packages and the low yield of many RF ICs [Fisher]. KGD will also reduce the need for component rework, which is still a major manufacturing issue for RF assemblies. Critical properties of these RF probes include ultra-low contact resistance and small contact area [Fisher]. This combination reduces RC impedance and allows increased switching speeds. The goal is for the probes to have symmetrical ground performance to reduce the area between signal and ground. Because these tests will originate from an RF MMIC manufacturer, the manufacturer will have to ensure proper procedures are followed. Auditing these processes, would be a great risk deduction for the end customer. Finally, the implementation of KGD and wafer probing itself is a complex, time consuming, and costly effort. Space customers wishing to use this methodology in a rapid RF development must rely on manufacturers who have already established technology in this arena.

### 3.5 Design-for-Test (DFT)

DFT is already an established technology for digital devices. DFT is not, however, common among RF die manufacturers, due to issues from RF electrical measurements based on forward propagation and reflected power levels instead of logic-level signals. EVM and XYZ have excellent methods to digitize RF measurements thus simplifying these measurements for computation.

Research into developing RF DFT architectures is showing a strong benefit for future RF developments. This is due to the fact that semiconductor costs have dropped while IC test costs have remained stagnant [Fan]. Fan states that the cost of implementing DFT architecture on an RF IC would be negligible on wafer fabrication. Fan continues to list common RF receiver tests: NF, gain, IIP3, IIP2, RSB, gain compression, BBAF, SNDR, DC offset, and transmitter RF test including: gain control, gain flatness, ACPR, AltCPR, image suppression, carrier suppression, PDET, EVM, harmonic spurs, and linearity tests that would be useful DFTs. Many of these tests, however, are not currently compatible with built-in self-test (BIST). Further development is needed to properly implement such tests.

To implement a BIST for an RF IC, an RF loopback must be designed into the semiconductor [Fan]. Fan continues by stating the loopback can be accomplished by bypassing the antenna and having the transmit signal return directly into the receive circuitry. The key to this BIST layout is proper attenuation of the transmitted signal [Fan]. A huge advantage is on-chip impedance matching vs. extensive matching networks needed on an automated test equipment (ATE) test board. The key drawback with RF BIST is proper isolation of Tx/Rx after the BIST has completed; when the device is operating as designed. These integrated tests still require external bit chains to be inputted to the ADC/DAC of the transceiver; just as digital bit trains are required for BIST on digital ICs.

Other BIST for RF ICs include the use of power measurements on each element on the IC, which can be translated into digital with on-chip ADCs. These tests would be useful due to the fact that there is a strong correlation between power consumption and degradation in the Tx/Rx elements [Fan].

Once again a space customer wishing to rapidly implement a DFT or BIST for an RF component must pursue manufacturers who have established designs.

The highest benefit DFT for RF ICs would be increases in wafer yields, which directly increase wafer reliability. However, without the RF IC manufacturer's input on yield, these tests can do little to steer downstream screening options for these ICs. The sophistication of RF ICs must also include control

registers to ensure the device is in the correct mode of operation. These registers would increase I/O demand and convert an RF IC into a mixed-signal IC [Fan].

# 4.0 COMPONENT-LEVEL TESTING (SPACE GRADE)

## 4.1 Active device screening

Packaged discrete semiconductors and MMIC devices should be 100% screened, per MIL-PRF-19500 and MIL-PRF-38535 requirements respectively. Screening tests could include pre-cap visual, temperature cycling, constant acceleration, PIND, electrical, burn-in, hermeticity tests, and external visual inspections. Device requirements are based on project requirements. Each device screen listed previously has its own defined test method for each of the defined inspections. These test methods are designed to screen out infant mortality failures due to defects in the die or packaging. Many RF die are not compatible to typical IC packaging due to the electrical parasitics of the package and/or the inability to provide 50 ohm port matching [Lau]. Because of these limitations, chip-on-board and chip-on-carrier packaging methodologies offer viable solutions for bare die. Clear screening criteria for these implementations, however, have yet to be properly defined. MIL-PRF-38534 requirements could be used if the circuits are implemented on a common substrate; however, chip-on-board solutions do not necessarily meet this requirement.

## 4.2 Passive device screening

Many RF passive devices do not have clear screening procedures due to the simplicity of the devices. RF passive devices (resistors, capacitors, and inductors) do not typically follow standard film deposition or core wiring construction as typical passive devices for power applications. RF passives are typically constructed using microstrip transmission paths on substrates with known dielectric constants. Coil inductors, parallel plate capacitors, and 50 ohm transmission paths and terminations can be constructed using microstrip technology. Many of these passive elements are delivered unscreened with all initial temperature cycling occurring at the assembly level. There typically is not a need for extensive screening beyond a comprehensive visual inspection. This is due to the fact that these substrate elements cannot be electrically tested until bonded to boards or carriers. The vast majority of defects are solely due to the deposition of the microstrip material on the dialectic substrate. Visual inspection and lot qualification test can properly reduce risk and prevent failures.

## 4.3 Device lot qualification

Lot qualification is used to prove the effectiveness of the screening process. If screening properly removed infant mortality failures from the flight lot, no qualification failures should be expected. Qualification testing proves this (within a confidence range) by operating the device into a usage state where constant failures rates can be expected. Lot qualification typically includes Group A tri-temp electrical testing, Group B package qualification tests, and Group C life qualification tests.

## 4.4 Destructive physical analysis/construction analysis

DPAs can provide insight into assembly and packaging processes. A construction analysis should be performed on all commercial RF devices before any attempt to space qualify them. A sample size of five devices will show consistency within a device lot and if reoccurring issues exist. If anomalies are seen in only one of the samples, best engineering judgment must be used to factor if the anomaly warrants the rejection of the lot or device technology. Any systemic issue, of course, would warrant rejection. Undesired quality could be identified early. Recommended device alternatives could be found.

While DPA requirements are clearly defined for MMIC and RF discrete semiconductors, many passive RF devices do not have clear standards. A full understanding of the device type is necessary for a proper DPA evaluation. This understanding can be obtained from discussions with the manufacturer to understand the intent and processing of devices.

## 5.0 ASSEMBLY-LEVEL TESTING OF DIE

### 5.1 KGD testing

NGD testing is not a common practice currently due to the low manufacturing cost of silicon and GaAs semiconductors. Testing costs have not, however, decreased in a similar scale. Many commercial RF die manufactures are willing to bypass full functional wafer probe tests for a combination of wafer acceptance, element evaluation, and DC probing. This suite of tests, however, might not sufficiently screen RF die for space applications. This is because tri-temperature electrical testing and burn-in cannot be performed on unbounded die. RF die must have an excellent ground and thermal pad to achieve specified performance. Chip-on-board/chip carrier designs are particularly venerable to Unknown Bad Die [Lau]. Because of this issue, RF system manufacturers need an economical approach to assemble and test RF die at as low an assembly level as possible. This approach will screen out defective die earlier in the implementation phase, which will minimize the effects of board-level failures.

JPL has devised a carrier-based approach for bare die, which allows for individual chip DC biasing during burn-in. This approach will allows each chip to have a maximized burn-in junction temperature. This approach is similar to a chip-on-board; however, devices are bonded to substrates not a wiring board. The substrate provides a better CTE match and thermal conductivity. Each carrier acts as a bonding substrate that can provide a constant baseplate temperature. Die are bonded into signal chains and individually biased. Burn-in and screening occurs after the dice are bonded to the carrier. The current draw back with the methodology is the inabilities to electrical test each individual device after integration. The performance characteristics of the entire chain must be tested simultaneously. Only the insertion loss/return loss/gain of the entire carrier can be measured. Individual current biasing of each chip, however, can be monitored. This is acceptable for small signal amplifiers; however, individual s-parameters are desirable to fully characterize the performance of large signal pulsed amplifiers.

These test methodologies can be based on MIL-PRF-38534 element evaluation requirements but applied on a 100% bias for each carrier. If individual carriers are found to be noncompliant, the carrier can either be scraped or reworked. The true advantage of the carrier comes at this point in assembly. If multiple identical carriers have been assembled, screened, and tested simultaneously, a one-for-one swap can be completed, minimizing rework schedule delays.

### 5.2 Ribbon and wire bonding

Ribbon bonds are qualified through destructive coupon testing. These coupons are assembled in parallel with flight hardware using identical processes, materials, and technicians. In-house testing should follow MIL-PRF-38534 methodologies. MIL-STD-883 test method 2011 defines the procedure for destructive bond pull.

### 5.3 Third-party vendor testing

Commercial-grade devices are purchased, which are then sent to a third-party test-house for inspection, serialization, and testing. Up-screening plans and specifications must be agreed to by both the space customer and the test-house. Sample units should be subjected to defined test methods before actual flight units are tested. This step prevents troubleshooting on flight units and preserves screening yield. All flight devices should originate from a single lot date code. This ensures all flight devices will be subjected to identical manufacturing processes and the screens will yield similar results for all devices.

Many high frequency RF manufactures have custom device test fixtures designed to maximize electrical performance during test. A third-party test-house might not be able to reproduce this level of performance without destructively bonding flight devices to a substrate or test board. This bonding is not acceptable for flight hardware, rendering it unusable. If device-level performance cannot be accurately measured on

individual flight units, viable options include an increased destructive qualification sample (where qualification units are bonded for electrical test) or system-level performance verification.

Other issues include poor manufacturing techniques by RF commercial manufactures. Unlike the commercial-grade digital device, many commercial-grade RF devices are still handmade and/or hand tuned. Lot variation is common and should be expected. Common defects include wire bonding issues, die attach issues, solder attach issues, and lid seal/encapsulate issues. Because of these manufacturing issues, lower yields should be expected. Because of these lower yields, extensive screening becomes vital for both space-grade RF devices and commercial devices up-screened to space requirements.

## 6.0 CURRENT RF PACKAGING AND MANUFACTURING (COMMERCIAL/HIGH RELIABILITY)

Current RF packing, screening, and qualification methodologies will be discussed to understand differences between commercial and space-grade RF devices.

RF/microwave packaging presents unique performance difficulties uncharacteristic of other standard microcircuit devices. The RF wavelengths relative to the device circuit lengths result in phase interactions which affect device parameters. General analog terms of voltage and current have less meaning than power, field strength, and loss [Green]. Due to these issues, typical microcircuit design is avoided. Transmission line topologies must be used. Standardized, passive-discrete elements (inductors, resistors, tuning stubs, and some capacitors) can be implemented with microstrip device structures. Microstrip (Microstrip, Coplanar, and Stripline) ensures predictable dielectric properties, loss, and impedance matching [Green]. Microstrip topologies can also implement RF coupler, dividers, and power combiners.

Standard MIL-PRF-38534 element elevation criteria are defined for microcircuit/die, passive, surface acoustic wave, substrate, package, and polymeric elements. Elements not falling into these categories still need element evaluation; however, the definitions do not exist. It is up to a commercial RF manufacturer and space customer to define evaluation requirements for these elements. Typically for projects with lower component requirements, 100% visual, performance, and sample-based bonding test will suffice.

Because MIL standard test methods are defined for discrete passive elements, not microstrip structures, unique processes might need to be developed. Typical commercial processes are highly controlled making them acceptable alternatives for space application. Many of these elements rely less on screening to ensure quality deliverables and more on tight process controls. Typical component screens such as power conditioning and thermal cycling will not be as informative as evaluating the manufacturing processes for the deposition and etch of these elements. Numerous in-process monitors for plating, wire-bonding, shear testing, substrate metal adhesion, metal cross sections, and electrical sampling will ensure the elements will meet performance requirements. When dealing with commercial manufacturers, space customers need insight into how manufacturers are using in-process monitors to improve lot yields. Slight tweaks of these requirements might be needed to ensure compliance for space. This can only occur with a close working relationship with the manufacturer. Getting a manufacturer to alter their internal processes is a difficult issue and beyond the scope of this paper.

While traditional device screens are not completely applicable to microstrip devices, system-level screens are still needed to ensure stable performance over temperature. System-level screens include thermal cycling, high temperature bakes, and system-level RF measurements.

Capacitors performance cannot readily be replicated with microstrip topologies. Discrete capacitors are often required, in addition to other microstrip circuitry. Space- and military-grade discrete capacitors should be used. Convincing a commercial manufacturer to stop using commercial-grade discrete capacitors can be a difficult task in itself; however, many space-grade capacitors are based on commercial product lines. The current adhesion and test procedures of these discrete capacitors many not have to be severely altered to upgrade to space discretes. A cost benefit analysis for a commercial lot with class K element evaluation vs. procuring standard space-grade capacitors might easily prove to a manufacturer that procuring space-grade discretes is the optimal choice for small lot quantities.

The vast majority of commercial RF manufacturers use gold wire/ribbon bonding techniques similar to space RF manufacturers. Proper RF performance tends to only be achievable with RF ribbon bonds when connecting Stripline RF traces. Aluminum bonds should be avoided. Manufacturers using aluminum bonds for RF manufacturing should be avoided. Commercial RF manufacturers need to be extremely familiar with MIL-STD-883 visual inspection criteria for wire and ribbon bonding.

Often commercial RF manufacturers will follow the standard MIL-STD-883 test method for destructive bond pulls. This is where similarities between commercial RF designs and space RF designs crease. Commercial RF manufacturers are only obligated to monitor their own processes to their own

requirements. The frequency and need for in-process wire bond pull tests needs to be clearly defined in customer requirements. The familiarity to non-destructive bond pull might also be a critical issue. If a commercial manufacturer has no established methods for non-destructive bond pull, considerable training and quality assurance monitoring needs to be implemented.

Commercial and space RF devices are tuned by similar methodologies. Typically this procedure requires the 50 ohm input and output ports to be interfaced with a network analyzer. A technician then preforms tuning steps on the RF device until the RF device under test meets the required s-parameter measurements over the required bandwidth. Tuning steps can be as simple as physically etching away material (transmission path or dielectric) on the device on designated tuning metallization, or as complex as laser trimming out networks of transmissions paths thus eliminating excess resistance and capacitance. Ultimately, the effect is the same. The largest difference between space and commercial processing is the documentation of the processing and quality assurance oversight. It typically is not advantageous for a space customer to attempt to alter or improve a manufacturer's tuning procedures. The tuning procedures are intimately defined by the technology of the RF device. If a space customer finds a manufacturer's tuning procedures to be unacceptable, the best path forward would be to find an alternate supplier.

Commercial RF devices are not typically hermetically sealed. Many devices are designed to operating in air due it dielectric constant and to prevent multipaction. Devices that are sealed typically follow similar hermeticity testing as space-grade RF devices. These tests are defined in MIL-STD-883 TM 1014 (fine and gross leak) and must be performed by commercial manufacturers who claim hermetic devices. Residual gas analysis testing must also be performed to ensure proper sealing procedures and environment.

## 7.0 DEVICE SCREENING

Tables 7.0-1 through 7.0-3 contain standard screens for space-level components. Screening occurs on a 100% basis on delivered flight RF components. RF components not meeting the criteria listed below are rejected and removed from the screening flow. An RF device is not technically space screened until it has passed each of the listed screens for its corresponding category.

Table 7.0-1. MIL-PRF-38534 RF hybrid device screening.

| Test | Method (MIL-STD-883) | Condition |
|---|---|---|
| Non-destructive bond pull | 2023 | 100 percent of wires |
| Open burn-in | 1030 | Optional |
| Internal visual | 2017 | |
| Temperature cycle | 1010 | Condition B, 10 cycles<br>−55°C to 125°C |
| Constant acceleration or mechanical shock | 2001<br>2002 | 3000 G, Y1 direction<br>Condition B, Y1 direction |
| PIND | 2020 | Condition A |
| Pre-burn-in electrical | | |
| Burn-in | 1015 | 320 hours at 125 °C |
| Final electrical | | |
| Seal (fine and gross) | 1014 | |
| Radiographic | 2012 | Optional |
| External visual | 2009 | |

Table 7.0-2. MIL-PRF-19500 RF-discrete semiconductor device screening.

| Test | Method (MIL-STD-750) | Condition |
|---|---|---|
| Die visual | 2073 | Condition B |
| Internal visual | 2074<br>2069<br>2070 | Diodes<br>Power FETS<br>Microwave transistors |
| Stabilization bake | 1032 | As needed |
| Temperature cycle | 1051 | |
| Constant acceleration | 2006 | Y1 at 20,000 G; 10, 000 G for >10 watts |
| PIND | 2052 | Condition A |
| Interim electrical | | |
| High temperature reverse bias | 1039<br>1042<br>1038 | Condition A (Transistors)<br>Condition B (Power FETS)<br>Condition A (Diodes) |
| Interim electrical | | |
| Burn-in | 1039<br>1038<br>1042 | Condition B (Bipolar Transistors)<br>Condition B (Diodes)<br>Condition A (Power FETs) |
| Final electrical | | |
| Seal (fine and gross) | 1071 | Not required on double plug diodes |
| Radiographic | 2076 | |
| External visual | 2071 | |

Table 7.0-3. MIL-STD-883 test method 5010 MMIC device screening.

| Test | Method (MIL-STD-883) | Condition |
|---|---|---|
| Wafer lot acceptance | 5010 appendix II and 5007 | |
| Non-destructive bond pull | 2023 | 100 percent of wires |
| Internal visual | 2010 | Condition A |
| Stabilization bake | | As needed |
| Temperature cycle | 1010 | Condition C |

| Test | Method (MIL-STD-883) | Condition |
|---|---|---|
| Constant acceleration | 2001 | Condition E, Y1 direction only |
| Visual inspection | | |
| PIND | 2020 | Condition A |
| Pre-burn-in electrical | | |
| Burn-in | 1015 | 240 hours at 125°C |
| Interim electrical | | |
| Reverse bias burn-in | 1015 | Condition A or C, 72 hours at 150°C |
| Final electrical | | |
| Seal (fine and gross) | 1014 | |
| Radiographic | 2012 | Two views |
| External visual | 2009 | |

MMIC devices also differ from common analog and digital monolithic die. Many MMIC die do not have passivation or have polymer layers to control the dielectric constant of the RF material. MMICs also commonly use air-bridges rather than vias for signal propagation. Airbridges are unpassivized and are commonly damaged due to improper handling.

## 8.0 COMMERCIAL SCREENING ISSUES

Many of the above mentioned screens might not be applicable to all devices. A risk analysis must be performed with non-space-qualified RF devices to ensure each screen provides additional benefit rather than increased risk. Table 8.0-1 discusses issues with the screens listed above and possible alternatives to mitigate similar risks. These issues must be considered by an RF component specialist when devising a screening flow for any non-space-qualified RF device. The goal of these screens is to prevent infant mortal devices, which contain defects from being issued as flight conforming devices. Screens should not introduce unnecessary risk.

Table 8.0-1. Device screening issues.

| Test | Issue | Alternative |
|---|---|---|
| Wafer lot acceptance | Commercial die can be purchased without wafer lot acceptance | A commercial die lot can be qualified post-production via a SEM metallization exam by the space customer |
| 100% non-destructive bond pull | Kinks in ribbon bonds can cause undesired reflections | Destructive bond pull on coupon substrates manufactured in parallel with flight devices |
| Open burn-in | Many RF die are not passivated. High temperature operation in non-inert environment could cause reliably risk | The goal of an open burn-in is to allow rework before package seal. A cost benefit analysis must be performed to determine if rework vs. scrap is more appropriate. |
| Internal visual | Commercial device are not manufactured to the tight visual constraints of space-level hybrids | Internal visual is a must and many space requirements must be adhered. Many nonconformities do not pose a reliability risk. These issues must be understood and risk assessed. |
| Temperature cycle | Many commercial-grade devices are not capable of withstanding a −55°C to 125°C temperature swing or the rapid temperature swing required by test method 1010 | Modify temperature swing to devices nonoperating maximum and minimum. Lower ramp rate to an acceptable transition. |
| Constant acceleration or mechanical shock | Many hybrid devices can not fit properly into a centrifuge | Qualification of design on flight lot samples to a higher 5000 G (mechanical shock) |
| PIND | Many do not apply to device construction. Natural resonance frequencies might exist in the commercial device. | Critical internal visual inspection can be used to mitigate risk |
| Pre-burn-in electrical | Should only occur if burn-in is applicable | |
| HTRB | Reverse bias might be incompatible with some transistor/MMIC technologies | Proper biasing schemes must be established with the manufacturer |
| Burn-in | Passive RF hybrids might not require burn-in. It may be impractical to RF burn-in on active devices. An appropriate DC burn-in that properly removes infant mortals could be established. | Temperature conditioning could be used to stabilize electrical performance on passive RF devices. Extensive life-testing must be performed to ensure infant mortal have been removed from flight lot |
| Final electrical | Many high frequency device must be soldered into test boards to measure proper RF performance | Higher number of destructive qualification test samples must be tested. The device lot performance must have a uniform distribution with enough margins to ensure RF performance on flight devices. |
| Seal (fine and gross) | Many commercial-level hybrids are not hermetic | Follow non-hermetic hybrid screening flows |

| Test | Issue | Alternative |
|---|---|---|
| Radiographic | Package might be opaque to x-ray | A construction analysis could be used to verify such a condition |
| External visual | Commercial device are not manufactured to the tight visual constraints of space-level hybrids | Nonconformities must be risk assessed. Overly strict rejection criteria may not improve device reliability. |

Nonconformities should be documented in an EEE part waiver. These nonconformities could include omitted screening steps, higher but expected percentage defective allowable, and inapplicable screens.

Other issues that need to be considered when converting a commercial RF device into a space commercial device include rework, increased qualification, and cost of screening at a higher level of assembly. These issues are listed below.

Additionally, rework constrains are defined differently for commercial devices. All rework procedures performed by commercial manufacturers must be reviewed and approved by the space customer. Commercial manufacturers should not be allowed to perform rework without extensive training and quality assurance oversight.

In many cases where screening introduces an increased and unacceptable risk, additional qualification steps/samples must be introduced to offset a diminished screening procedure. Many screens inappropriate at the component level could occur at higher assembly screening steps.

The balance of cost vs. risk is a major calculation. Pushing risk onto subsequent assembly levels can be extremely costly if failures do occur. However, waiting years for a new device development and qualification is a huge risk if the new technology development proves unsuccessful.

## 9.0 LOT QUALIFICATION

Beyond 100% screening of RF flight lot components, an additional sample-based qualification should be performed. Qualification tests should be performed on flight lot devices that have passed screening. Many qualification tests are destructive, which prevent the samples from being used as flight devices. The qualification tests provide confidence the screening steps effectively removed infant mortality failures from the flight lot. The higher the number of samples; the higher the statistical confidence achieved. Higher mission classes, which typically do not allow deviation from space requirements, require a significant number of qualification samples. Lower mission classes, like the ones that allow for the deviations listed above, allow for a lower qualification confidence. Sample quantities and cost need to be factored into qualification plans. Many qualification tests do not have the significance or relevance to justify higher costs/higher destructive sample numbers.

### 9.1 Qualification tests

Qualification tests are typically subdivided into four groups: A, B, C, and D. Group A RF electrical tests include lot specific dc measurements, s-parameter measurements over bandwidth, and pulsed power measurements. Each of these measurements should occur at three different operating temperature points: room, the highest rated maximum, and the lowest rated minimum temperature. Group B package tests include lot specific inspections that verify uniform construction to design requirements, consistency in lot processing, and the robustness/survivability of the flight device. Important Group B tests include extended temperature cycling and life-testing.

Group C periodic life-tests and Group D package tests are periodically performed and are typically repeated tests from Group B. These tests are not specific to particular lots, but rather they are specific to a manufacturing line using defined assembly/testing processes.

Higher level mission requirements require all qualification groups on all flight lots. Lower level missions do not. It is, however, vital that all qualification groups be performed on commercial-grade devices when initially up-screened for space. A careful analysis must be performed on these commercial-grade RF devices to ensure qualification tests are performed as intended under the correct conditions. Overstressing RF devices during qualification could produce sample failures with erroneous results. The entire flight lot could be rejected unnecessarily due to these failures.

## 10.0 JASON-3 CASE STUDY OVERVIEW

Previous flight projects using bare die have faced issues with component-level burn-in because bare die cannot be burned-in prior to integration onto the flight assembly. This is a particularly crucial issue if the dice are installed on multiple component assemblies such as a radar receiver channel. If a defective die is detected during assembly testing the entire receiver would have to be scraped and the assembly process would have to start from the beginning. A possible solution for this problem is to integrate the die onto smaller carriers with a smaller circuit subset of the entire subsystem. This would allow the die to be burned-in and electrically tested prior to system integration thus reducing the likelihood of a downstream failure.

The JASON-3 project (AMR RF subsystem) established a new set of requirements for a RF subsystem with one receiver unit (three frequency channels) and one noise source. Both the receiver unit and noise source units would be redundant and connected to the instrument antenna via waveguides. The three receiver channels included a 23.8 GHz, 18.7 GHz, and 34 GHz channel. Prototype development of the AMR RF subsystem concluded a new flight design would have to be procured, manufactured, and assembled (older flight builds did not meet system requirements). Due to design, schedule, and budget constraints this effort would be performed by a team internal to JPL.

During the flight model design, it was determined that typical JPL part requirements would delay the manufacturing and testing of the AMR subsystem. The project could not delay the build cycle to match with needed lead times to procure space-grade components for the subsystem. Instead of purchasing fully screened, tested, and packaged components, the project elected to purchase commercial-level die and mount the circuit on a non-hermetic carrier. Element evaluation would be performed on each of the flight die lots either by the manufacturer or JPL. Screening would occur at the subsystem level (carrier level). This screening would include assembly temperature cycling, DC biased burn-in of each die, and circuit-level RF performance tests while monitoring shifts in the individual DC biases of each active device.

The AMR RF subsystem would use RF hybrid manufacturing techniques. The hybrids would be non-hermetic. The signal chains for the various receiver channels and noise source would be attached to multiple “carrier” units. These carrier units could be screened separately and then assembled onto the subsystem “chassis.” This multicarrier approach allowed for the removal and replacement of individual carriers if an infant mortality failure was detected during the RF subassembly testing. The carrier could be immediately replaced by a spare flight carrier that was processed side-by-side with the original flight carrier. This would allow the testing of the integrated chassis to continue with minimal delays and test repeats.

Multiple in-process control monitors were established during the assembly and test process to ensure all manufacturing steps met quality requirements. While the assembly processes of the AMR RF subsystem does not fully comply with typical space qualification processes for RF hybrids, the required steps for element evaluation, screening, and in-process controls are in place and mitigate the risk of an infant mortality hardware failure. The collection of these steps is a low risk approach for rapid RF hybrid development, assembly, and test.

### 10.1 Devices used in case study hardware

Six active devices were used in the AMR RF subsystem. The six die were supplied by five manufacturers with varied screening levels. Five of these devices received a subset of a class “K” element evaluation by the device vendor. The UMS CHA3689-99S/00 and the Sumitomo FMM5703X-S samples received burn-in and life-testing; however, no thermal cycling or mechanical tests were performed on samples. The Metelics MBD-1057-C18, Mpulse MP3X8346, and Mpulse MP3X7834 samples received no 1000-hour life-test on the element samples. The M/A-COM MA4AGSW2 was a commercial-level die, so element evaluation was not performed. A SEM metallization exam was performed by JPL on the M/A-COM samples from the dice flight lot.

From Table 10.1-1below, it can be seen that each active device received the equivalent tests listed. These tests were performed by either JPL or the device manufacturer. While these tests were not performed in the typical order, all steps were performed on either bare die or on die after they were assembled onto the flight carriers. The carrier-based testing approached assured 100% of flight die were burned-in at optimal junction temperatures before integration into the RF subassembly chassis.

Table 10.1-1. Planned element tests and inspections for all die (case study).

| Testing / Devices | Element Electrical | Element Visual | Internal Visual | Interim Electrical | Burn-In | Post Burn-In Electrical | Wire Bond Evaluation | SEM |
|---|---|---|---|---|---|---|---|---|
| CHA3689-99S/00 | X | X | X | X | X | X | X | |
| FMM5703X-S | X | X | X | X | X | X | X | |
| MA4AGSW2 | X | X | X | X | X | X | X | X (five devices) |
| MBD-1057-C18 | X | X | X | X | X | X | X | |
| MP3X8346 | X | X | X | X | X | X | X | Per JPL-10268284 |
| MP3X7834 | X | X | X | X | X | X | X | |
| JASON-3/level 2 (min. required) | X | X | X | | | | X | |
| | Performed by manufacturer or at JPL | | Note 3 | | | | Note 4 | Note 5 |

*Notes:*

1. *Parts requirement for JASON-3 are level 2 (EEE-INST-002: Instructions for EEE Parts Selection, Screening, Qualification, and Derating: NASA/TP-2003-212242; Section M2 Microcircuits Hybrid, pages 7 and 80.*
2. *If treated as a hybrid, piece parts are required to meet the class H element evaluation requirements of MIL-PRF-38534. In addition, the MMICs are subjected to the burn-in and life-testing similar to class H requirements.*
3. *To be performed at the assembly level. MMICs have additional burn-in and life-test (procured from vendor was: CHA3689-99S/00 on 10 devices and FMM5703X-S on three devices only) similar to the element evaluation requirements of MIL-PRF-38534, see appendix C3 and section 4.4.1.2.1.Interim electrical tests are on assembly level not individual LNAs.*
4. *Wire bond evaluation should be performed as part of the in-process operator/bonding machine qualification.*
5. *The JPL Failure Analysis lab will perform SEM on die level to verify wafer/metallization thickness.*

Passive devices were also used on the carrier assemblies. Microstrip substrates and filter elements, and isolators were used. Microstrip transmission and filter element lines received element visual inspection during JPL receiving inspection. Electrical testing was performed during carrier integration. Typically, element evaluation electrical inspections are performed prior to installation. The risk of installing electrically nonconforming substrates was considered a low risk. This risk posture allowed the integration to remain on schedule. System-level electrical performance showed the risk tradeoff was acceptable.

The two RF isolators used on the carriers included surface mount isolators procured from Dorado international. Dorado is a commercial company producing commercial-grade isolators. The Dorado isolators had been designed into prototype designs and showed they meet all performance requirements. The JASON-3 project had requested quotes from other hi-rel isolator companies for space-grade surface mount isolators; however, the development and integration time for space-grade isolators proved to be to long for the project assembly schedule.

At this point the project determined the most productive course of action was to up-screen a new lot of the Dorado isolators to a JPL screening specification. The specification included 100% device screening, sample qualification, and additional test at JPL once the flight devices were received. These requirements were documented in JPL SCD 10346661. 100% screening included electrical (insertion loss, isolation, and voltage standing wave ratio [VSWR]) per MIL-DTL-28791 and visual inspections to MIL-STD-883

TM 2032 and 2016. Sample qualification steps included extended visual inspection, stabilization bakes of the materials and devices, electrical testing (identical to screening), temperature cycling per MIL-STD-883 TM 1010, and constant acceleration per MIL-STD-883 TM 2001.

Once again, the risk of not performing the 100% temperature cycling and constants acceleration screens on all of the flight isolators was considered. This risk was determined to be acceptable due to the fact that all flight isolators would be thermal cycled at the carrier-level prior to installation into the AMR instrument and all isolators would receive 100% centrifuge testing (3000g) at JPL after delivery. The delays by having the manufacturer perform these screens were unacceptable to the project. The project also had no way of ensuring the commercial manufacturer would follow necessary procedures for temperature cycling and constants acceleration screens. Final electrical measurements at the carrier level would indicate if infant mortality failures were occurring. If failures did occur, the entire carrier (see Figure 10.1-1) could be swapped out for a fully screened spare.

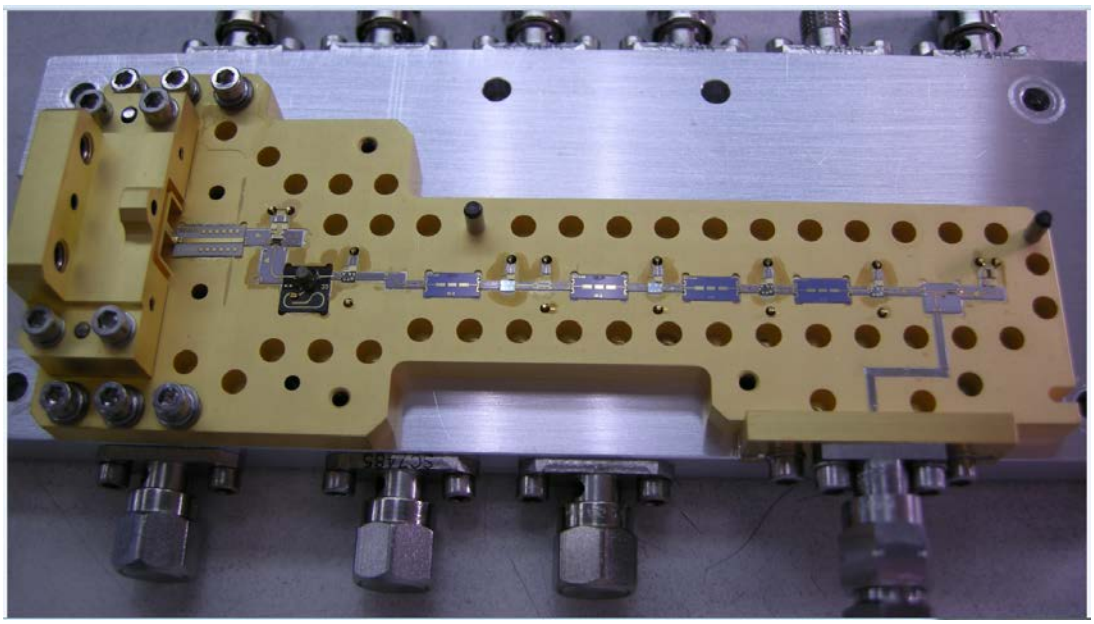

Figure 10.1-1. Carrier mounted to chassis.

## 10.2 Integration

"The RF electronics subsystem is comprised of two assemblies, the Receiver and the Noise Source. Both units have RF circuits, which are assembled with bare die and inter-connections with ribbon or wire bonding to substrates. The RF parts are separated by an H-frame chassis design. With electrical feedthrus, the RF components are DC biased. The DC bias conditioning electronics are assembled onto PCB boards with standard SMD components" [Maiwald]. In this discussion, the paper will focus on the assembly of the two receiver carriers.

Two carrier varieties were assembled for the JASON-3 project. These carriers where then integrated into the AMR instrument chassis alongside the noise source. The first carrier, specified in JPL drawing 10342440 (Figure 10.2-1), was an 18/24 GHz receiver chain containing two channels separated by the MMIC switch. Each channel was constructed with a low pass filter, low noise amplifier, passive elements, and waveguide/termination substrates. The receiver input port was buffered by the broadband surface mount isolator.

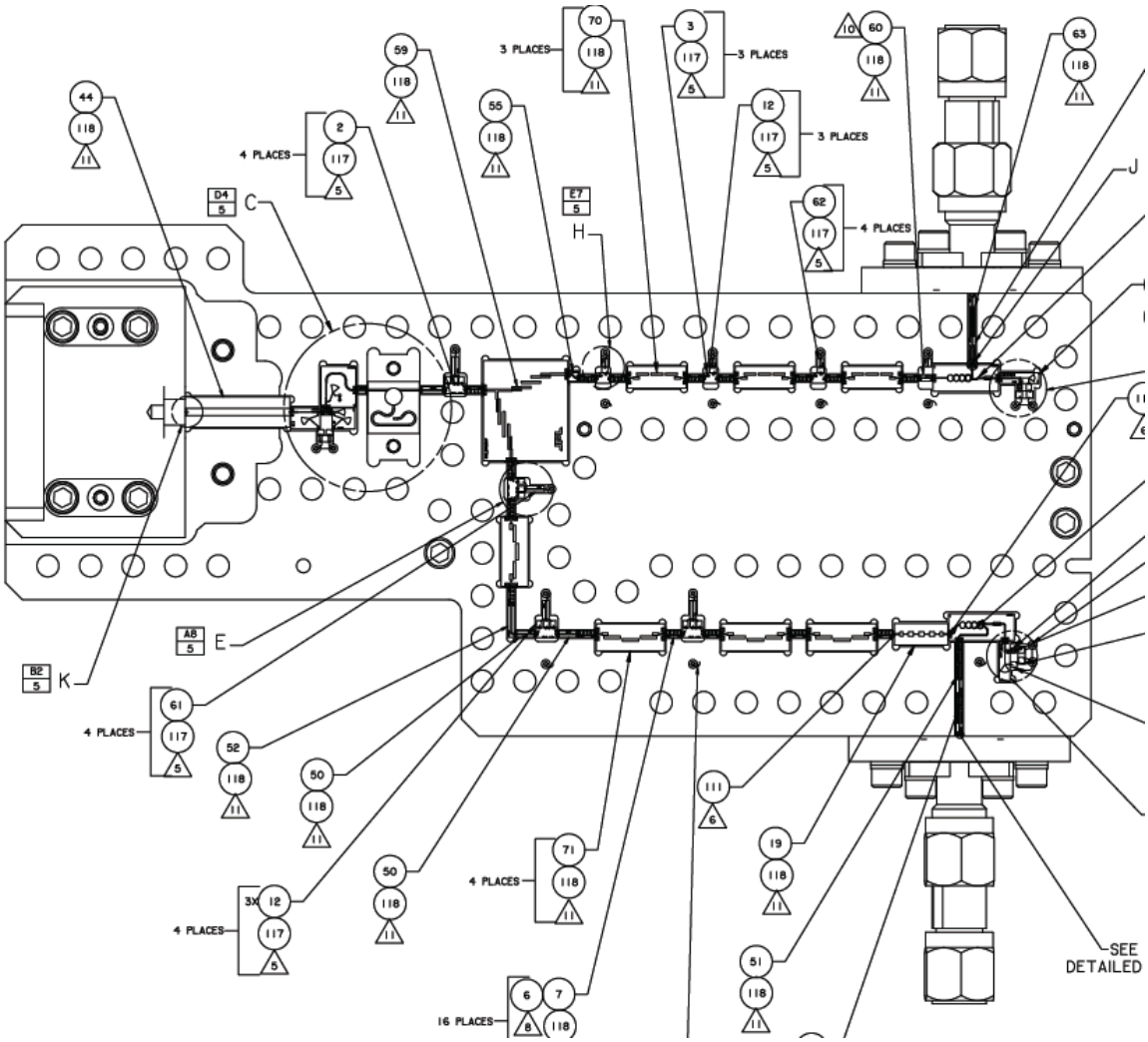


Figure 10.2-1. 18/24 GHz carrier.

The second carrier, specified in JPL drawing 10342430 (Figure 10.2-2), was a 34 GHz receiver chain containing one channel. This channel was constructed again with a low pass filter, low noise amplifier, passive elements, and waveguide/termination substrates. The receiver input port was buffered by a different surface mount isolator (tuned to 34GHz).

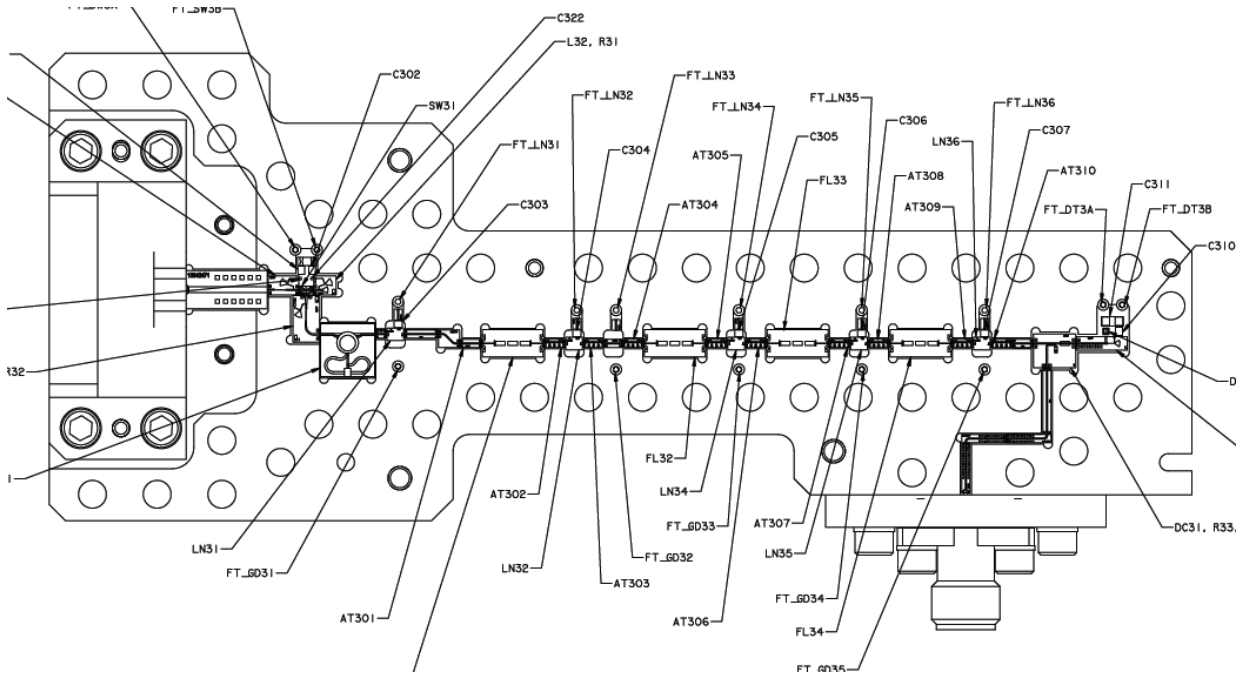


Figure 10.2-2. 34 GHz carrier.

Initially, all carriers were plated and cleaned. In-process monitors for the plating and cleaning steps included high temperature bake and water break test. After successful cleaning, the substrate, passives, and die were bonded on to the carriers with silver epoxy. A 125°C bake was required after bonding to cure the epoxy. All bonds were visually inspected.

The next step required all RF signal chains were bonded together. All RF connections between substrates were initially connected. This step included the preheating of the carrier to 120°C and ribbon bonding the transmission paths. Once the substrates were ribbon bonded, all DC feedthrus and DC boards were attached. DC feedthrus were epoxied with a 125°C cure. The DC boards were attached with Sn63 solder at a temperature of 210°C. This high soldering temperature did not affect previous bonding because the 210°C heat was localized to the feedthrus. Finally, the MMIC die were ribbon bonded and tuned at a temperature of 120°C. In-process pull testing was performed on coupons bonded just prior bonding of the flight carriers.

After bonding, all carriers entered a temperature cycling/rework iteration. The carriers were first temperature cycled to a defined thermal profile. If the devices failed subsequent RF testing, rework was required to replace the failed component(s). After rework, the carriers would once again receive temperature cycling to the defined profile followed by RF testing. The maximum number of rework/temperature cycles was limited to three iterations.

At this point, in-process shear testing (for die) and visual/pull tests (for substrates) were performed on test coupons assembled and temperature cycled alongside of the flight carriers. In-process pull testing also occurred on coupons that also received thermal cycling.

Then a 240-hour carrier burn-in was performed. RF testing was also performed on the carriers prior to and post the burn-in. Both the burn-in and RF testing will be described below.

Next, the surface mount isolators were mounted to the carriers. Visual inspection was used to ensure the isolators were properly bonded to the carriers. Further RF measurements (noise figure and gain) occurred during chassis temperature cycling on the next level of integration to ensure proper isolator installation. An example of this can be seen in Figure 10.2-3.

Further explanation of these carrier screens and in-process inspections are discussed below. In addition to the screening and in-process monitors, 500 hours of accumulated operation occurred for the carriers either prior or post integration into the AMR instrument chassis.

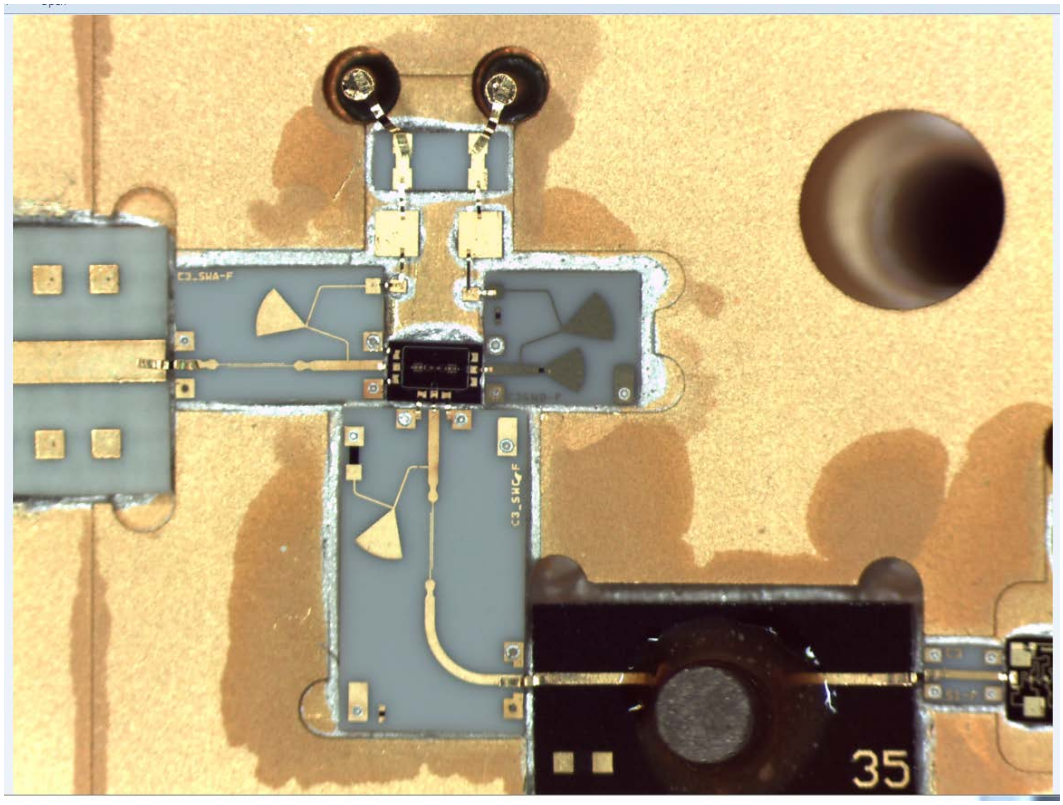


Figure 10.2-3. Isolator and switch bonded on carrier.

In total eight carriers were constructed. The inventory is documented below in Table 10.2-1. All carriers passed the listed inspections without issue. At this point all carriers were ready for system-level integration into the AMR instrument chassis. Carriers passing screening but unused on the flight chassis were retained as flight spares.

Table 10.2-1. Carrier assembly list.

| Carrier Type | Serial Number | Part Number | Where Installed |
|---|---|---|---|
| 34 GHz | 001 | 10342430-2 | Receiver 101 |
| 34 GHz | 002 | 10342430-2 | Receiver 102 |
| 34 GHz | 003 | 10342430-2 | Flight spare |
| 34 GHz | 004 | 10342430-2 | Receiver 103 |
| 18/24 GHz | 001 | 10342440-2 | Receiver 102 |
| 18/24 GHz | 002 | 10342440-2 | Receiver 101 |
| 18/24 GHz | 003 | 10342440-2 | Flight spare |
| 18/24 GHz | 004 | 10342440-2 | Receiver 103 |

## 10.3 Carrier Screening and Qualifications

Beyond element elevation each active RF device received additional carrier-level screening. This screening was defined in the JASON-3 project document J3_D-68339. The document contains the non-standard device screening requirements for the JASON-3 AMR instrument. The document was authored by the project qualification team and reviewed by Mission Assurance. The JPL team included the project

RF Electronics Lead Engineer, Instrument Manager, Mission Assurance Manager, and Mission Assurance RF part specialist. The qualification team's purpose was to ensure the plan properly applied element evaluation, on-board screening, in-process testing, and sample qualification, ensuring infant mortality-free RF carriers were manufactured for assembly onto the RF instrument chassis. The result (testing and manufacturing) of this effort is captured in three summary IOMs. These IOMs list all of the milestone events in each carrier's delivery.

Three major screens were performed and monitored by the qualification team. These screens included carrier temperature cycling, carrier burn-in, and carrier RF testing.

The carrier temperature cycling profile included three cycles from +125°C to 0°C and three sets of 10 cycles from +25°C to −60°C. The initial three temperature cycles transversed the assembly and rework temperatures achieved during bake-out and curing steps. The later three sets of temperature cycles encompassed the proto-flight temperature ranges the AMR instrument would receive during higher levels of integration. The combined temperature cycling profile was designed to ensure the flight carriers and test coupons were capable of withstanding all the multiple iterations of thermal stress it would encounter during assembly, integration, and test.

All active die received a burn-in for 240 hours at 106°C baseplate temperature. Each active die was DC forward biased to optimize the maximum junction temperature during burn-in. This approach allowed each device to receive the maximum number of equivalent hours of operation while still operating each device within manufacturer's limits. It just happened that all the die manufacturers recommended the maximum junction temperatures to be 125°C. See Table 10.2-1 below. Because each device had a different thermal resistance, analysis was perform to calculated the required DC bias to generate the need temperature rise above the 106°C baseplate temperature to achieve the 125°C junction temperature. In addition, the M/A-COM switch was cycled with a 50% duty cycle, during burn-in, to ensure each diode branch received equal burn-in.

Also, a parallel 1000-hour life-test was performed on spare carrier assemblies. The parallel life-test was performed on hardware processed concurrently with flight hardware. Typically, the life-test is performed post burn-in to verify successful screening; however, in this case additional carrier units received additional hours of identical burn-in conditions. The parallel approach was used to lower risk while still allowing to the project to meet delivery dates.

Table 10.3-1. Active devices used on carriers.

| Raw Part Number | w/Class K Element Eval. | Comments | Manufacturer Max. Junction Temperature per Datasheet in C | Actual Burn-In Junction Temperature per Manufacturer Flow in C |
|---|---|---|---|---|
| CHA3689-99S/00 | CHA3689-99S/00 | UMS class K element evaluation | 175 | UMS typical class K flow does burn-in at 125°C |
| FMM5703X-S | FMM5703X-S | Sumitomo class K element evaluation | 125 | |
| MA4AGSW2 | N/A | No element evaluation performed | 125 | |
| MBD-1057-C18 | M1X1564 | Metelics class K flow | 110 | Manufacturer approved burn-in at 125°C. |
| MP3X8346 | 10268284-003 | Mpulse to screen SCD | 150 | Mpulse qual flow shows burn-in at 125°C. |
| MP3X7834 | SOW 3V023 | class K element evaluation | 150 | Mpulse qual flow shows burn-in at 125°C. |

Electrical parameters were monitored during burn-in, as well as during pre and post burn-in electrical testing for both receiver carriers. Bias currents were monitored on all amplifiers during burn-in. Bias

voltage was monitored across the MMIC switch during burn-in. A ±10% variation in the bias current or voltage was considered a carrier failure.

Pre and post electrical measurements for the carriers included gain of the entire receiver channel and the noise figure of the first amplifier in the channel. A ±1dB shift in gain or noise figure was considered a carrier electrical failure.

In-process control monitors were defined for each major element on the RF carriers. These elements include substrates, substrate coupons, components, and wire bonds. The tests for these elements included checks for plating, cleaning, substrate attach, die attach, wire/ribbon pull, and soldering checks.

Plating tests included crosssections, tape test, and a high-temperature bake. Cleaning inspections included a water break test. The substrate attach test focused on destructive shear test (coupons), 100% visual for the filet, and ultrasound inspection. Die attached methodologies were tested with coupon die shear. Destructive wire/ribbon bond tests were performed on coupon bonds. Soldering inspections included 100% visual inspection on all filets and RF leads. Standard JPL, MIL-STD-883, or ASTM test methods were used.

Thermal cycling was also performed on qualification carrier coupons prior to die and substrate shear testing. The thermal cycling was modeled on the same three solder reflow assembly and rework cycles followed by two sets of 15 temperature cycles of the proto-flight temperature range. The temperature cycling profile proved carriers were capable of assembly, two rework cycles, and twice the required proto-flight testing scheme (Note: flight hardware only received one proto-flight cycle). The flow of was defined by Figure 10.3-1.

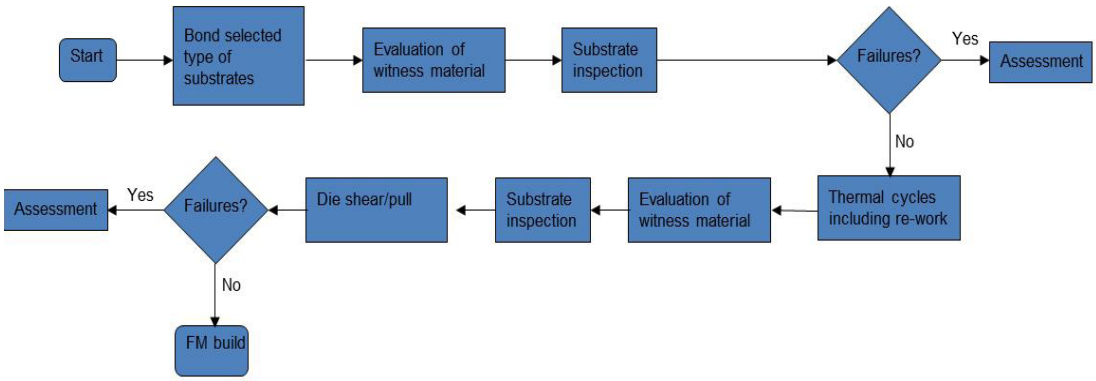


Figure 10.3-1. Carrier Production Flow

The case study mentioned above proved to be a successful approach to integrating unscreened die into a flight RF subsystem while reducing risk and schedule impacts. The approach used in the case study allowed the project to deliver the AMR hardware without schedule delays. If traditional component-level screening and qualification was used, a 12-month delay could have been expected.

The case study is not the only method to achieve similar results; however, this approach (plan and implementation) definitely shows promise for future flight builds. Other die-level and component-level tests and screens, as mentioned above, could also be incorporated into a future screening plan to mitigate risks associated with hardware used on the new flight design.

## 11.0 CONCLUSIONS

This paper discussed possible screening methods a flight project could use to mitigate risk of a downstream RF component failure during a RF subsystem built while still maintaining a strict delivery schedule. The discussion included a summary of RF device and screening issues JPL encounters, devices JPL has up-screened for space, methodologies to screen die, packaged components, and RF assemblies. Industry standards for manufacturing, packaging, screening, and qualification were also covered. Finally, a case study was presented that demonstrated JPL's ability to balance needed screens at various implementation phases. The case study discussed an alternative approach to standard space component qualification. The alternative approach allowed hardware to be delivered on schedule.

Modification to screening/qualification plans many not always be acceptable for a project. It is up to the project management, engineers, and mission assurance to ensure a balanced approach is carefully planned and implemented so that infant mortality failure risks are reduced and schedule milestones are achieved. The best approach is to procure screened hardware for integration into an RF subsystem. Screening does not necessarily mean burn-in; however, burn-in and electrical testing are the most effective screens.

Additional screening on individual components will increase development costs; however, the cost of a system-level failure could be orders of magnitude higher. Schedule delays at the component level/lower levels of integration will also be minor when compared to delays of system-level failures. Troubleshooting, itself, would be greatly reduced if it occurs at the component/carrier level rather than occurring at the subsystem level.

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