Effects of Temperature Cycling on the Signal Integrity of CompactPCI® Connectors

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1. INTRODUCTION

Today CompactPCI® (cPCI) connectors have several critical applications in space flight hardware. One example of such application is the use of these connectors on several single board computers (SBC) like the one shown in Figure 1 below. These SBCs support input and output interface to multiple I/O devices. They also provide supporting functions to control local memory and several other tasks needed to ensure precise functionality of an instrument or spacecraft. Commercial CompactPCI® connectors generally employ standard manufacturing practices which makes them unreliable for space flight applications. Factors such as plating thickness, contact fretting and pin retention force lower than the 100- gram-force required to wipe away surface contamination has lead to the development of a hi-rel Compact PCI® connector such as the Hypertronics cPCI connector.

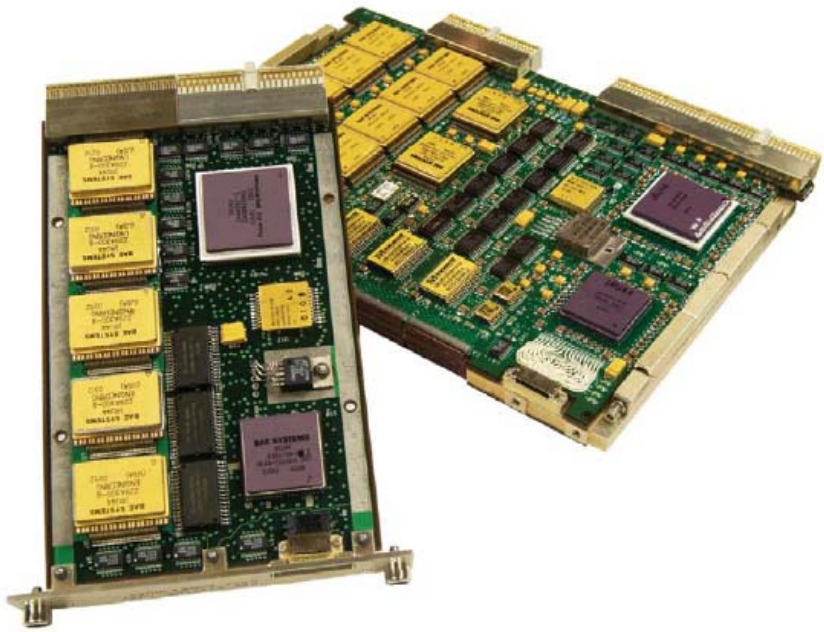

Figure 1: BAE RAD750 Single Board Computers with CompactPCI® connectors.

Nevertheless, failures due to connector degradation will eventually occur with time. Mechanical and thermal vibrations are two environmental factors that affect the long term reliability of CompactPCI® connectors. Commercial CompactPCI® connectors were designed for use in the telecommunication and data communication industries, where temperature variations are minimal, and the mechanical vibration are far less than those experienced during a spacecraft launch.[1] During a typical spacecraft launch, the bulk of the mechanical vibrations are experienced by the instrument during lift off. Once in orbit, pure mechanical vibration becomes weak and almost non-existent. However, the observatory is exposed to various temperature cycles during its useful life in orbit. These temperature extremes vary widely depending on the mission orbit of the instrument and are one of several key factors of component fatigue in space.

For most CompactPCI® connectors, component fatigue would typically manifest as intermittent variations in resistance which are normally indicative of contact fretting. Fretting of CompactPCI® connector pins occurs when plating thickness of mated connector pairs are worn down due to repetitive mechanical vibration or thermal cycling. Although Printed Circuit Boards or daughter cards used for space flight applications are locked in place with an edge card wedge lock and housed in an aluminum chassis to restrict the movements of such components, this precaution is mostly effective in reducing wear and damage due to mechanical vibration. Given enough time the thermal expansion process experienced by the observatory in the harsh environment of space could indirectly affect the long term reliability of CompactPCI® connectors used onboard the instrument. Depending on the frequency of the expansions and cooling process, fretting could occur between pins of mated CompactPCI® connector after a few thousand temperature cycles. This would certainly lead to intermittency of the connector if used for long term space flight applications.

The Hypertronics cPCI connector design employs a Hypertac® technology, an advanced hyperboloid contact design with 50 micro inches gold plating over a 50 micro inches nickel under layer. As gold is a noble metal and does not form corrosion product films, pin corrosion will not occur prior to wear through of the gold coating[2]. The Hypertac® technology utilizes a hyperbolic arrangement of wires to elastically form multiple points of contact around the pin thus increasing the amount of surface contact between the pin and socket as shown in Figure 2. On the other hand, most commercial CompactPCI® connector designs exploit the use of bifurcated socket tines to provide two points of contact between the pin and socket. The Z-PACK series connector manufactured by AMP/Tyco electronics is an example of such connector with (30 µin/50 µin) gold over nickel contact plating. Although these contact points appear to be flat when viewed with the naked eyes or with a low magnification scope, in reality these surfaces are never entirely smooth. Several peaks exist along both surfaces that actually make contact, thus the area of real contact is usually significantly smaller than the apparent contact area.

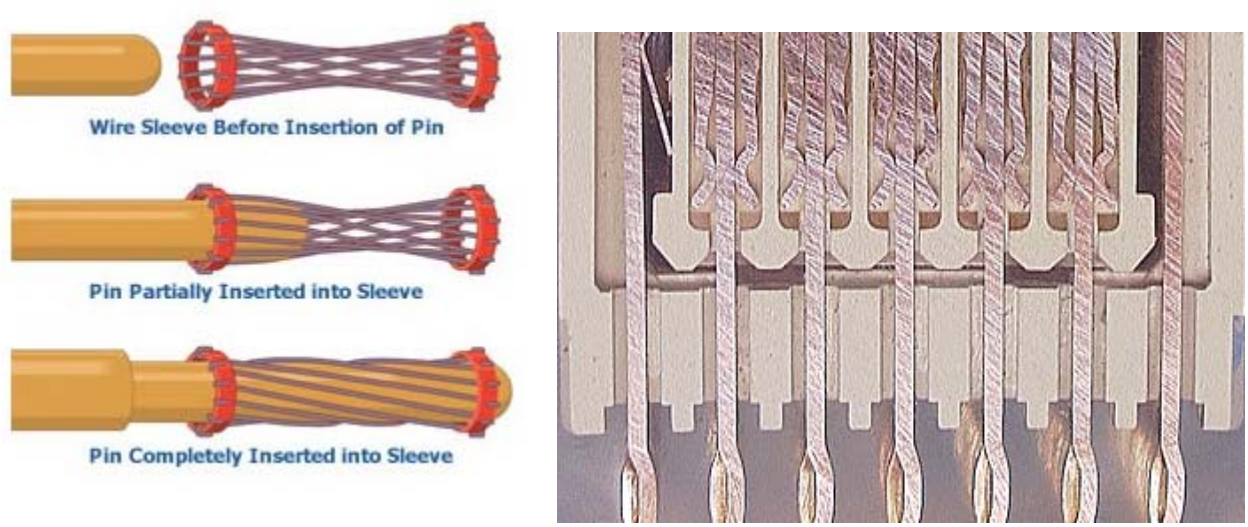

Figure 2: Mating process for the Hypertronics (Left) and AMP CompactPCI® connector (Right)

Nevertheless, the small size and radii of these real contact points would undergo plastic deformation until an area sufficient enough to support the contact load is achieved[3]. Furthermore, although the normal force determines the size of the contact area for both CompactPCI® connectors, the geometry of the mating surface determines how the contact areas are distributed. This gives the Hypertronics cPCI connector a superior advantage over most commercial CompactPCI® connectors and makes it less susceptible to intermittencies caused by mechanical vibrations. The bifurcated socket tines design of the commercial CompactPCI® connector makes it prone to open circuit failure if one tine becomes bent due to severe vibration. This would leave the pin with only one contact surface with the socket which would eventually succumb to fretting wear if used for a long period of time. Such connection would be constantly plagued with intermittent faults and a high probability of an open circuit failure. In addition, most commercial CompactPCI® connectors require proper tooling and training to successfully press-fit the compliant pins into a printed wiring board. One problem with this method of termination is if the compliant pin is bent during the press fitting process, both the board and connector are rendered useless and must be discarded. For a project this could mean more cost for rework and a possible impact to delivery schedule. Now, unlike most commercial CompactPCI® connectors the Hypertronics cPCI connector was designed to meet NASA's outgassing and solderabilty requirements. The S-311-P-822A specification also establishes the general requirements for connectors that utilize the Hypertac® contact system. These connectors are designed to perform reliably in severe environments and with the absence of pure tin, the issue of tin whisker growth is completely eliminated.

As the need for faster data processing rate increases, nanosecond intermittencies become a more prominent threat to these high speed systems. As such, it is important to understand the limitations of existing CompactPCI® connectors used for space flight applications. Although the Hypertronics cPCI connector is the connector of choice for the space industry, commercial CompactPCI® connectors sometimes make their way into flight hardware, usually by means of heritage design. An example of such instance is the RAD6000 single board computer that was used on the spacecraft for the Aeronomy of Ice in the Mesosphere (AIM) mission. Generally, the cost of rework to change a heritage design and the impact to schedule might not always be practical for a project, however necessary precaution should be exercised to prevent known failure mechanisms in heritage parts. This test would simulate and observe the effect of thermal stress on the long term electrical reliability of both the Hypertronics and AMP CompactPCI® connectors.

2. TEST OBJECTIVE

The objective of this test is to monitor the Amp CompactPCI® and the Hypertronics cPCI for any electrical intermittency that could occur due contact degradation of connector pins. As this

test would simulate the use of CompactPCI® connectors in orbit, it will focus primarily on the effect of temperature cycling on the electrical performance of these connectors. Printed circuit boards (PCB) designed for spacecraft digital electronics are normally housed in an aluminum chassis. The chassis holds the PCBs in place and provides a structural support which restricts the movement of the PCB due to vibration at launch. Similarly, this test also accounts for a locking mechanism to hold the daughter card to the backplane. As chassis design widely varies among designers, a simple but unique clamping mechanism was implemented to represent the function of the chassis in this test as shown Figure 3. The thermal chamber, materials and dimensions of the card locking mechanism were also chosen to induce a relative micro-movement between the mated CompactPCI® connectors of the daughter card and the motherboard.

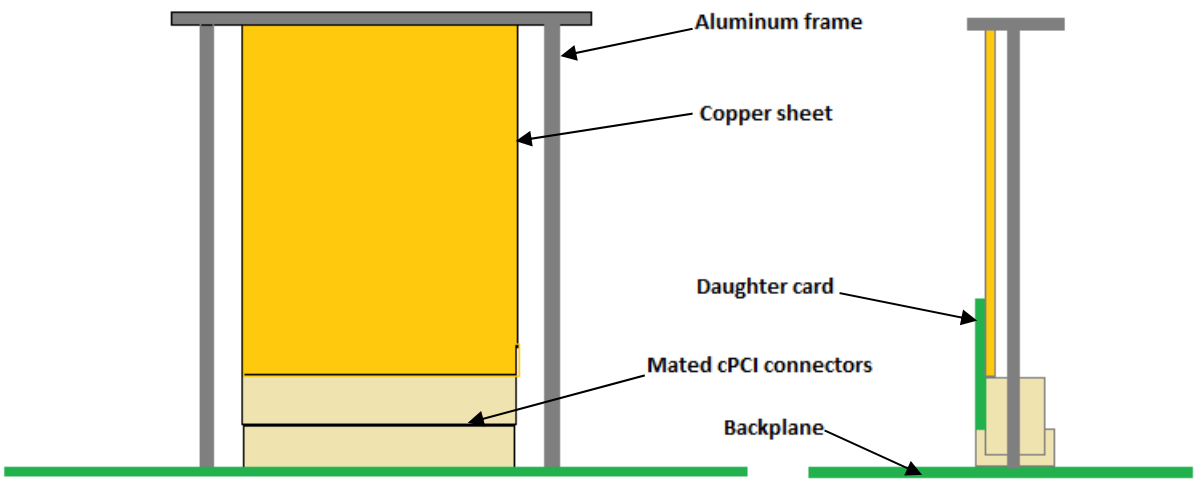

Figure 3: Front and side view of the locking mechanism holding the daughter card to the motherboard.

To calculate how far the connector pins are displaced from their original mated point, let's assume initial distance between the tip of the mated pin and socket is X. The final displacement as a result of heat expansion would be $X + \sum \Delta L$.

The coefficient of thermal expansion (CTE) of a given material is calculated as follows:

$$\text{CTE} = \alpha = \frac{1}{L}\frac{dL}{dT} \quad \text{where L is the length of the material.}$$

The dimensions of the daughter cards were chosen so that the thermal chamber can hold multiple test samples. As a result, copper sheets were attached to the daughter card to compensate for the CTE of a larger and more realistic daughter card.

CTE of Aluminum (Al) ≈ 23 ppm/°C

CTE of Copper (Cu) ≈ 17 ppm/°C

$\Delta L = \alpha \times L \times \Delta T$, where T = temperature and L = length

$$\sum \Delta L = \Delta L_{\text{copper in cPCI pin}} - \Delta L_{\text{copper in cPCI socket}} - \Delta L_{\text{copper sheet}} + \Delta L_{\text{Aluminum frame}}$$

$$= [(\alpha_{Cu} \times L_{\text{copper in cPCI pin}}) - (\alpha_{Cu} \times L_{\text{copper in cPCI socket}}) - (\alpha_{Cu} \times L_{\text{copper sheet}}) + (\alpha_{Al} \times L_{\text{copper in cPCI pin}})]\ \Delta T$$

$$= [(17\text{ppm/°C} \times 0.95\text{cm}) - (17\text{ppm/°C} \times 0.8\text{cm}) - (17\text{ppm/°C} \times 8.86\text{cm}) + (23\text{ppm/°C} \times 10.12\text{cm})]\ 90°\text{ C}$$

$$= [0.16\ \mu\text{m/°C} - 13.6\ \mu\text{m/°C} - 150.62\ \mu\text{m/°C} + 232.76\ \mu\text{m/°C}]\ 90°\text{ C}$$

$$\sum \Delta L = 76.5\ \mu\text{m}$$

The configuration of the edge card wedge locking mechanism is such that a relative movement of about 77 µm is achieved between the contact surface of the connector pin and socket. One might suggest that brief intermittent discontinuity in a CompactPCI® connector could be easily detected by daisy chaining the connectors in series, applying a signal and monitoring for an open circuit using a volt meter. This method of detection would be ideal if the duration of discontinuity is large enough to be detected by the sampling circuitry of the meter. Although most tests require an intermittency duration sensitivity of 1 microsecond[4], as the duration of the electrical discontinuity decreases, the less likely it is for a conventional meter to detect an Event. In this test, connection from the test specimen to the event detector is achieved by soldering wires from the termination trace on backplane to a set of D-sub connectors outside the thermal chamber which interfaces directly with the event detector. Installing the D-sub connectors directly on the backplane would effectively eliminate the CompactPCI® connectors under test as the only source of intermittent fault. Thus the ambiguity involved with determining the source of intermittent fault between the D-sub and the CompactPCI® connectors could complicate data analysis of results from test.

3. INSTRUMENTATION

A total of four daughter cards and motherboards were used in this test. Each motherboard was populated with a single 110 pin male CompactPCI® connector in the center of the board. Table 1

below shows the mating arrangement and operations needed to attach the connector to the printed wiring board. The motherboards were designed to connect to the event detector without daisy chaining the cPCI connector pins so that independent pin to pin resistance monitoring is possible.

Table 1 Configuration of cPCI connectors on PWBs

Serial No.	Manufacturer	Backplane connector part number	Daughter card connector part number	Connector to board termination
H1	Hypertronics	K2A110FFDTABH DC: 0530	K2A110FMDTBH DC: 0525	Solder
H2	Hypertronics	K2A110FFDTABH DC: 0530	K2A110FMDTBH DC: 0502	Solder
A1	Tyco/AMP	188834-1	352068-1	Press fit
A2	Tyco/AMP	188834-1	352068-1	Press fit

The event detector designed by Analysis Tech also provides real time data acquisition software for failure analysis of the resulting test data. By measuring the total resistance of the circuit under test and applying a constant DC current source through the CompactPCI® connectors, a known threshold voltage (V_{th}) could be set to detect any intermittent burst of high resistance on any monitored pin. Figure 4 shows a simple schematic of the test setup using a positive temperature coefficient thermistor (PTC) as the device under test (DUT). As the temperature in the thermal chamber increases so does the resistance of the PTC thermistor. The event detector eventually registers a failure once the resistance of the PTC thermistor reaches a preset threshold.

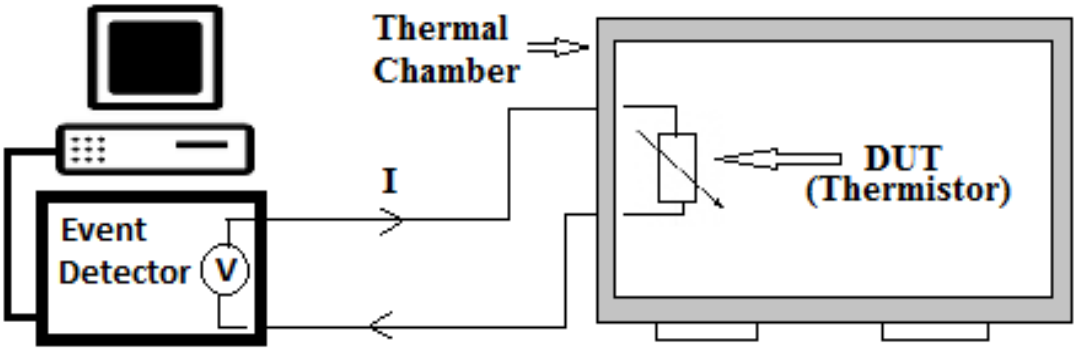

Figure 4: A simple illustration of the test set up.

The threshold voltage is determined using this formula $V_{th} = I\ (R_1 + \Delta R)$ where I is a constant DC current source supplied by the event detector, R_1 is the loop resistance of the circuit

including wires, connector resistance and PWB copper trace resistance . ΔR is a delta resistance threshold value for setting the threshold voltage. Besides the ability to monitor 128 channels simultaneously, the duration sensitivity of the event detector should be set to maximum sensitivity. In this state, the detector can detect events with duration as low as 100 nanoseconds. Lastly, a thermal chamber capable of housing all four boards would cycle the CompactPCI® connectors using a set temperature profile.

Figure 5: Test configuration and setup.

4. TEST PROCEDURE

The Analysis Tech™ Model 105 Series Event Detector was calibrated for functionality and accuracy per the manufacturer's operation manual, before the beginning of the test. Two commercial CompactPCI® connectors were then carefully press fitted with proper tooling into their respective test boards. In order to maintain consistency during the press fitting operation, a torque gauge was used to measure the force required to successfully press-fit the CompactPCI® connector into its compliant holes. The logic behind this press-fitting technique is that if the force required to successfully press-fit a CompactPCI® connector to a PWB is 110 lbf, any deviation from that force would indicate a problem with the CompactPCI® connector. A higher press-fitting force is normally indicative of a bent pin while a lower press-fitting force might suggest a wider compliant hole. Either way it is a good practice to measure the force required for this operation and inspect the backside of the PWB for pin penetration or cracks around the compliant hole. The Hypertronics connectors are manually soldered to the printed wiring boards termination and an external visual examination is performed on all CompactPCI® connectors for possible defects such as cracks, bent pins or evidence of pin corrosion. Figure 6b shows a Hypertronics connector which was discarded since it was missing a few termination pins.

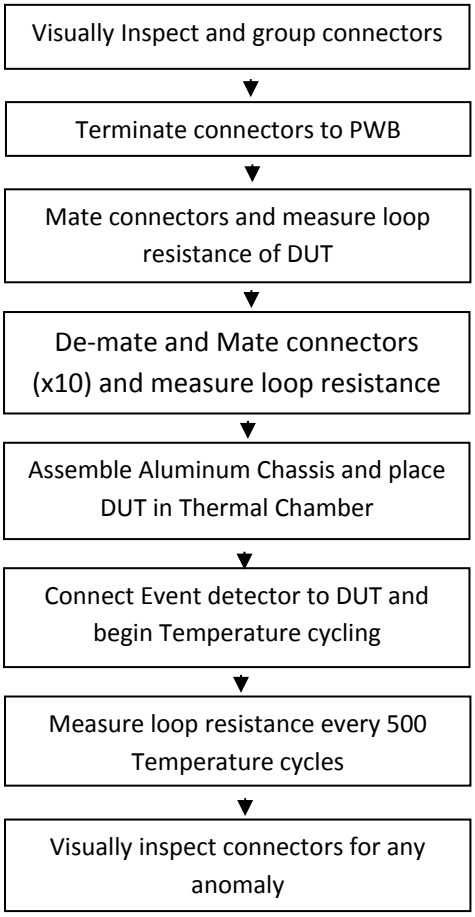

Figure 6a: Flow diagram of test procedure.

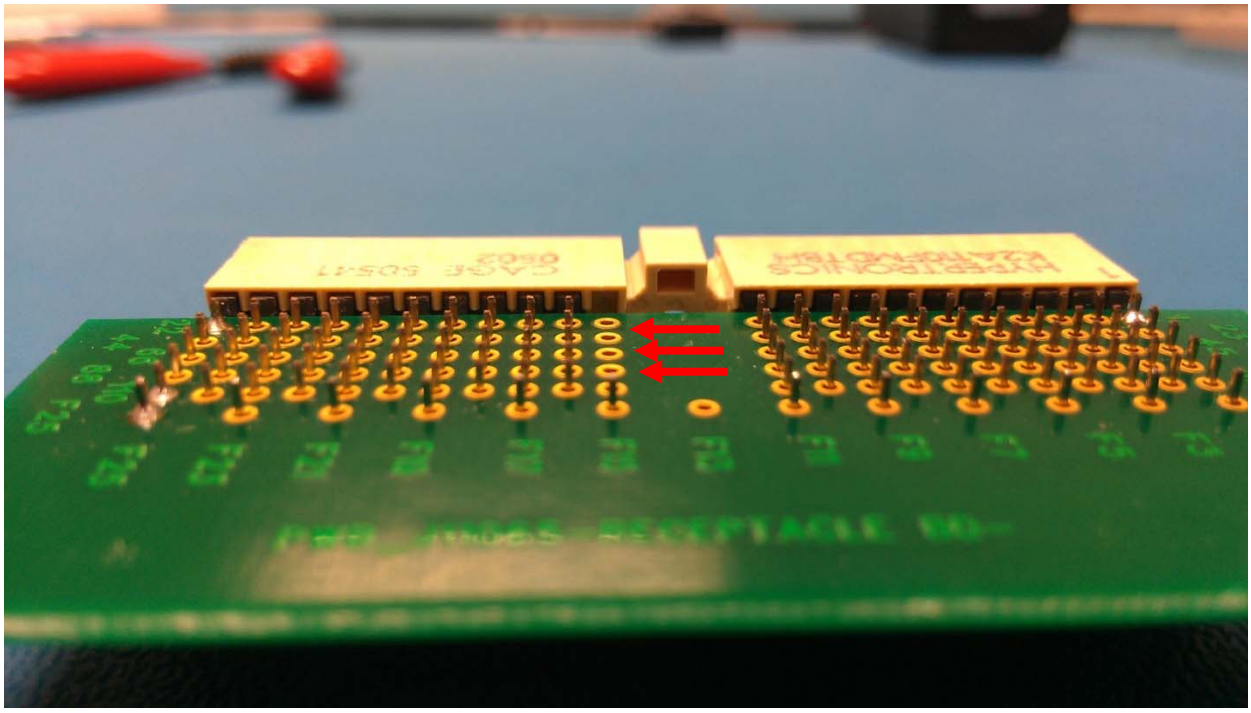

Figure 6b: Visual inspection of Hypertronics connector shows missing terminating pins

After a thorough visual examination, the CompactPCI® connectors are grouped into pairs (one male connector mated with one female connector) and labeled with serial numbers so that it can be recorded which two connectors form a mated pair. The DC resistance of the 110 pin connector is measured and recorded at room temperature. The CompactPCI® connectors are then mated and de-mated 10 times to simulate minimal use before proceeding with the test. Connector savers are normally used on flight connectors to prevent premature wear down of connector pin during several mate and de-mate cycles in ground testing. After the 10 mate and de-mate cycles the connector's DC resistance was measured again to see if the mate and de-mate process caused any increase in pin resistance. Next the generic edge card wedge locking mechanism is installed to hold daughter card to the backplane. After installing all four card locks, the total loop resistance of the circuit is measured and recorded. The boards are evenly spaced with aluminum spacers and placed in a thermal chamber for temperature cycling using the temperature profile in Table 2.

Table 2 Thermal chamber temperature profile

Temp Range	-20°C to 70°C
Transfer Time	18 minutes
Dwell Time	10 minutes
# of Cycles	2000

For a typical spacecraft design, component operating and survival temperatures differ among various sub-systems. The operating range of most digital electronic systems, for example, fall between 0 to 50 °C while the solar panels fall within the range of -100°C to 125°C. The temperature range selected for this evaluation was based on the survival temperature of most spacecraft digital and analog electronics. The threshold voltage of the event detector is set using the equation $V_{th} = I\ (R_1 + \Delta R)$. Where I is a constant 100 mA DC current, ΔR is the delta resistance threshold and R_1 is the measured loop resistance of the circuit and the 110 pin CompactPCI® connector under test.

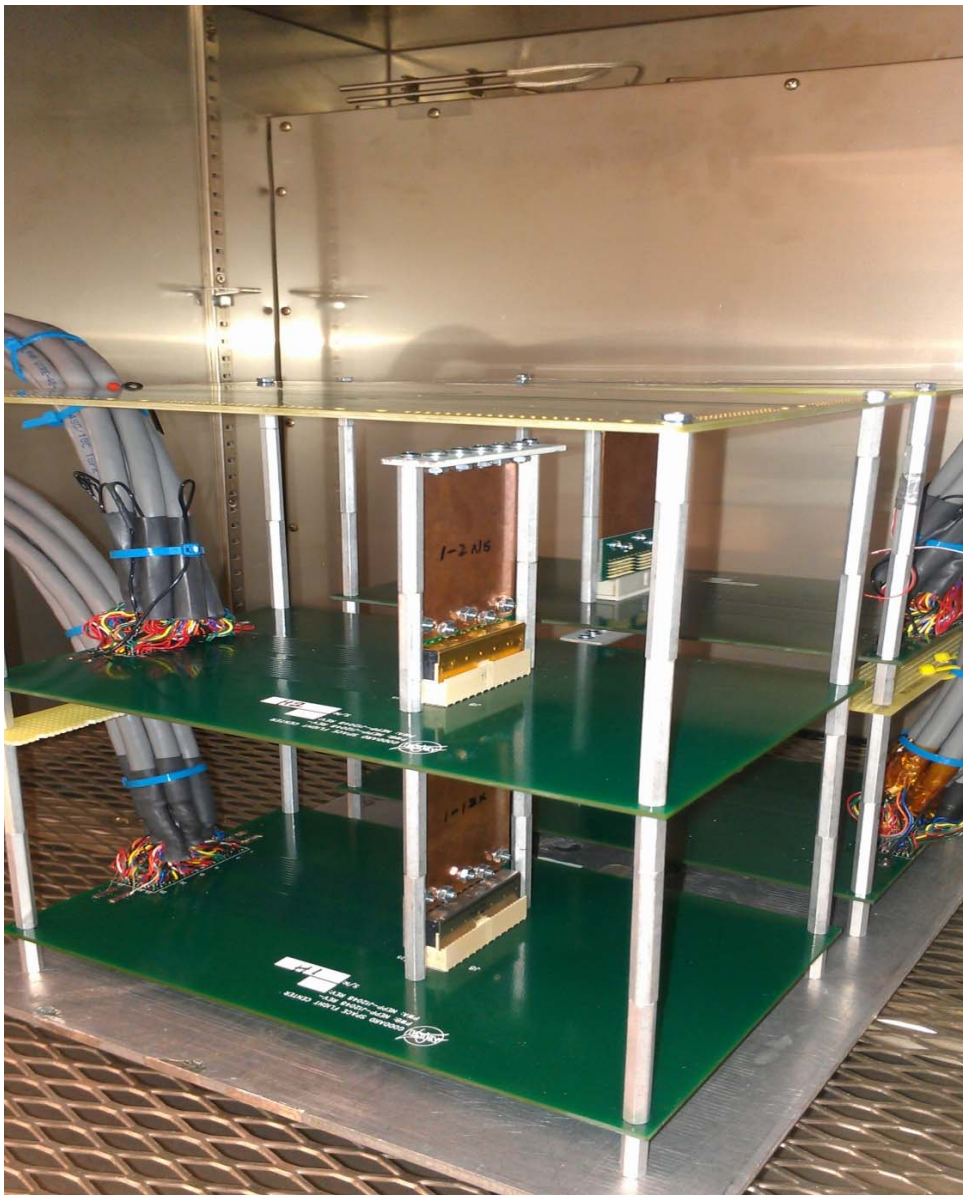

Figure 7: Test fixtures in the thermal chamber. Hypertronics 1 (Top left) Hypertronics 2 (Bottom Left) AMP (Top Right) AMP 2 (Bottom Right)

Note that the event detector provides no means of setting individual threshold voltages for all 110 pins of the CompactPCI® connector but instead sets a group threshold voltage in increments of 32 channels. Duration sensitivity of event detector is set to maximum to detect any intermittent duration equal or greater 100 ns. A test run is performed at room temperature to verify the setup is working properly. The CompactPCI® connectors should be sampled for Events in 24 hour increments until the target number of thermal cycle is reached. This would allow equal monitoring of all 440 channels under test. Since fretting is a progressive degenerative process, event occurrence is bound to increase with time. A visual examination along with any discrepancy in DC loop resistance should be recorded for all four test samples at the end of the test. Since the contact resistance is the only variable resistance in the setup, an increase in loop resistance is proportional to an increase in contact resistance.

5. TEST RESULT

Although the event detector sets a standard threshold voltage for a given group of channels, during data collection, each channel is evaluated individually to see if the failure criterion has been met for that channel. The event detection failure criteria was based on IPC-SM-785, with a 500 mΩ resistance level and a 100 nanosecond time duration. So any intermittent increase in resistance up to or above the delta resistance of 500 mΩ is logged by the Event detector as a failure. Figures 8a through 8d shows the number of intermittent pins detected versus time for all four connectors tested.

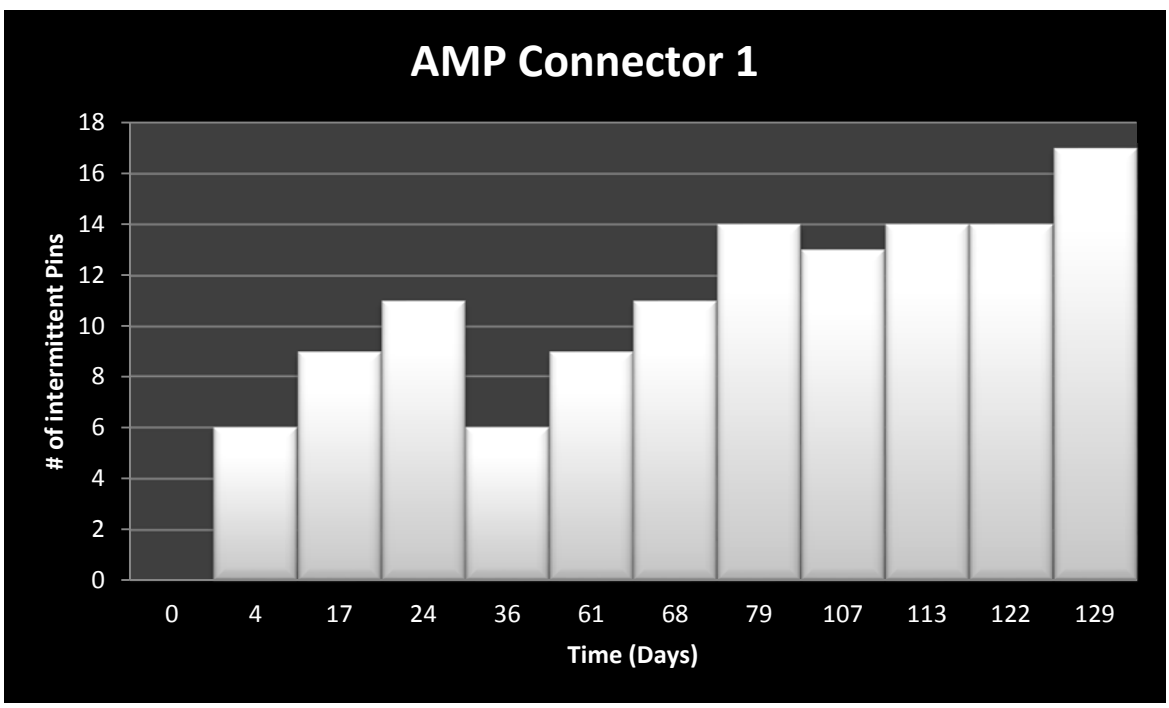

Figure 8a: Number of intermittent pins versus time for AMP Compact PIC Connector 1

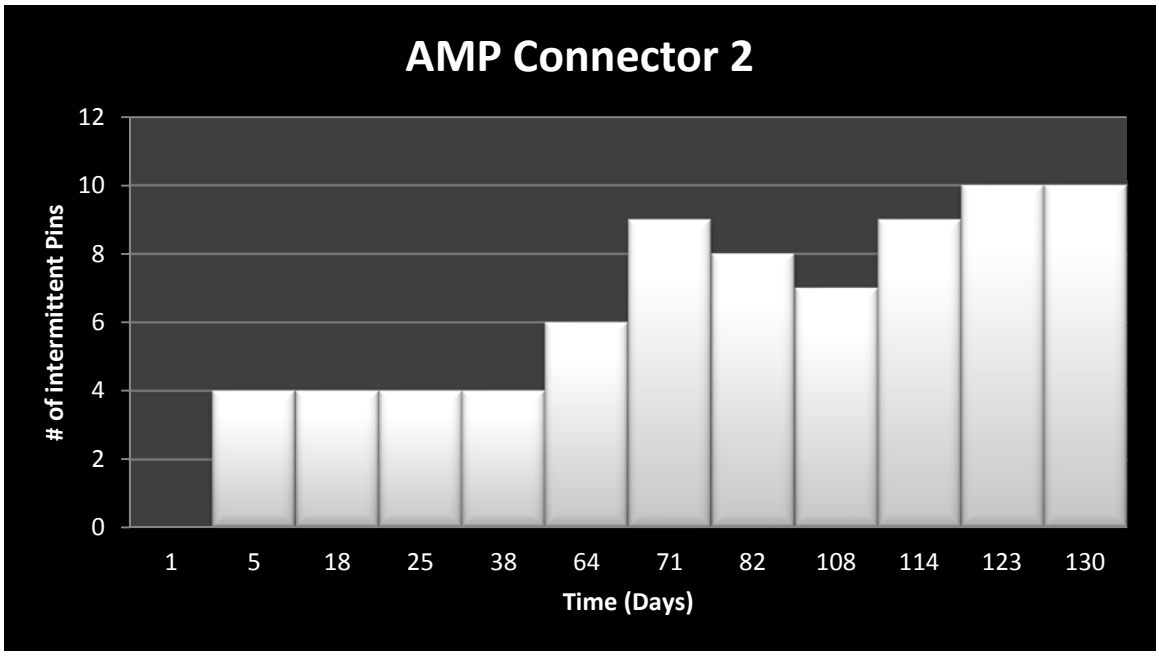

Figure 8b: Number of intermittent pins versus time for AMP Compact PIC Connector 2

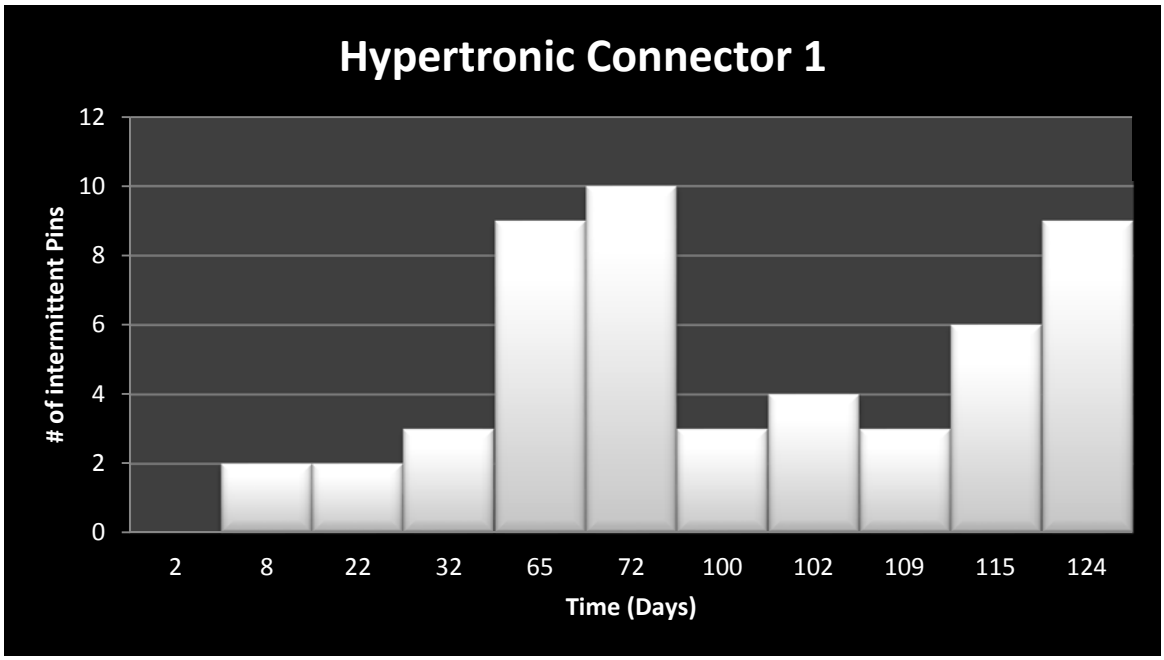

Figure 8c: Number of intermittent pins versus time for Hypertronics Connector 1

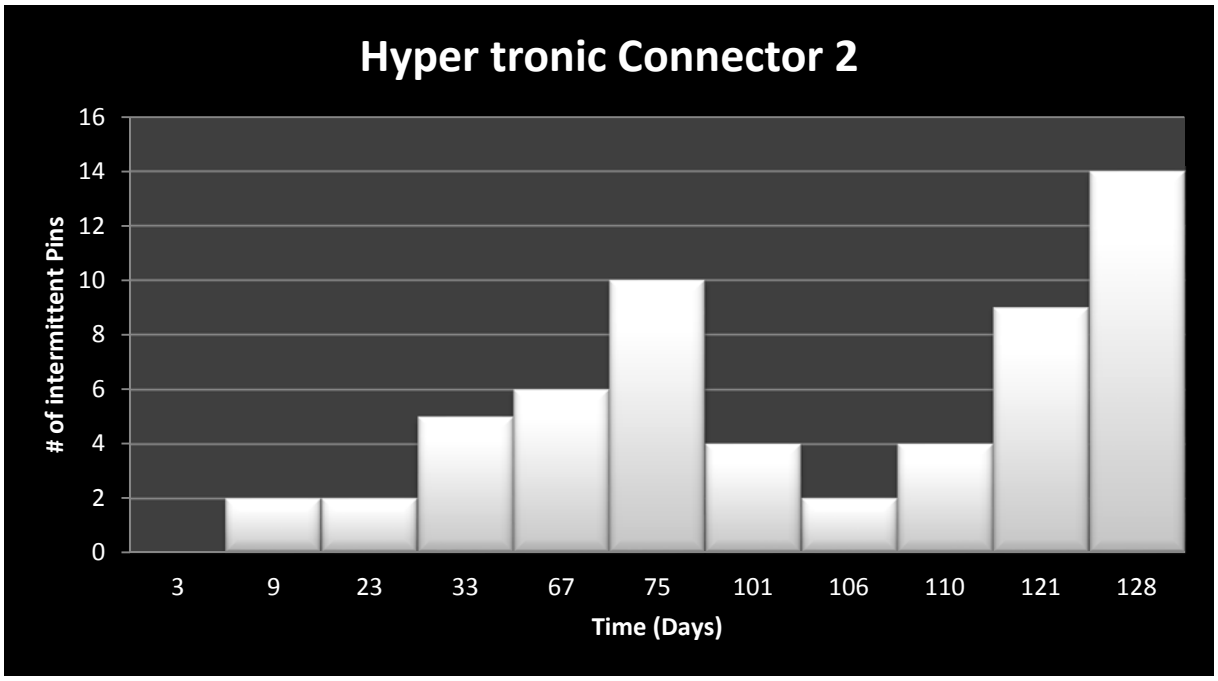

Figure 8d: Number of intermittent pins versus time for Hypertronics Connector 2

Looking at the total number of intermittent pins that were detected by the event detector, the AMP connector had a lot more intermittent pins on the average, with 17 being the highest number of intermittent pins per sample period when compared to the Hypertronics connectors. Also, unlike the connectors in Figures 9b through 9d, the AMP connector showed in Figure 9a had an above average initial loop resistance for some of the connector pins. This could be due to conductive debris lodged between the pin and socket because the loop resistance of those affected pins dropped within the average range of other pins in the circuit after the first 500 cycles. Table 3 below shows the average changes in circuit loop resistance for all 4 connectors after every 500 temperature cycles.

Table 3 Average changes in circuit loop resistance for all 4 connectors

Connector	Initial Circuit Loop Resistance	Circuit Loop resistance after 500 thermal cycles	Circuit Loop resistance after 1000 thermal Cycles	Circuit Loop resistance after 1500 thermal Cycles	Circuit Loop resistance after 2000 thermal Cycles
AMP1	1.855 Ω	1.928 Ω	2.039 Ω	1.977 Ω	1.977 Ω
AMP 2	1.841 Ω	1.874 Ω	1.935 Ω	1.943 Ω	1.956 Ω
Hypertronics 1	1.831 Ω	1.858 Ω	1.918 Ω	1.923 Ω	1.936 Ω
Hypertronics 2	1.833 Ω	1.880 Ω	1.934 Ω	1.934 Ω	1.942 Ω

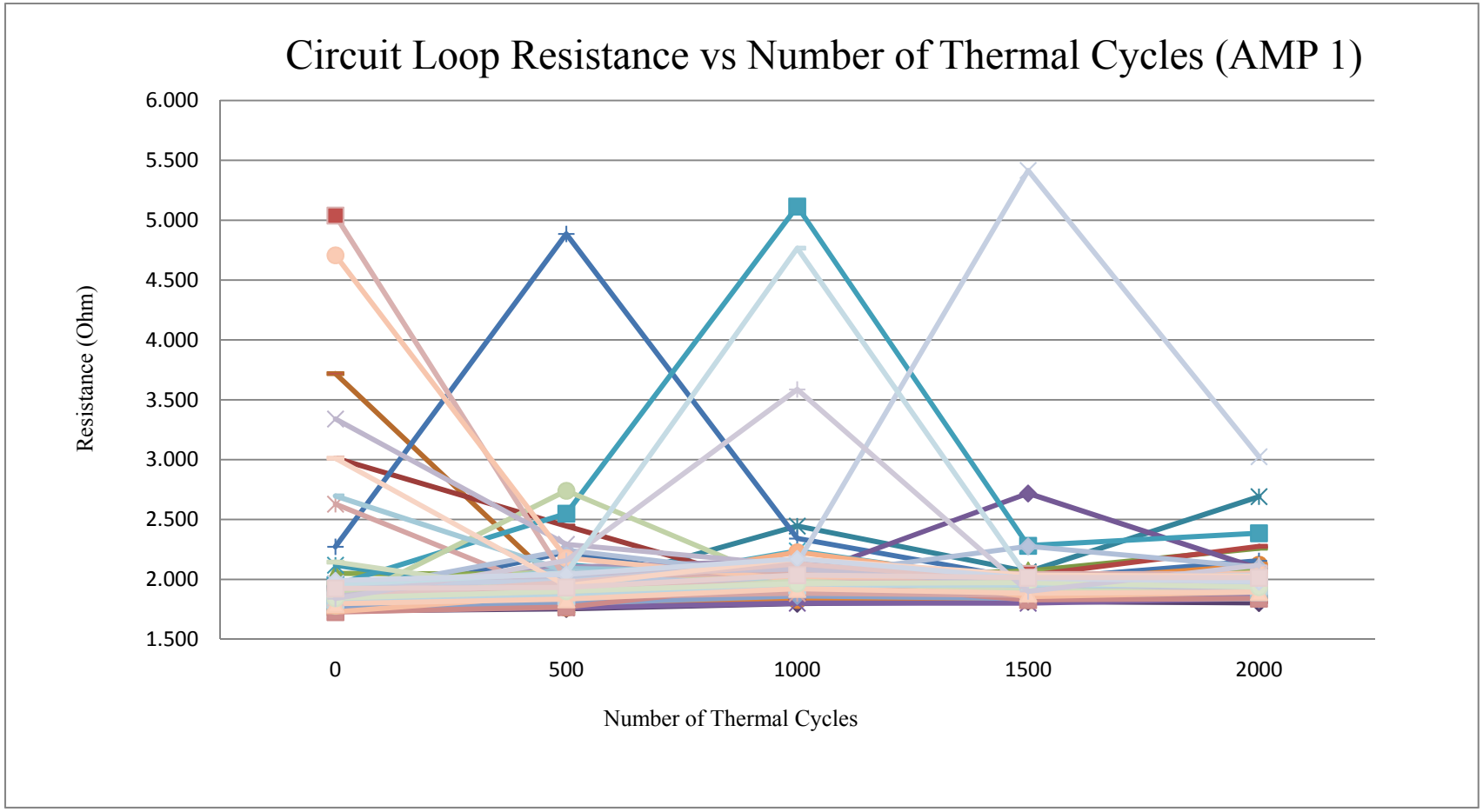

Figure 9a**:** Loop resistance for all 110 pins on the AMP connector 1 over the duration of test

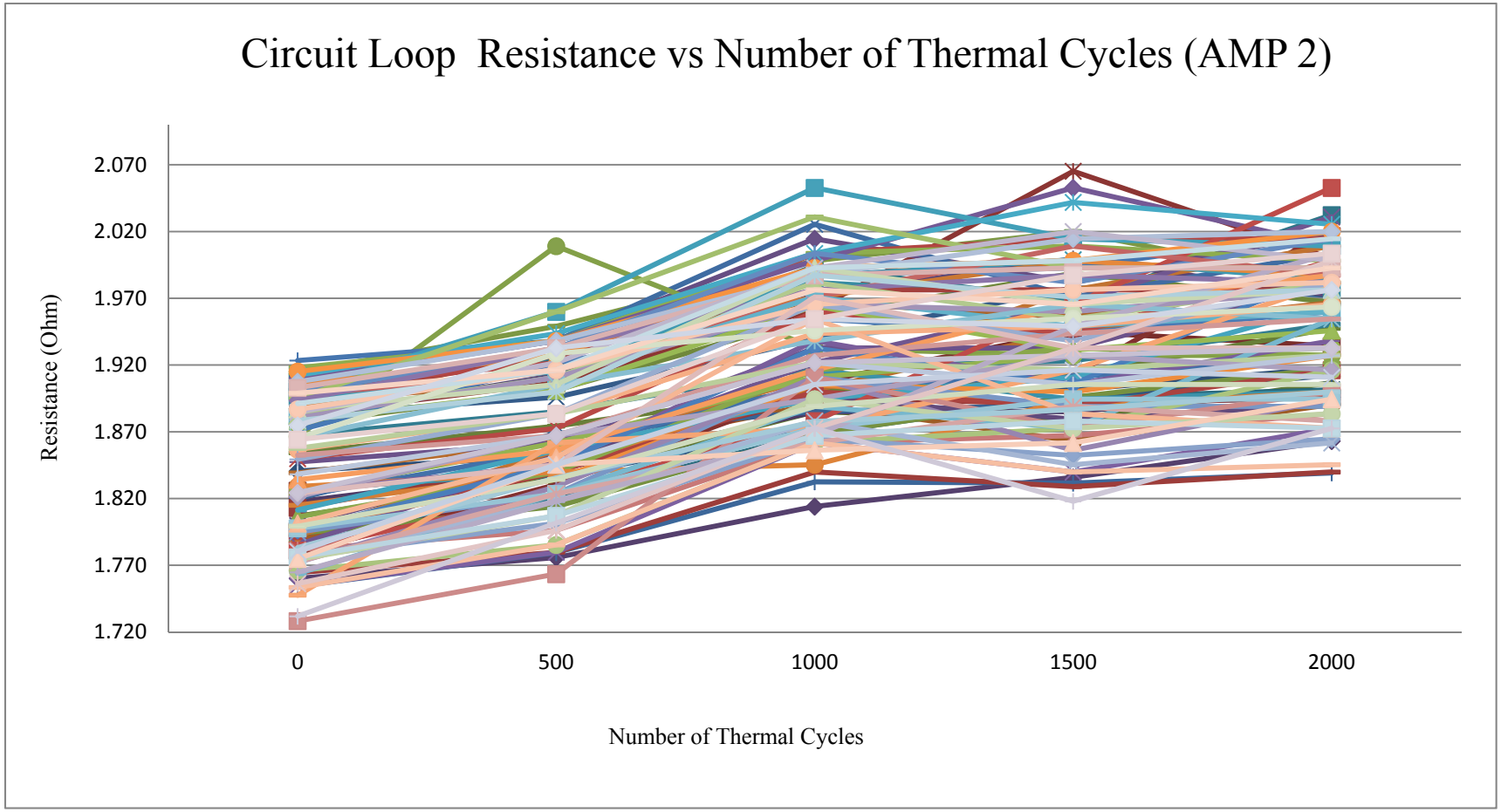

Figure 9b: Loop resistance for all 110 pins on the AMP connector 2 over the duration of test.

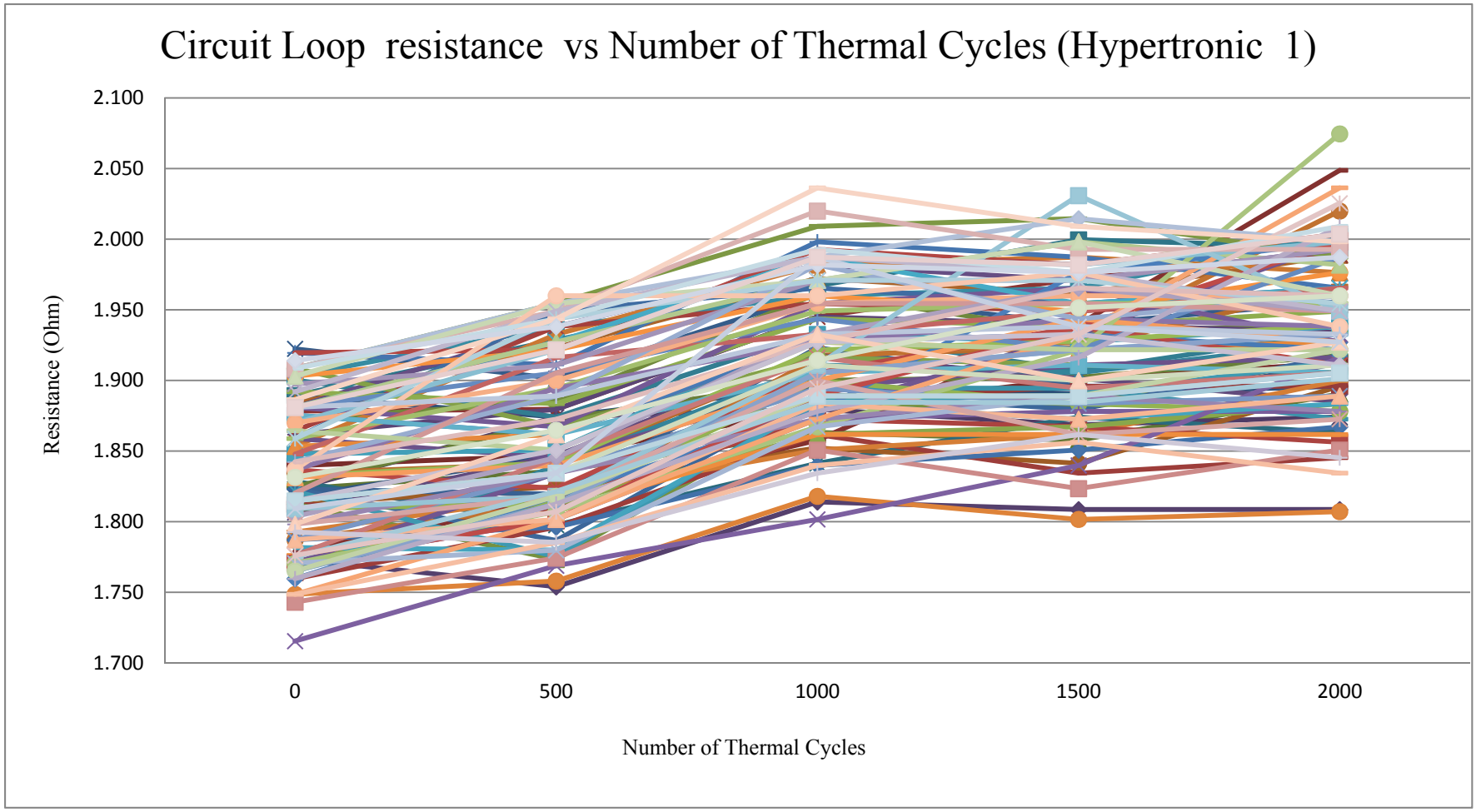

Figure 9c: Loop resistance for all 110 pins on the Hypertronics connector 1 over the duration of test.

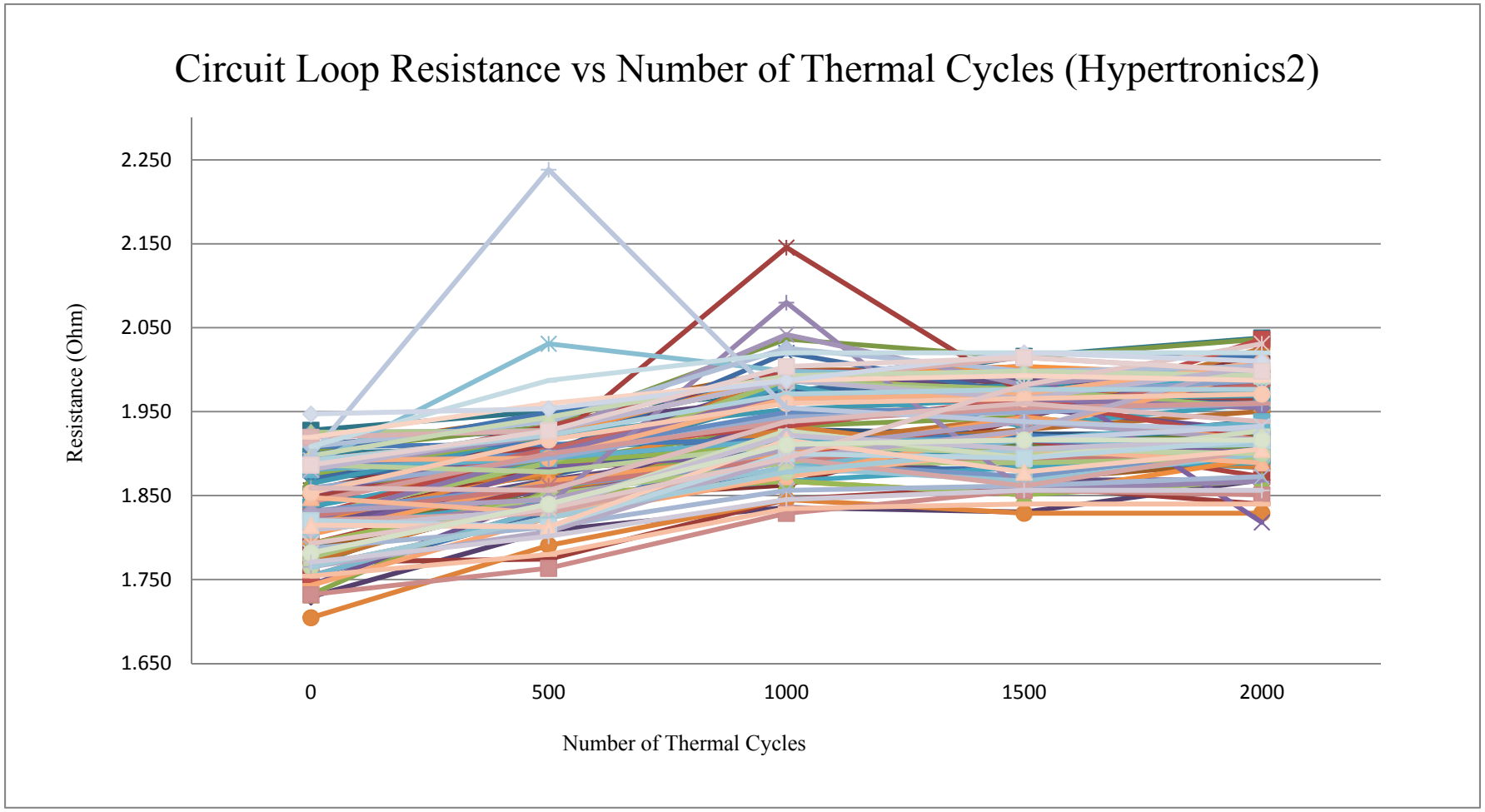

Figure 9d: Loop resistance for all 110 pins on the Hypertronics connector 2 over the duration of test.

Nevertheless, ignoring all above average initial loop resistance for the AMP connector 1, all four connectors tested follow a nearly identical pattern as shown in Figure 10. The slope of the graph shows a steep change in the loop resistance during the first 1000 cycles when compared to the slope between 1000 cycles and 2000 cycles.

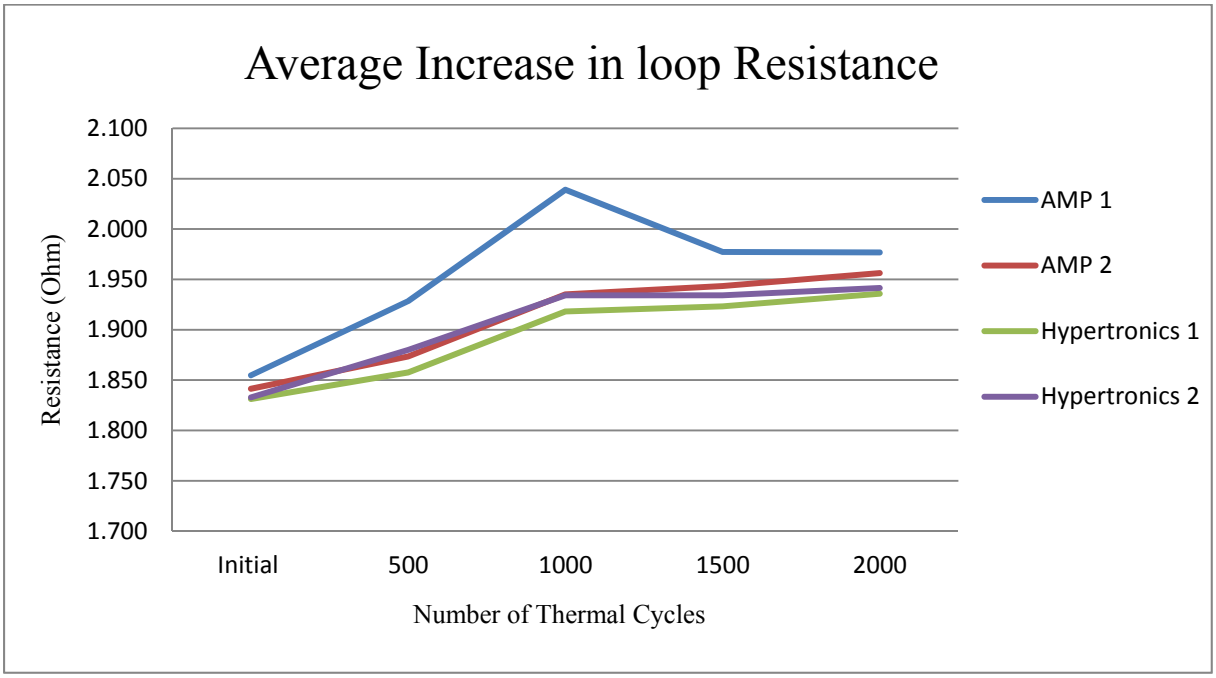

Figure 10: Average increase in loop resistance for all 4 connectors over the duration of test.

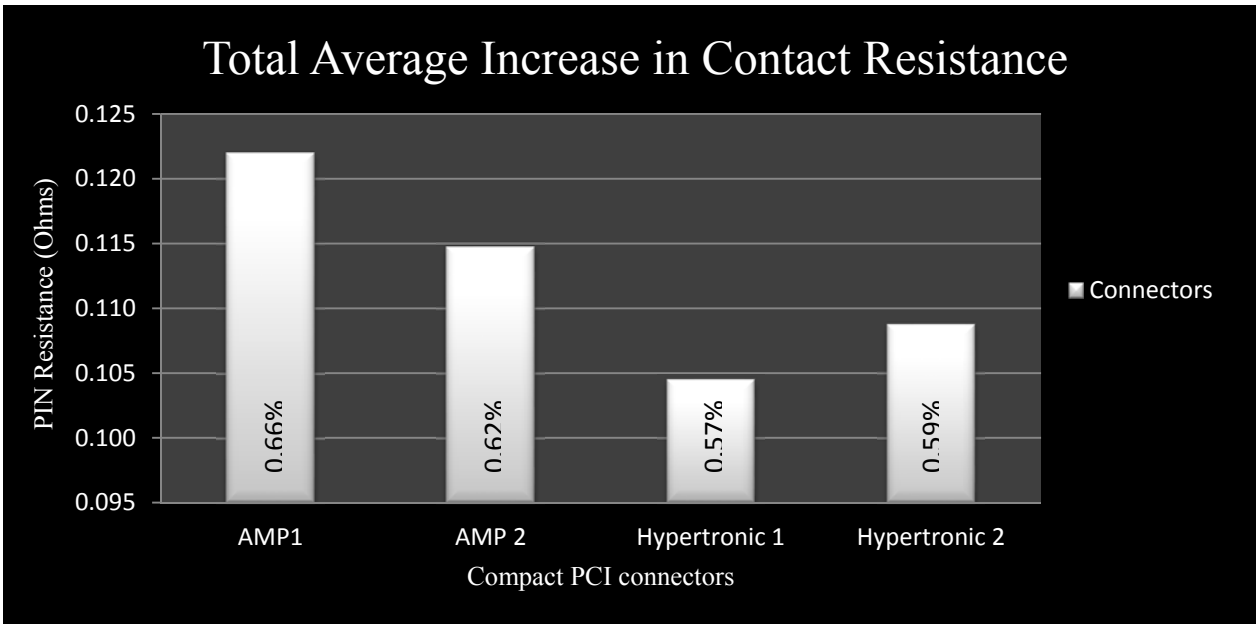

Figure 11: Total average increase in connector contact resistance for all four connectors.

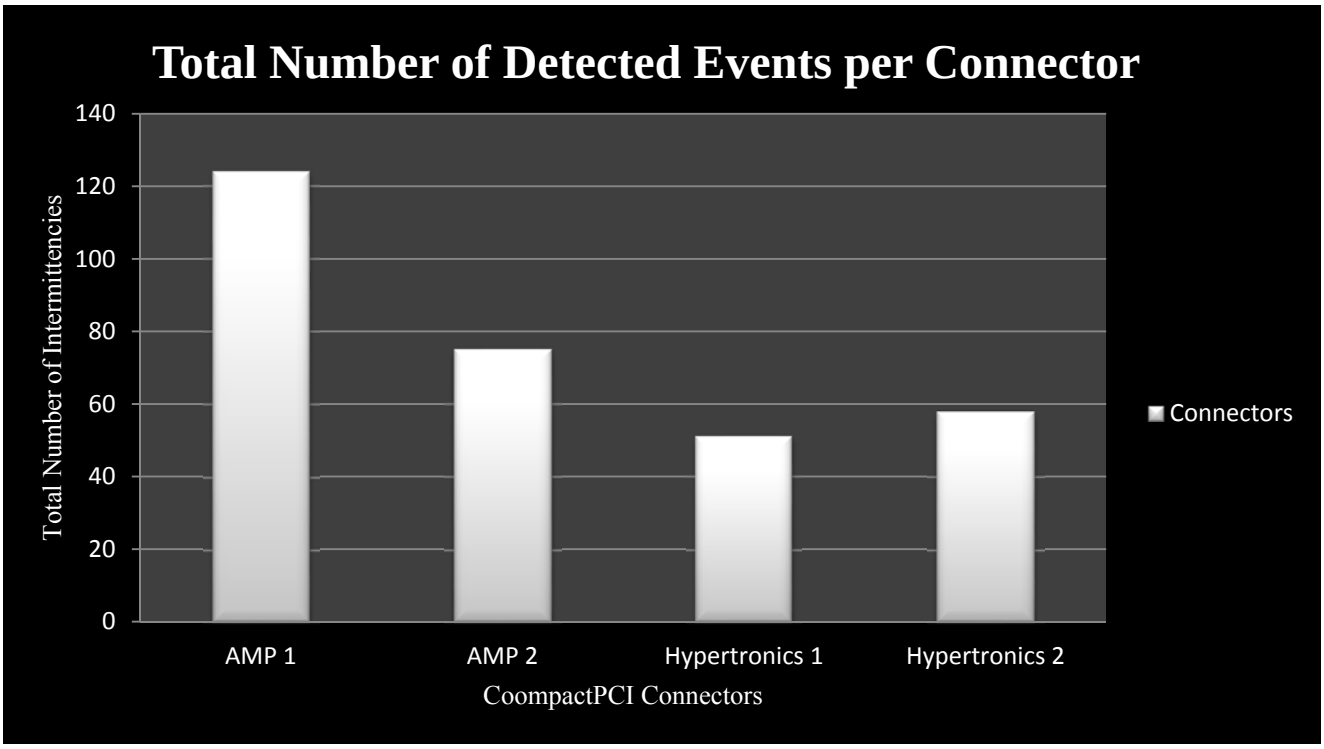

Figure 12: Total number of intermittencies detected for the duration of test.

In addition, there was an average increase in contact resistance of 0.116Ω for the AMP connectors. The Hypertronics on the other hand had an average increase of about 0.107Ω. Also looking at Figures 11 and 12, there seems to be a positive correlation between the total numbers of intermittences detected during the duration of test and the total average increase in connector contact resistance for all four connectors. A visual inspection of all four connectors showed several sites where the gold plating had worn down however, the wear out on the Amp connectors were severe enough to reveal the base metal at the contact points. Some of the Hypertac® wires and pins for the Hypertronics connectors were partially worn down due to pin and socket displacement during thermal cycle and thus had gold debris at those contact sites as shown in Figures 13 and 14. A closer examination of the Hypertronics female connector showed marking along the rim of the socket as shown in Figure 15.

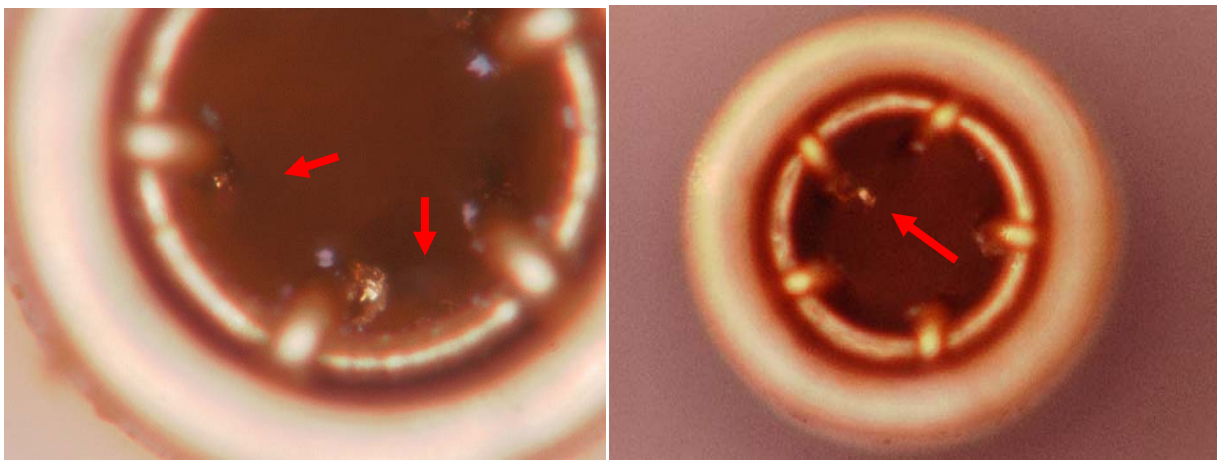

Figure 13: Worn down gold debris along Hypertac® wire.

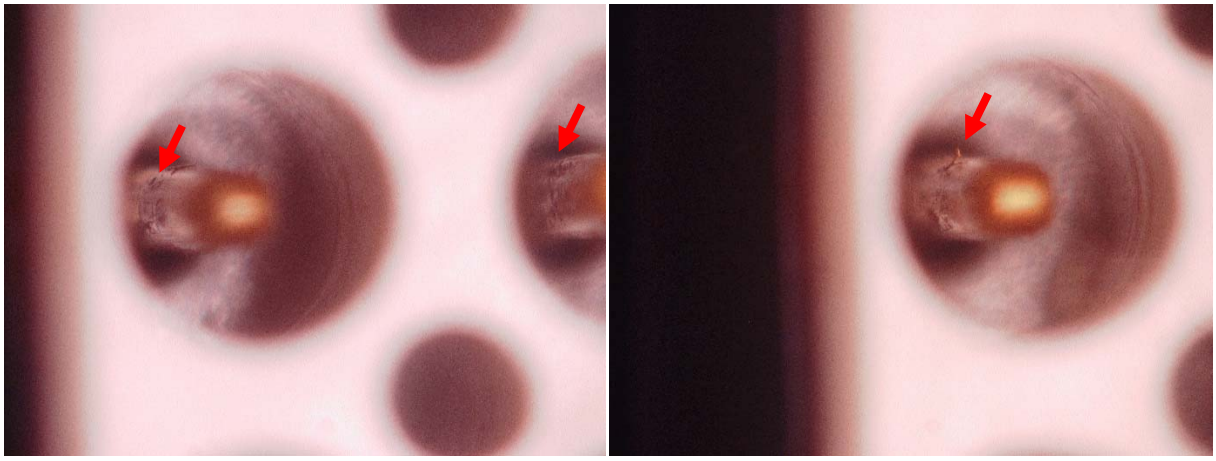

Figure 14: Worn down sites on Male pins of the Hypertronics connector.

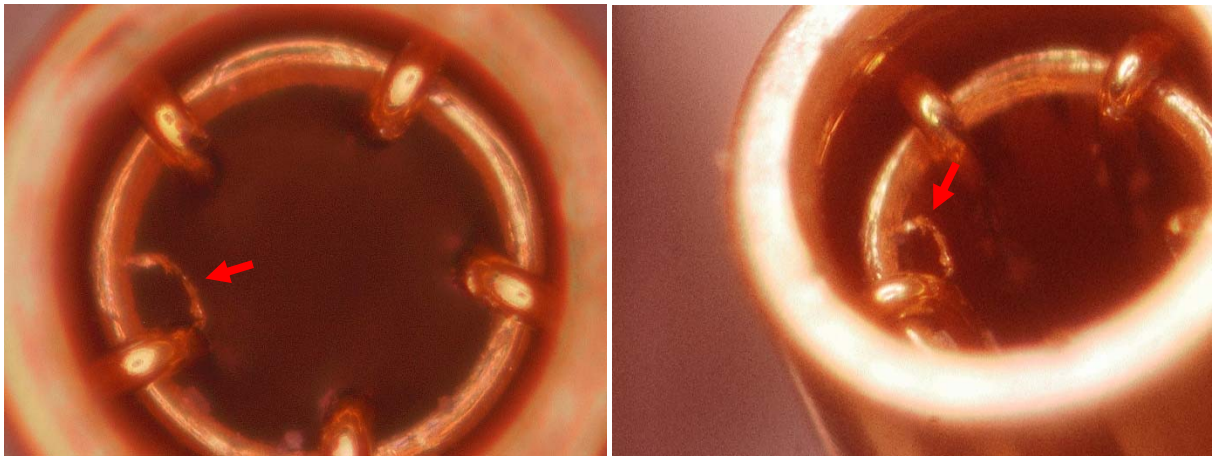

Figure 15: Top and side view of worn down site on the rim of the socket due to movement of Hypertac® wires.

This suggests that the Hypertac® wires are not secured in place either by a soldering or welding process. It is also possible that whatever process is implemented to restrict the movement of the Hypertac® wires was not strong enough to hold the wires in place. As a result, given the right conditions, these wires are free to slide along the rim of the socket thereby shedding gold debris inside the socket. Although the long term effect of this shedding process is unknown, debris build-up between two electrical contact points can effectively lead to a rapid increase in contact resistance.

In general, there were no deformations with the plastic housing geometry for all four connectors tested, however, due to the construction of the female AMP CompactPCI® connector, it was difficult to explicitly determine if there were any worn down sites at the contact point between the bifurcated tines. An optical examination showed no debris between the bifurcated tines at the end of the test. Nevertheless, over 65% of the AMP connectors male pins had worn down sites with lengths varying from 47µm to 82 µm.

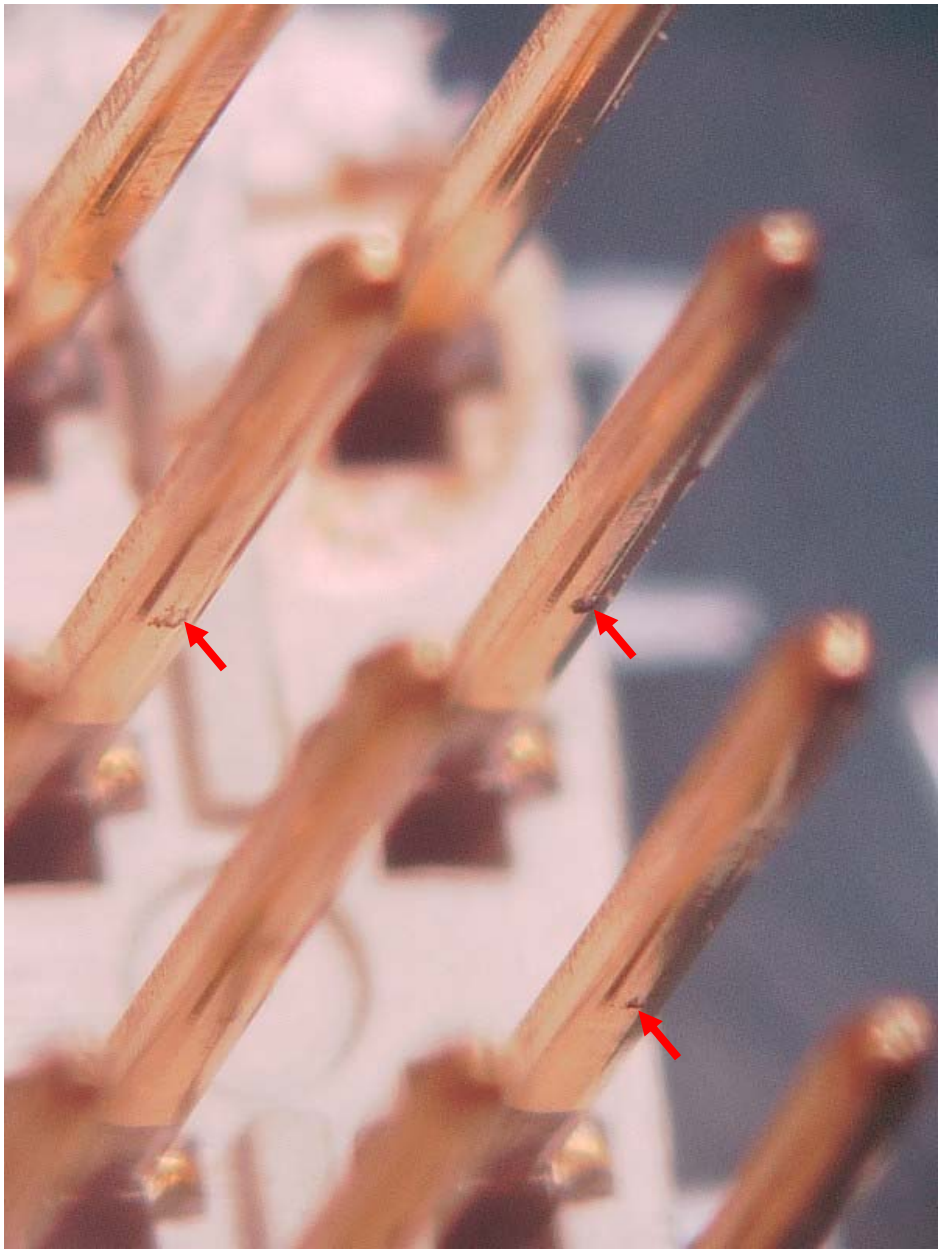

Figure 16: Worn down site on AMP male pins.

6. CONCLUSION

Both the Hypertronics and the AMP connector experienced intermittent electrical continuity during the thermal cycle process and had several sites with worn down gold plating. However, the gold and nickel under layer of the AMP connector contact sites were worn down enough to expose the base metal of the connector pins. This affected the signal integrity of both connectors by increasing the contact resistance of the individual pins in the connector which in turn increased the potential for intermittent open circuit faults. Nevertheless, the Hypertronics connectors had fewer intermittent failures when compared to the AMP connectors. The

frequency at which the intermittent failure occurred increased as the thermal cycling process progressed with time. Further evaluation is needed to understand how elevated temperature ranges like those seen on the solar panels of a spacecraft could affect the long term reliability of these connectors. At these temperature ranges, particular attention should be focused on possible deformation in plastic housing geometry, unequal spacing between pins and changes in pin retention force due to longer fretting distances.

7. RECOMMENDATION

An ideal evaluation would involve testing the CompactPCI® connectors for Events throughout the length of a proposed mission. When this approach is not feasible these simple guidelines outlined below should be observed.

- When a cPCI connector is needed for flight application use only space qualified connectors as specified in S-311-P-822[5]
- Use connectors with more than three contact points per socket such as the Hypertronics 2mm cPCI connector
- Use connector savers for flight connectors to prevent premature change in contact resistance due to fretting as a result of frequent mating and de-mating sessions.
- Do not use cPCI connectors with press-fit technologies for space flight applications. NASA discourages the use of press-fit termination for flight application and prefers all components to be soldered in place. There are numerous problems that could result from soldering these terminations since they generally don't have a solderability requirement.

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